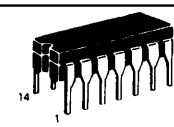
MC54/74HCU04

Hex Unbuffered Inverter
High Performance Silicon-Gate CMOS

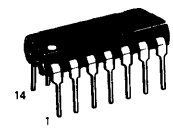
The MC54/74HCU04 is identical in pinout to the LSO4 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single-stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high-input impedance amplifier. For digital applications, the HC04 is recommended.

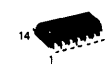
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V; 2.5 to 6 V in Oscillator Configurations
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 12 FETs or 3 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



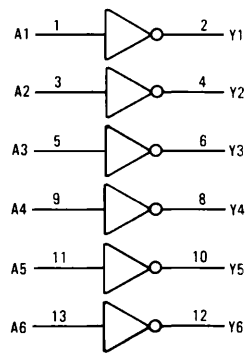
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC74HCUXXN	Plastic
MC54HCUXXJ	Ceramic
MC74HCUXXD	SOIC

T_A = −55° to 125°C for all packages.
Dimensions in Chapter 6.

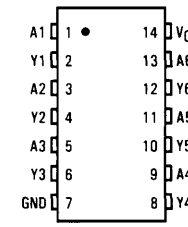
LOGIC DIAGRAM



$Y = \overline{A}$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs A	Outputs Y
L	H
H	L

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \le (V_{in} \text{ or } V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in},V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	No Limit	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit 25°C to −55°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.5 V* $\lvert I_{out}\rvert \le 20\ \mu A$	2.0	1.7	1.7	1.7	V
			4.5	3.6	3.6	3.6	
			6.0	4.8	4.8	4.8	
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = V_{CC} − 0.5 V* $\lvert I_{out}\rvert \le 20\ \mu A$	2.0	0.3	0.3	0.3	V
			4.5	0.8	0.8	0.8	
			6.0	1.1	1.1	1.1	
V_{OH}	Minimum High-Level Output Voltage	V_{in} = GND $\lvert I_{out}\rvert \le 20\ \mu A$	2.0	1.8	1.8	1.8	V
			4.5	4.0	4.0	4.0	
			6.0	5.5	5.5	5.5	
		V_{in} = GND $\lvert I_{out}\rvert \le 4.0$ mA	4.5	3.86	3.76	3.70	
		$\lvert I_{out}\rvert \le 5.2$ mA	6.0	5.36	5.26	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{CC} $\lvert I_{out}\rvert \le 20\ \mu A$	2.0	0.2	0.2	0.2	V
			4.5	0.5	0.5	0.5	
			6.0	0.5	0.5	0.5	
		V_{in} = V_{CC} $\lvert I_{out}\rvert \le 4.0$ mA	4.5	0.32	0.37	0.40	
		$\lvert I_{out}\rvert \le 5.2$ mA	6.0	0.32	0.37	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.
*For V_{CC} = 2.0 V, V_{out} = 0.2 V or V_{CC} − 0.2 V.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 15	pF

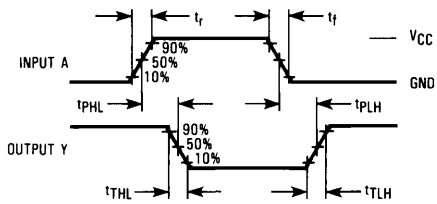
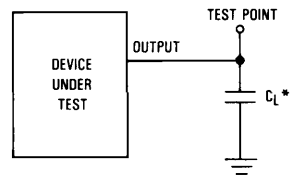


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

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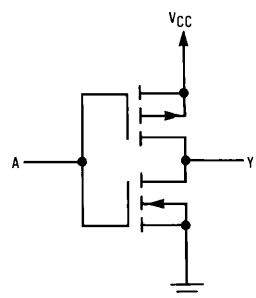
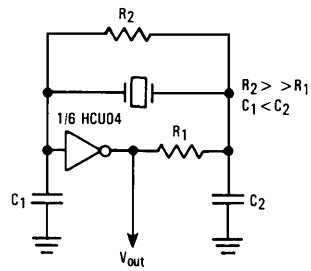
LOGIC DETAIL
(1/6 of Device Shown)

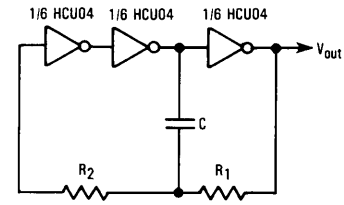


TYPICAL APPLICATIONS

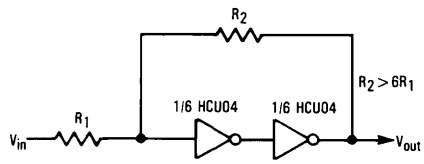
Crystal Oscillator



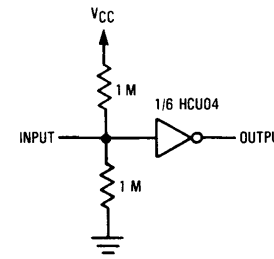
Stable RC Oscillator



Schmitt Trigger



High Input Impedance Single-Stage Amplifier with a 2 to 6 V Supply Range



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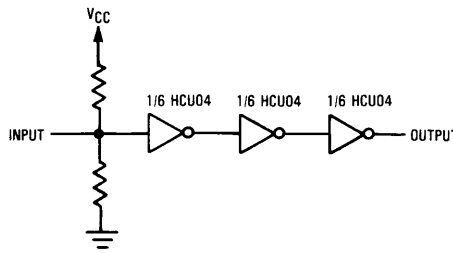
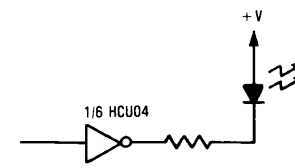
Multi-Stage Amplifier



LED Driver



For reduced power supply current, use high-efficiency LEDs such as the Hewlett-Packard HLMP series or equivalent.