MOTOROLA

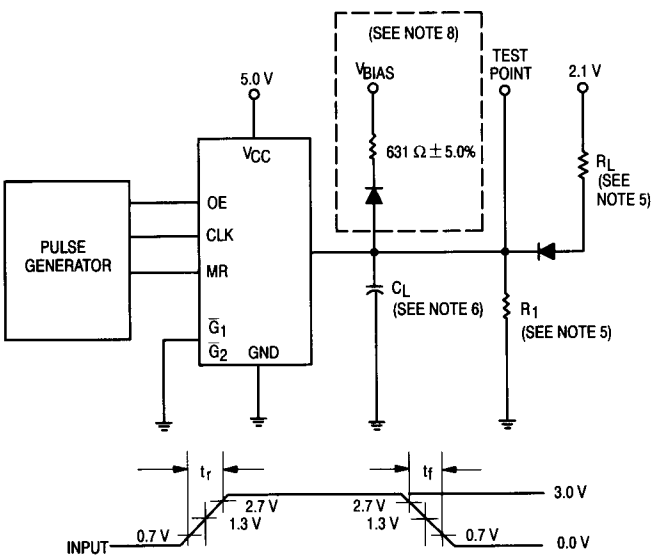
4-Bit D-Type Register With 3-State Outputs

ELECTRICALLY TESTED PER:
MPG54LS173

The 54LS173 is a high-speed 4-bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable lines ($\overline{IE}_1$, $\overline{IE}_2$). A HIGH on either Output Enable line ($\overline{OE}_1$, $\overline{OE}_2$) brings the output to a high impedance state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the Register regardless of the state of the clock (CP), the Output Enable ($\overline{OE}_1$, $\overline{OE}_2$) or the Input Enable ($\overline{IE}_1$, $\overline{IE}_2$) lines.

- Fully Edge-Triggered
- 3-State Outputs
- Gated Input and Output Enables
- Input Clamp Diodes Limit High-Speed Termination Effects

TEST CIRCUIT AND WAVEFORM



NOTES:
1. The Input pulse generator has the following characteristics: V_{gen} = 3.0 V, $t_r \leq 6.0$ ns between 0.7 V and 2.7 V, $t_f \leq 6.0$ ns between 0.7 V and 2.7 V, PRR ≤ 1.0 MHz, and $Z_{OUT} \approx 50\ \Omega$.
2. Clear input pulse characteristics are as follows: $t_{p(CLR)}$ = 20 ns.
3. Clock input pulse characteristics are as follows: $t_{p(CLOCK)}$ = 20 ns.
4. Data input pulse characteristics are as follows: t_{setup} = 17 ns, t_{hold} = 5.0 ns.
5. $R_1 = 2.4\ k\Omega \pm 5.0\%$, $R_L = 110\ \Omega \pm 5.0\%$.
6. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance without package in test fixture.
7. All diodes are 1N3064 or equivalent.
8. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all test except for t_{PHZ}; for t_{PHZ} test, V_{BIAS} shall be -0.6 V.
9. Voltage values are with respect to ground terminal.
10. Terminal conditions (pins not designed may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Military 54LS173

AVAILABLE AS:

1) JAN: N/A
2) SMD: N/A
3) 883: 54LS173/BXAJC

X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{OE}_1$	1	1	2	GND
$\overline{OE}_2$	2	2	3	GND
Q_0	3	3	4	OPEN
Q_1	4	4	5	OPEN
Q_2	5	5	7	OPEN
Q_3	6	6	8	OPEN
CP	7	7	9	V_{CC}
GND	8	8	10	GND
$\overline{IE}_1$	9	9	12	V_{CC}
$\overline{IE}_2$	10	10	13	V_{CC}
D_3	11	11	14	V_{CC}
D_2	12	12	15	V_{CC}
D_1	13	13	17	V_{CC}
D_0	14	14	18	V_{CC}
MR	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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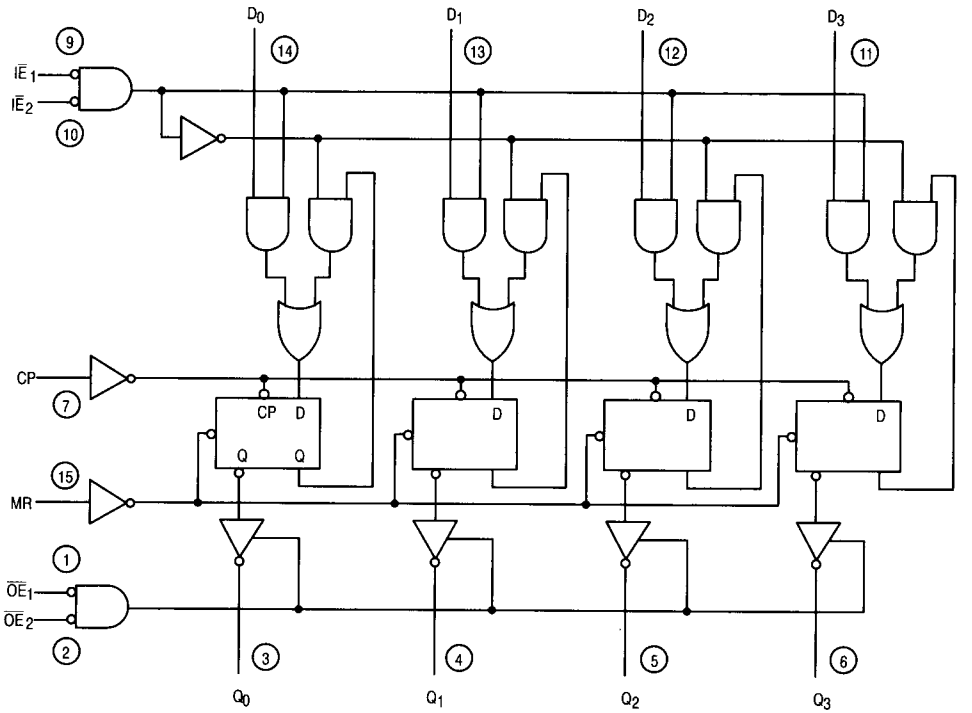
LOGIC DIAGRAM



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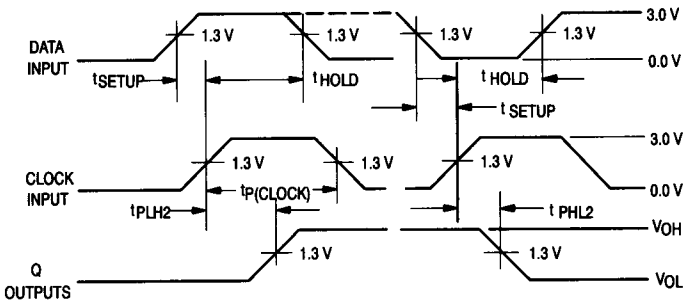
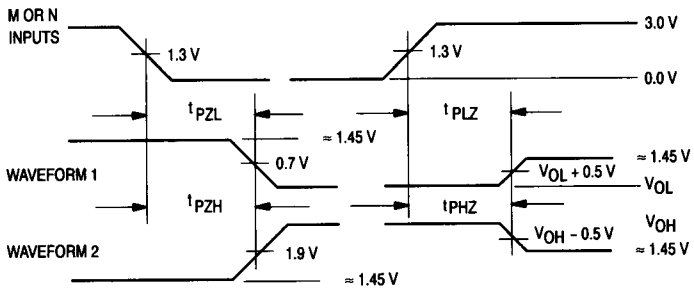
TRUTH TABLE					
MR	CP	$\overline{IE}_1$	$\overline{IE}_2$	D_n	D_n
H	X	X	X	X	L
L	L	X	X	X	Q_n
L	⌐	H	X	X	Q_n
L	⌐	X	H	X	Q_n
L	⌐	L	L	L	L
L	⌐	L	L	H	H

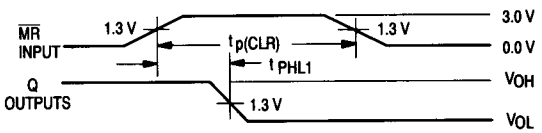
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
When either $\overline{OE}_1$, or $\overline{OE}_2$ are HIGH, the output is in the off state (High Impedance); however this does not affect the contents or sequential operation of the register.

CLOCK TO Q OUTPUTS



TRI-STATE SWITCHING





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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = − 1.0 mA, V_{IN} = 2.0 V, CP = (See Note 1), $\overline{IE}$ = 0.7 V, MR & $\overline{OE}$ = GND.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IN} = 0.7 V, CP = (See Note 1), MR & $\overline{OE}$ = GND.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open, $\overline{IE}$ = (− 18 mA) or GND.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{IE}$ = (2.7 V) or GND.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open, $\overline{IE}$ = (5.5 V) or GND.
I_{IL}	Logical "0" Input Current		− 400		− 400		− 400	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, $\overline{IE}$ = (0.4 V) or GND, other inputs are open.
I_{OZH}	Output Off Current High		20		20		20	mA	V_{CC} = 5.5 V, $V_{IN(MR)}$ = 4.5 V, $\overline{OE}_1$ = 2.0 V, $\overline{OE}_2$ = GND, V_{OUT} = 2.7 V, other inputs are open.
I_{OZL}	Output Off Current Low		− 20		− 20		− 20	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, MR = GND, CP = (See Note 1), V_{OUT} = 0.7V, $\overline{OE}_1$ = 2.0 V, other inputs are GND.
I_{OS}	Short Circuit Output Current	− 30	− 130	− 30	− 130	− 30	− 130	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, V_{OUT} = GND, CP (See Note 2), other inputs are GND.
I_{CC}	Power Supply Current Off		30		30		30	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, MR = (See Note 2), other inputs are GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subqroup 8B			per Truth Table with V_{CC} = 4.5 V, **(Repeat at)** V_{CC} = 5.5 V. V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

NOTE:

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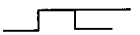
2. 

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output MR to Output	2.0 —	30 35	2.0 —	40 44	2.0 —	40 44	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 2.4 k Ω, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output CP to Output	2.0 —	35 30	2.0 —	45 38	2.0 —	45 38	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 2.4 k Ω, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output CP to Output	2.0 —	25 25	2.0 —	35 30	2.0 —	35 30	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 2.4 k Ω, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZH} t_{PZH}	Propagation Delay Output Enable Time	2.0 —	23 23	2.0 —	33 28	2.0 —	33 28	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 2.4 k Ω, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZL} t_{PZL}	Propagation Delay Output Enable Time	2.0 —	27 27	2.0 —	37 32	2.0 —	37 32	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 2.4 k Ω, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHZ} t_{PHZ}	Propagation Delay Output Disable Time	2.0 —	30 17	2.0 —	40 35	2.0 —	40 35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 2.4 k Ω, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLZ} t_{PLZ}	Propagation Delay Output Disable Time	2.0 —	22 17	2.0 —	32 27	2.0 —	32 27	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 2.4 k Ω, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
f_{MAX}	Maximum Clock Frequency	25 30		20 —		20 —		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 2.4 k Ω, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.

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