



3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

IDT74LVCH16952A

FEATURES:

- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

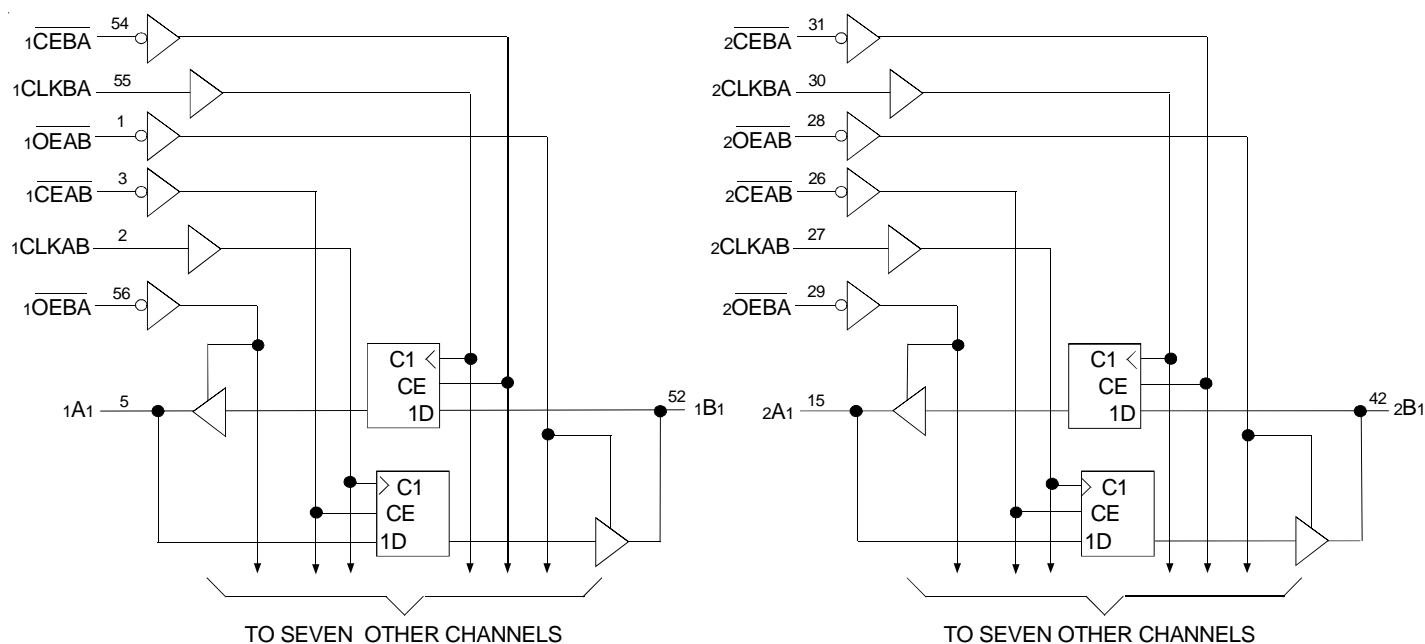
DESCRIPTION:

This 16-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit D-type registered transceivers with separate input and output control for independent control of data flow in either direction. For example, the A-to-B Enable (\overline{CEAB}) must be LOW to enter data from the A port. CLKAB controls the clocking function. When CLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. \overline{OEAB} performs the output enable function on the B port. Data flow from the B port to A port is similar but requires using \overline{CEBA} , CLKBA, and \overline{OEBA} inputs. Full 16-bit operation is achieved by tying the control pins of the independent transceivers together.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

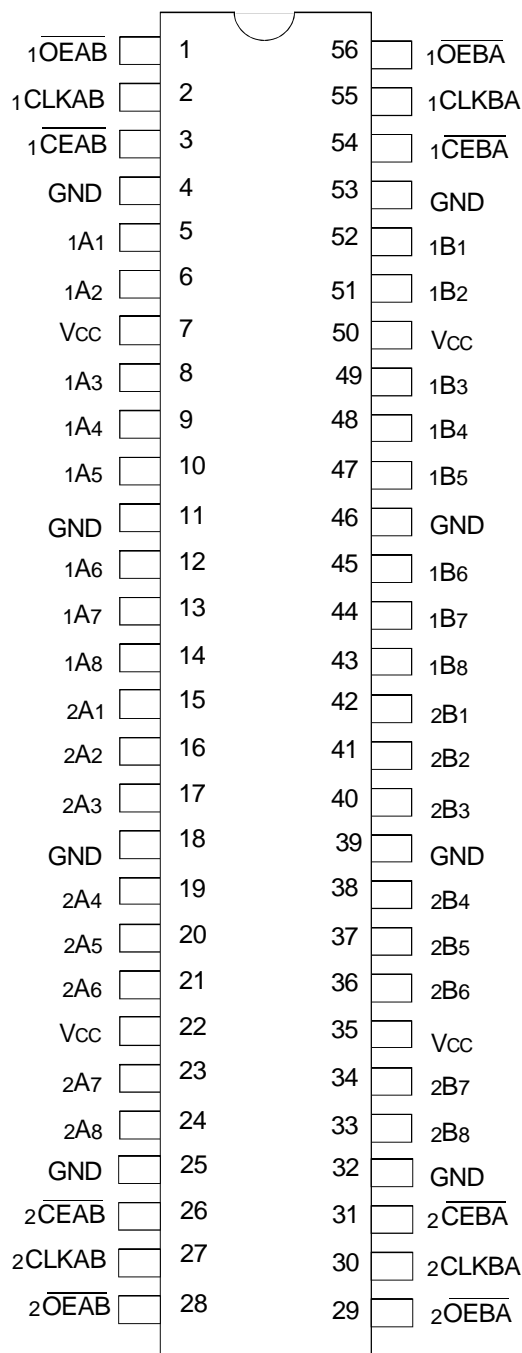
The LVCH16952A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	VIN = 0V	6.5	8	pF

NOTE:

1. As applicable to the device type.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, VI < 0 or VO < 0	-50	mA
I _{CC} I _{SS}	Continuous Current through each Vcc or GND	±100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Names	Description
x \overline{OEAB}	A-to-B Output Enable Inputs (Active LOW)
x \overline{OEBA}	B-to-A Output Enable Inputs (Active LOW)
x \overline{CEAB}	A-to-B Clock Enable Inputs (Active LOW)
x \overline{CEBA}	B-to-A Clock Enable Inputs (Active LOW)
xCLKAB	A-to-B Clock Inputs
xCLKBA	B-to-A Clock Inputs
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE^(1,2)

Inputs				Outputs
x \overline{CEAB}	xCLKAB	x \overline{OEAB}	xAx	xBx
H	X	L	X	B ⁽³⁾
X	L	L	X	B ⁽³⁾
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES:

- A-to-B data flow is shown: B-to-A data flow is similar but uses x \overline{CEBA} , xCLKBA, and x \overline{OEBA} .
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition
- Output level of B before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

NOTES:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3V	V _I = 2V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	—	—	—	μA
			V _I = 0.7V	—	—	—	
I _{BHO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

NOTES:

- Pins with Bus-Hold are identified in the pin description.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V		IOH = - 24mA	2	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

NOTE:
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	CL = 0pF, f = 10Mhz	87	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		43	

SWITCHING CHARACTERISTICS⁽¹⁾

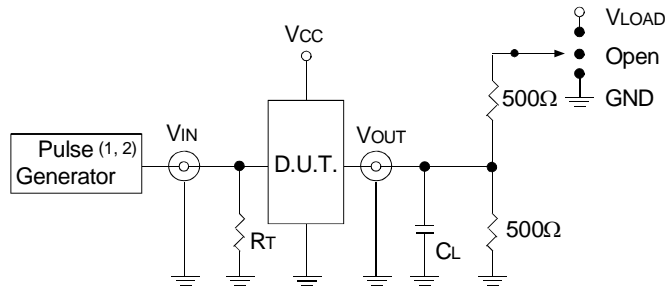
Symbol	Parameter	VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
fMAX		150	—	150	—	MHz
tPLH	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	—	7.6	1.6	6.6	ns
tPHL						
tPZH	Output Enable Time	—	8	1.1	6.6	ns
tPZL	xOEBA, xOEAB to xAx, xBx					
tPHZ	Output Disable Time	—	7.1	1.9	6.7	ns
tPLZ	xOEBA, xOEAB to xAx, xBx					
tsu	Set-up Time, data before xCLKAB↑, xCLKBA↑	3.4	—	2.8	—	ns
tH	Hold Time, data after xCLKAB↑, xCLKBA↑	0.5	—	0.5	—	ns
tsu	Set-up Time, xCEAB, xCEBA before xCLKAB↑, xCLKBA↑	1.8	—	1.4	—	ns
tH	Hold Time, xCEAB, xCEBA after xCLKAB↑, xCLKBA↑	1.1	—	1.9	—	ns
tW	Pulse Duration HIGH or LOW, xCLKAB or xCLKBA	3.3	—	3.3	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	1	ns

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ = 3.3V ± 0.3V	V _{CC} ⁽¹⁾ = 2.7V	V _{CC} ⁽²⁾ = 2.5V ± 0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



LVC Link

Test Circuit for All Outputs

DEFINITIONS:

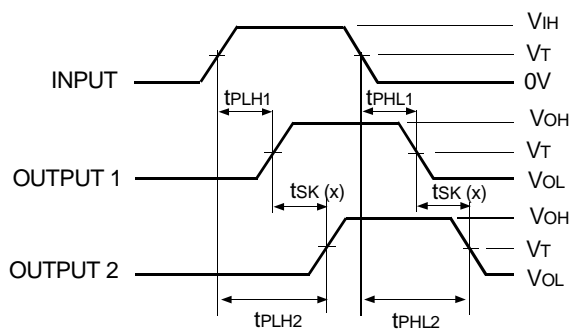
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



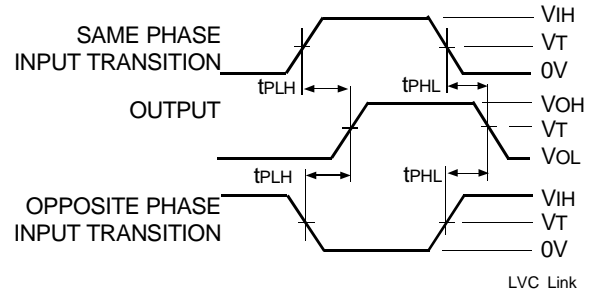
$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

LVC Link

Output Skew - tsk(x)

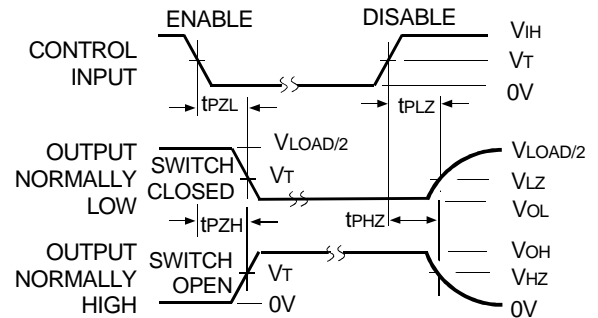
NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



LVC Link

Propagation Delay

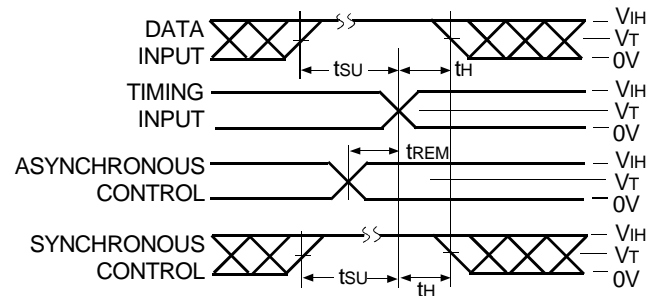


LVC Link

Enable and Disable Times

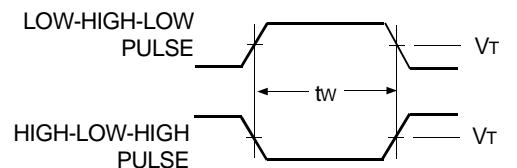
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



LVC Link

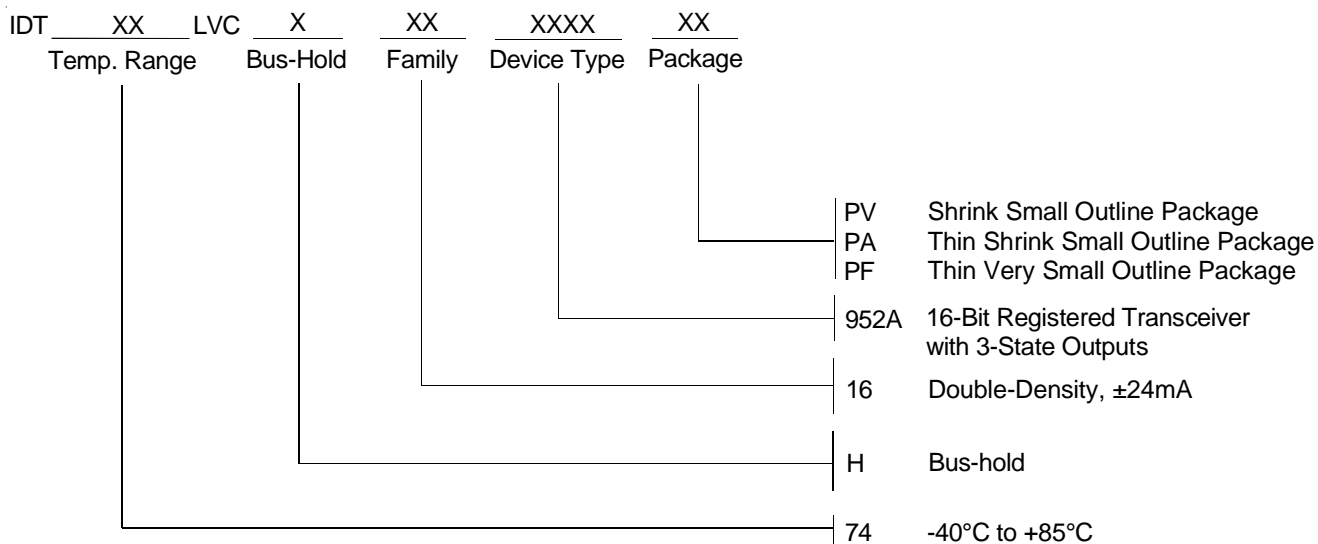
Set-up, Hold, and Release Times



LVC Link

Pulse Width

ORDERING INFORMATION



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