COS/MOS INTEGRATED CIRCUIT

4030B

HCC/HCF 4030B

QUAD EXCLUSIVE - OR GATE

- MEDIUM-SPEED OPERATION - $t_{PHL}= t_{PLH}= 60$ ns (TYP.) @ $C_L= 50$ pF and $V_{DD}-V_{SS}= 10V$
- LOW OUTPUT IMPEDANCE: 500Ω (TYP.) @ $V_{DD}-V_{SS}= 10V$
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD NO. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4030B** (extended temperature range) and **HCF 4030B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package, ceramic flat package and plastic micropackage.
The **HCC/HCF 4030B** types consist of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four n-channel and four p-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

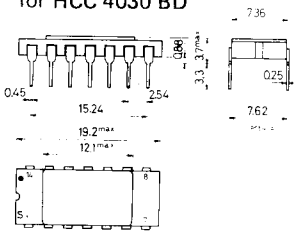
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

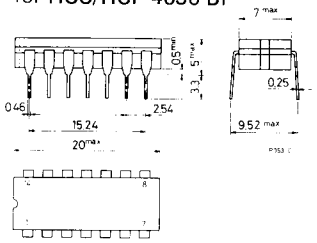
HCC 4030 BD for dual in-line ceramic package
HCC 4030 BF for dual in-line ceramic package, frit seal
HCC 4030 BK for ceramic flat package
HCF 4030 BE for dual in-line plastic package
HCF 4030 BF for dual in-line ceramic package, frit seal
HCF 4030 BM for plastic micropackage

MECHANICAL DATA (dimensions in mm)

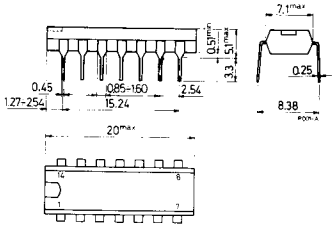
Dual in-line ceramic package for HCC 4030 BD



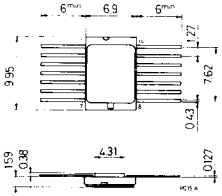
Dual in-line ceramic package for HCC/HCF 4030 BF



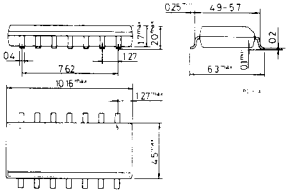
Dual in-line plastic package for HCF 4030 BE



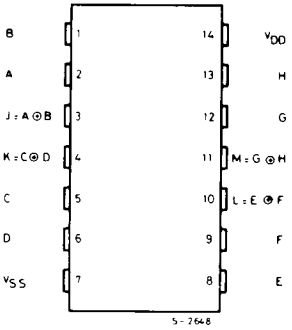
Ceramic flat package for HCC 4030 BK



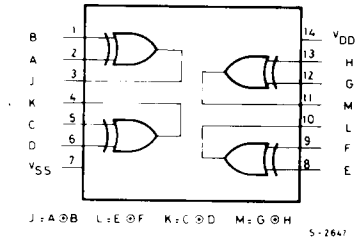
Plastic micropackage for HCF 4030 BM



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

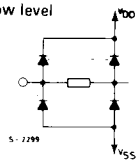


TRUTH TABLE

One of four identical gates

A	B	J
0	0	0
1	0	1
0	1	1
1	0	0

Where "1" = High level
"0" = Low level



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

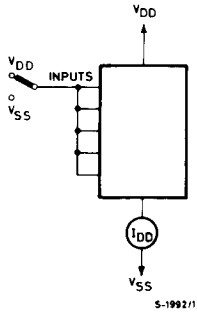
STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_i (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent current	HCC types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		HCF types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		± 1	
C_I	Input capacitance			Any input						5	7.5			pF

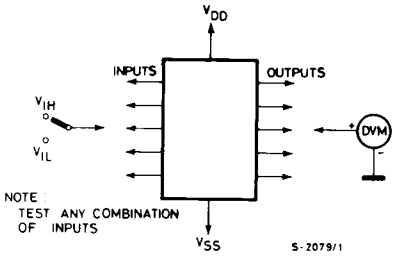
* T_{Low} = - 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

TEST CIRCUITS

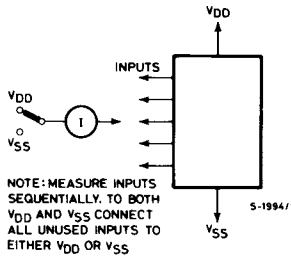
Quiescent device current



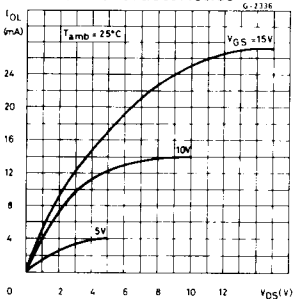
Input voltage



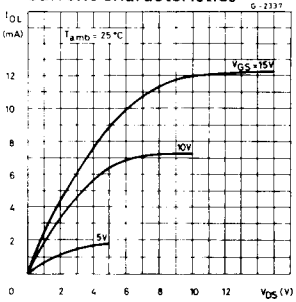
Input leakage current



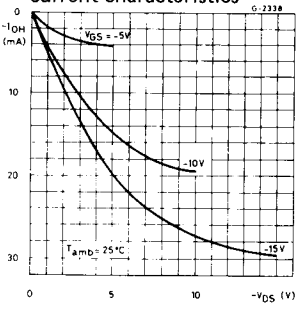
Typical output low (sink) current characteristics



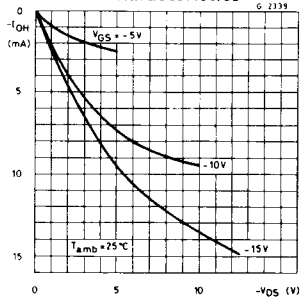
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics



Minimum output high (source) current characteristics

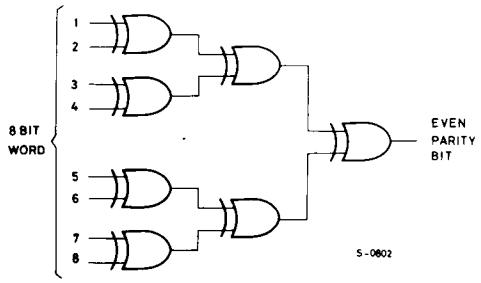


DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD}= 0.3%/°C values, all input rise and fall time = 20 ns)

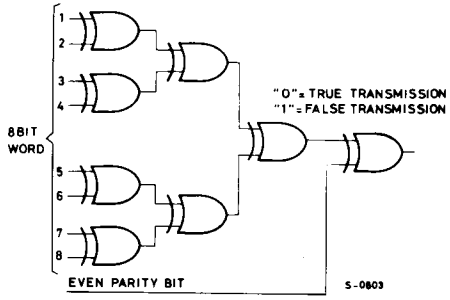
Parameter	Test conditions	Values			Unit
	V_{CC} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time	5		140	280	ns
	10		65	130	
	15		50	100	
t_{TLH}, t_{THL} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	

TYPICAL APPLICATIONS

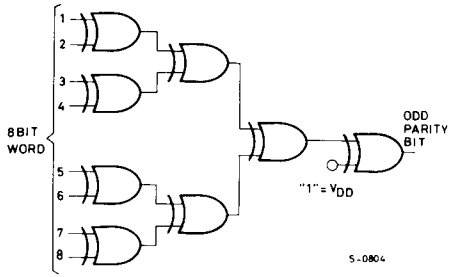
Even-parity-bit generator
(1-3/4 x **HCC/HCF 4030B**)



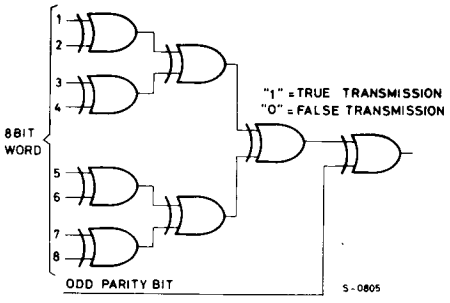
Even-parity checker
(2 x **HCC/HCF 4030B**)



Odd-parity-bit generator
(2 x **HCC/HCF 4030B**)

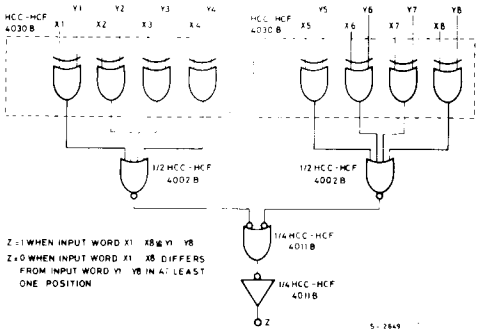


Odd-parity checker
(2 x **HCC/HCF 4030B**)



TYPICAL APPLICATIONS (continued)

8-bit comparator



8-bit two's complement adder-substractor

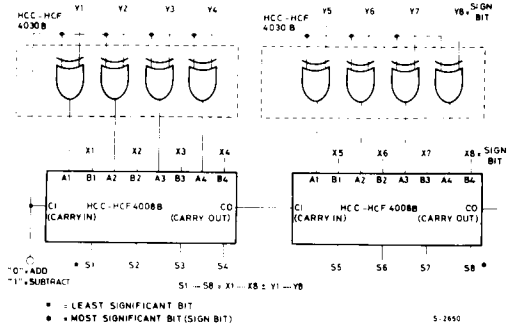


TABLE 1

Two's complement numbers and their equivalent decimal values

X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1			X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1		
0	0	0	0	0	0	0	0	=	0	1	1	1	1	1	1	1	1	=	-1
0	0	0	0	0	0	0	1	=	1	1	1	1	1	1	1	1	0	=	-2
0	0	0	0	0	0	1	0	=	2	1	1	1	1	1	1	0	1	=	-3
0	0	0	0	0	0	1	1	=	3	1	1	1	1	1	1	0	0	=	-4
										1	1	1	1	1	0	1	1	=	-5
0	1	1	1	1	1	1	0	=	126	1	0	0	0	0	0	0	1	=	-127
0	1	1	1	1	1	1	1	=	127	1	0	0	0	0	0	0	0	=	-128

The two's complement adder-substractor can add or substract any two of the numbers in TABLE 1. For example

a)

	2		SIGN								
+	=		BIT								
-5	X	0	0	0	0	0	0	1	0		2 +
—	Y	1	1	1	1	1	0	1	1		-5 +
	CI								0		
	S	0	1	1	1	1	1	1	0	1	= -3
	CO										

b)

			SIGN								
b)	- 2		BIT								
-	=	X	1	1	1	1	1	1	1	0	- 2 +
-5		Y	1	1	1	1	1	0	1	1	- 5
—		Y	0	0	0	0	0	1	0	0	+
		CI								1	
		S	1	0	0	0	0	0	1	1	= 3
		CO									