Signetics

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Status	Product Specification
FAST Products	

FAST 74F257, 74F257A
Data Selectors/Multiplexers

74F257 Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)
74F257A Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)

FEATURES

- **Multifunction capability**
- **Non-inverting data path**
- **3-state outputs**
- **See 'F258A for inverting version**

DESCRIPTION

The 74F257/74F257A has four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the common Select input is Low and the I_{1n} inputs are selected when the common Select input is High. Data appears at the outputs in true non-inverted form from the selected inputs. The 'F257/'F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the common Select input. Outputs are forced to a high impedance "off" state when the Output Enable ($\overline{OE}$) is High. All but one device must be in high impedance state to avoid currents that would exceed the maximum ratings if the outputs were tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices were tied together.

The 74F257A is the faster version of 74F257.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F257	4.3ns	12mA
74F257A	4.3ns	12mA

ORDERING INFORMATION

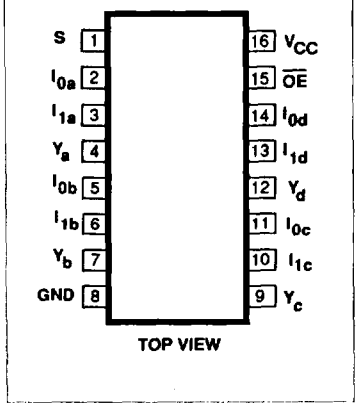
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F257N, N74F257AN
16-Pin Plastic SO	N74F257D, N74F257AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

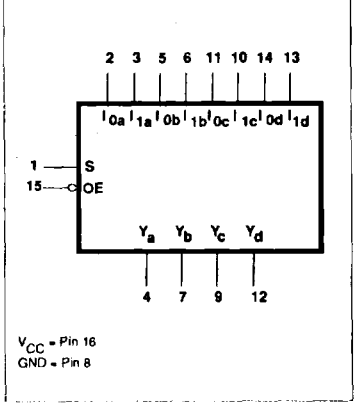
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20µA/0.6mA
S	Common Select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

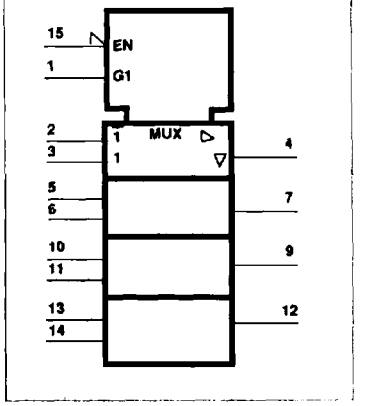
PIN CONFIGURATION



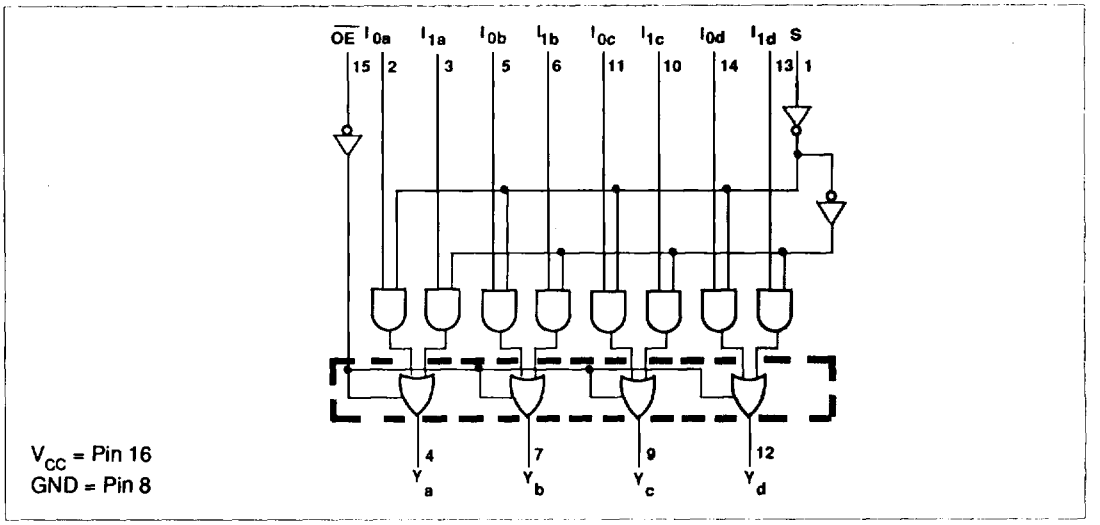
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state