MOTOROLA

Military 10521

4-Wide "OR-AND/OR-AND-INVERT" Gate

ELECTRICALLY TESTED PER:
5962-8857701

The 10521 is a basic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications.

- 150 mW Max/Pkg (No Load)
- t_{pd} = 2.3 ns typ
- t_r, t_f = 2.5 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8857701
3) 883: 10521/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

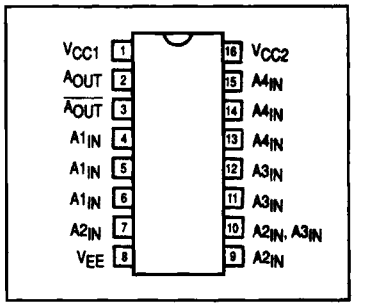
The letter "M" appears before the slash on LCC.

3

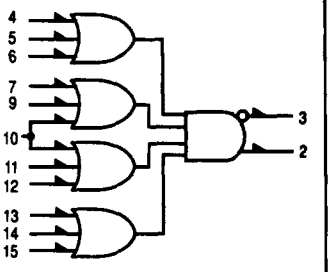
PIN ASSIGNMENTS

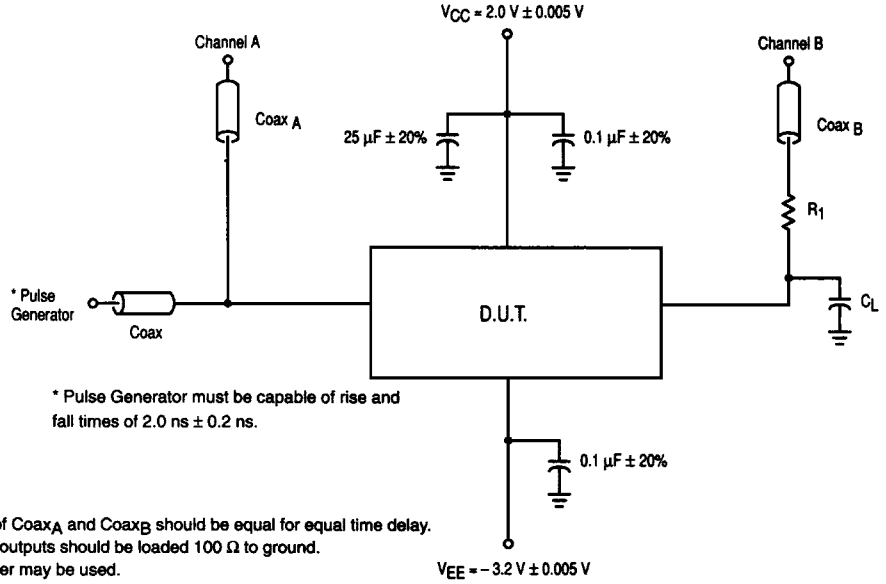
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	OPEN
$A1_{IN}$	6	10	8	OPEN
$A2_{IN}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$	9	13	12	OPEN
$A2_{IN}$, $A3_{IN}$	10	14	13	OPEN
$A3_{IN}$	11	15	14	OPEN
$A3_{IN}$	12	16	15	OPEN
$A4_{IN}$	13	1	17	OPEN
$A4_{IN}$	14	2	18	OPEN
$A4_{IN}$	15	3	19	OPEN
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns ± 0.2 ns measured at (20% - 80%).
5. $P_W \geq 20$ ns.
6. P_{RF} = 1.0 MHz.
7. R_1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
8. C_L = Jig and stray capacitance ≤ 5.0 pF.

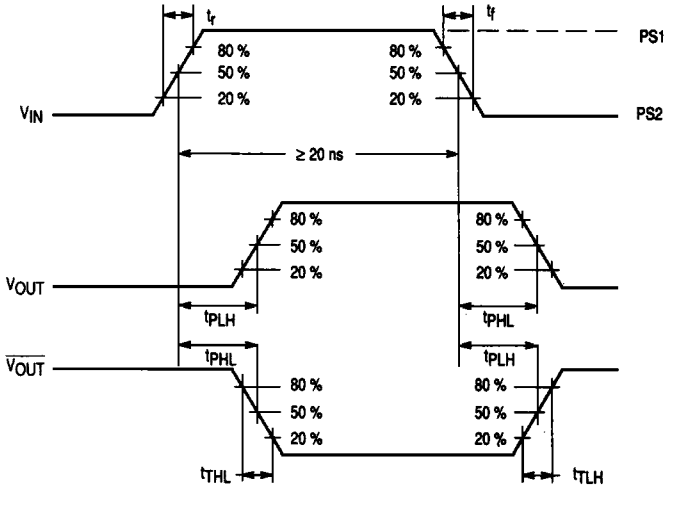


Figure 1. Switching Test Circuit and Waveforms

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QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4 - 7, 9 - 15	4 - 7, 9 - 15			8	1, 16	2, 3
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4 - 7, 9 - 13	4 - 7, 9 - 15			8	1, 16	2, 3
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	4, 7, 11, 13	4, 7, 11, 13	4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2, 3
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	4, 7, 11, 13		4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2, 3
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8	1, 16	8
I_{IH}	Input Current High		245		415		415	µA	4 - 7, 9, 11 - 15				8	1, 16	4 - 7, 9, 11 - 15
I_{IH1}	Input Current High		310		525		525	µA	10				8	1, 16	10
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 15			8	1, 16	4 - 7, 9 - 15

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Test Temperature	Test Voltage Values (Volts)							
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T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.1	4.0	0.9	4.4	1.0	4.5	ns	5, 9, 10 12, 15	3	1, 16	8	5, 9, 12, 15	2, 3
t_{THL}	Fall Time	1.1	4.0	0.9	4.4	1.0	4.5	ns	5, 9, 10 12, 15	3	1, 16	8	5, 9, 12, 15	2, 3
t_{PHL}	Propagation Delay High to Low	1.4	3.5	1.1	3.9	1.2	3.8	ns	5, 9, 10 12, 15	3	1, 16	8	5, 9, 12, 15	2, 3
t_{PLH}	Propagation Delay Low to High	1.4	3.5	1.1	3.9	1.2	3.8	ns	5, 9, 10 12, 15	3	1, 16	8	5, 9, 12, 15	2, 3