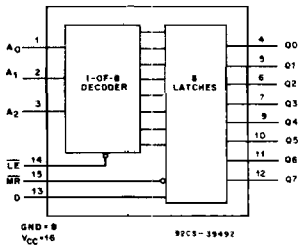
File Number **1727**

CD54/74HC259
CD54/74HCT259

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Bit Addressable Latch

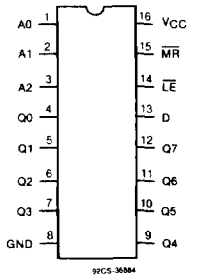
Type Features:
- *Buffered inputs and outputs*
- *Four operating modes*
- *Typical propagation delay of 15 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = +25° C*

The RCA-CD54/74HC259 and CD54/74HCT259 Addressable Latch features the low-power consumption associated with CMOS circuitry and has speeds comparable to low-power Schottky.

This latch has three active modes and one reset mode. When both the Latch Enable ($\overline{LE}$) and Master Reset ($\overline{MR}$) inputs are low (8-line Demultiplexer mode) the output of the addressed latch follows the Data input and all other outputs are forced low. When both $\overline{MR}$ and $\overline{LE}$ are high (Memory Mode), all outputs are isolated from the Data input, i.e., all latches hold the last data presented before the $\overline{LE}$ transition from low to high. A condition of $\overline{LE}$ low and $\overline{MR}$ high (Addressable Latch mode) allows the addressed latch's output to follow the data input; all other latches are unaffected. The Reset mode (all outputs low) results when $\overline{LE}$ is high and $\overline{MR}$ is low.

The CD54HC259 and CD54HCT259 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC259 and CD74HCT259 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
- *Bus driver outputs - 15 LSTTL loads*
  Wide operating temperature range:
  CD74HC/HCT: -40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC259
CD54/74HCT259

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = −55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = −40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... −55 to +125° C
PACKAGE TYPE E, M ..... −40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... −65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... 265° C
Unit inserted into a PC board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only ..... 300° C

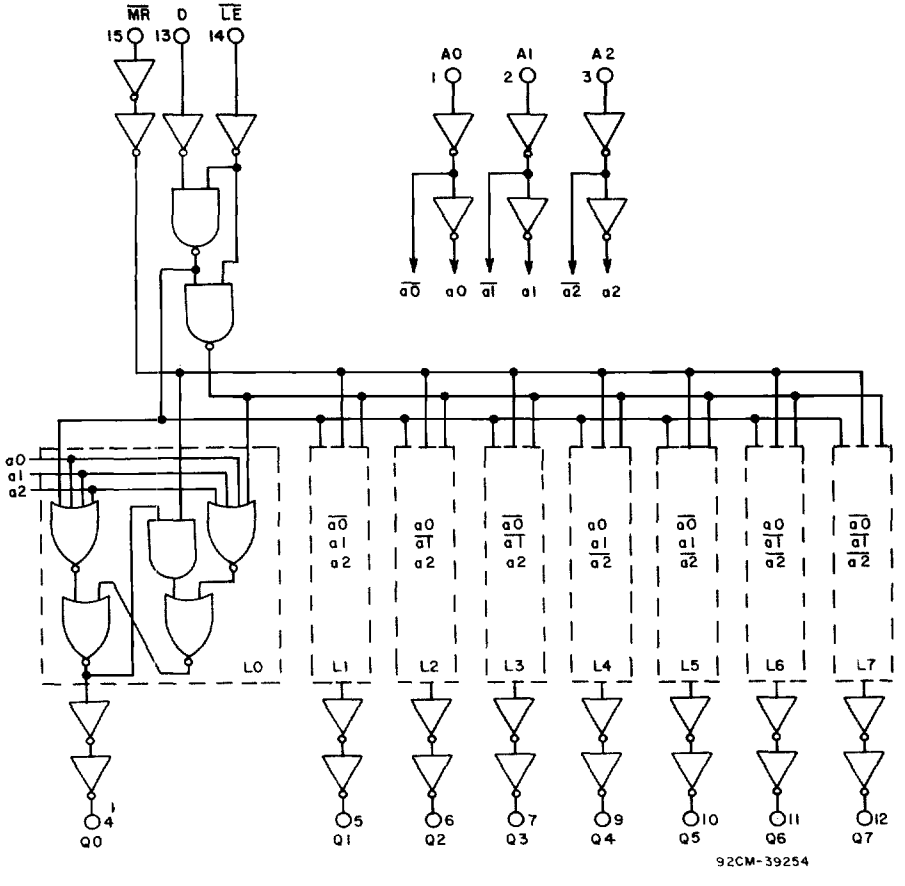


Fig. 1 - Logic diagram.

CD54/74HC259
CD54/74HCT259

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{CC}: *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE

INPUTS		Output of Address Latch	Each Other Output	Function
$\overline{MR}$	$\overline{LE}$			
H	L	D	Q_{io}	Addressable Latch
H	H	Q_{io}	Q_{io}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Reset

H = High level L = Low level

D = The level at the data input

Q_{io} = The level of Q_i (i = 0, 1...7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

Select Inputs			Latch Addressed
A2	A1	A0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

CD54/74HC259
CD54/74HCT259

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC259, CD54HC259										CD74HCT259, CD54HCT259										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5 to 5.5									
			4.5	3.15	—	—	3.15	—	3.15	—	—		2	—	—	2	—	2	—	V	
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5 to 5.5									
			4.5	—	—	1.35	—	1.35	—	1.35	—		—	—	0.8	—	0.8	—	0.8	V	
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V	
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V	
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V	
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V	
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA	
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
A0-A2, $\overline{LE}$	1.5
D	1.2
$\overline{MR}$	0.75

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25° C.

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SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay D to Q	t_{PLH} t_{PHL}	15	15	16	ns
$\overline{LE}$ to Q			14	16	ns
A to Q			15	17	ns
$\overline{MR}$ to Q		15	13	16	ns
Power Dissipation Capacitance*	C_{PD}	—	21	22	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD}V_{CC}^2f_i + \Sigma\ C_LV_{CC}^2f_o$ where f_i = input frequency, f_o = output frequency,

C_L = output load capacitance, V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min	HC Max	HCT Min	HCT Max	-40°C to +85°C 74HC Min	74HC Max	74HCT Min	74HCT Max	-55°C to +125°C 54HC Min	54HC Max	54HCT Min	54HCT Max	UNITS
Pulse Width $\overline{LE}$	t_{WL}	2	70	—	—	—	90	—	—	—	105	—	—	—	ns
		4.5	14	—	18	—	18	—	23	—	21	—	27	—	
		6	12	—	—	—	15	—	—	—	18	—	—	—	
$\overline{MR}$	t_{WL}	2	70	—	—	—	90	—	—	—	105	—	—	—	ns
		4.5	14	—	18	—	18	—	23	—	21	—	27	—	
		6	12	—	—	—	15	—	—	—	18	—	—	—	
Set-up Time D to $\overline{LE}$	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	17	—	20	—	21	—	24	—	26	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
A to $\overline{LE}$	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	17	—	20	—	21	—	24	—	26	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time D to $\overline{LE}$	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
A to $\overline{LE}$	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	

CD54/74HC259
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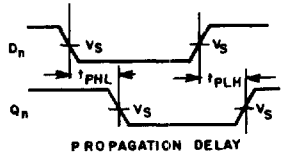
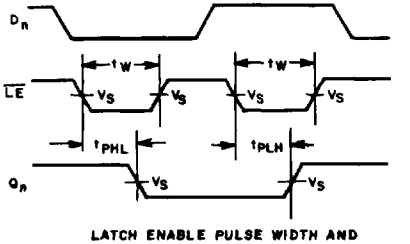
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

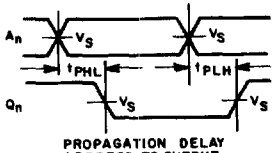
CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
	V_{CC} V	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation t_{PLH}	2	—	185	—	—	—	230	—	—	—	280	—	—	
Delay t_{PHL}	4.5	—	37	—	39	—	46	—	49	—	56	—	59	ns
D to Q	6	—	31	—	—	—	39	—	—	—	48	—	—	
	2	—	170	—	—	—	215	—	—	—	255	—	—	
$\overline{LE}$ to Q	4.5	—	34	—	38	—	43	—	48	—	51	—	57	ns
	6	—	29	—	—	—	37	—	—	—	43	—	—	
	2	—	185	—	—	—	230	—	—	—	280	—	—	
A to Q	4.5	—	37	—	41	—	46	—	51	—	56	—	61	ns
	6	—	31	—	—	—	39	—	—	—	48	—	—	
	2	—	155	—	—	—	195	—	—	—	235	—	—	
$\overline{MR}$ to Q	4.5	—	31	—	39	—	39	—	49	—	47	—	59	ns
	6	—	26	—	—	—	33	—	—	—	40	—	—	
Output t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Transition t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Time	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input C_I Capacitance		—	10	—	10	—	10	—	10	—	10	—	10	pF



PROPAGATION DELAY
DATA TO OUTPUT



LATCH ENABLE PULSE WIDTH AND
LATCH ENABLE TO OUTPUT PROPAGATION DELAY



PROPAGATION DELAY
ADDRESS TO OUTPUT

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

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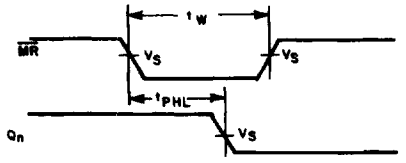
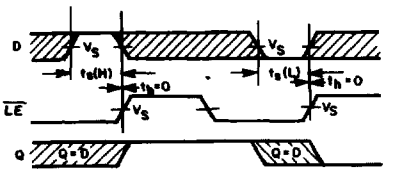
Fig. 2 - AC Waveforms.

CD54/74HC259
CD54/74HCT259

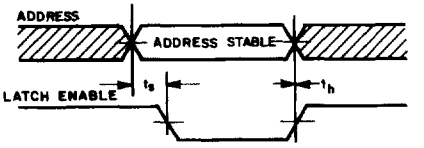


$\overline{MR}$ TO OUTPUT DELAY AND $\overline{MR}$ PULSE WIDTH

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V



DATA SETUP AND HOLD TIMES



ADDRESS SETUP AND HOLD TIMES

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Fig. 3 - AC Waveforms.