

GD54/74LS73A

DUAL NEGATIVE EDGE-TRIGGERED MASTER-SALVE J-K FLIP-FLOPS WITH CLEAR AND COMPLEMENTARY OUTPUTS

Description

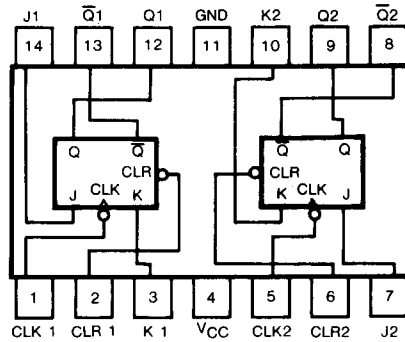
This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs is allowed to change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

Function Table(each gate)

Inputs				Outputs	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	Toggle
H	H	X	X	Q_0	\bar{Q}_0

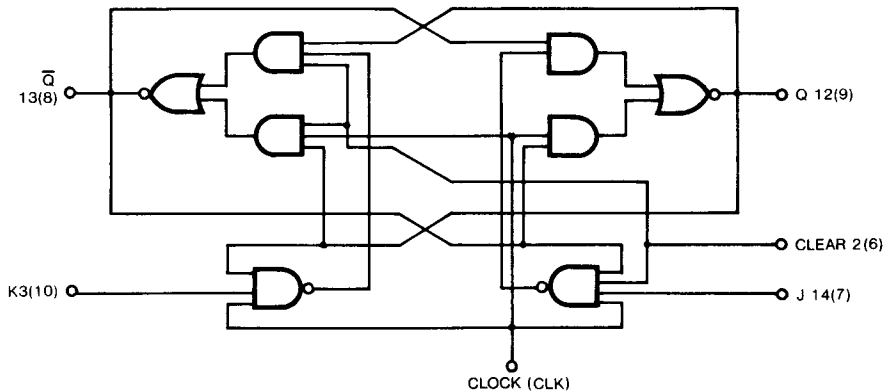
X = Either Low or High Logic Level
 ↓ = Negative going edge of pulse
 Q_0 = The output logic level before the indicated input conditions were established.
 Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package

Logic Diagram (Each Flip-Flop)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS -55°C to 125°C
- 74LS 0°C to 70°C
- Storage temperature range -65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output Current		-400			μA
I_{OL}	Low-level output current	54	4			mA
		74	8			
f_{clock}	Clock frequency		0	30		MHz
t_w	Pluse width	Clock high	20			ns
		Preset low	25			
		Clear low	25			
t_{su}	Clear inactive-state setup time		20↓			ns
t_h	Data hold time		0↓			ns
T_A	Operating free-air temperature	54	-55		125	$^{\circ}\text{C}$
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT	
V_{IH}	High-level input voltage		2				V	
V_{IL}	Low-level input voltage		54	0.7		V		
			74	0.8				
V_{IK}	Input clamp voltage		$V_{CC}=\text{Min}, I_I=-18\text{ mA}$			-1.5	V	
V_{OH}	High-level output voltage		$V_{CC}=\text{Min}, V_{IL}=\text{Max}$	54	2.5	3.4	V	
			$I_{OH}=\text{Max}, V_{IH}=\text{Min}$	74	2.7	3.4		
V_{OL}	Low-level output voltage		$V_{CC}=\text{Min}, V_{IL}=\text{Max}, V_{IH}=\text{Min}$	$I_{OL}=4\text{mA}$	54,74	0.25	0.4	V
			$I_{OL}=8\text{mA}$	74	0.35	0.5		
I_I	Input current at maximum input voltage	J,K	$V_{CC}=5.25\text{V}, V_I=7\text{V}$			0.1		mA
		Clear				0.3		
		Clock				0.4		
I_{IH}	High-level input current	J,K	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$			20		μA
		Clear				60		
		Clock				80		
I_{IL}	Low-level input current	J,K	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$			-0.4		mA
		Clear				-0.8		
		Clock				-0.8		
I_{OS}	Short-circuit output current		$V_{CC}=\text{Max}$ (Note 2)			-20	-100	mA
I_{CC}	Supply current		$V_{CC}=\text{Max}$ (Note 3)			4	6	mA

Note 1: All typical values are at $V_{CC}=5\text{V}, T_A=25^{\circ}\text{C}$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

SYMBOL*	FROM(INPUT)	TO(OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			$C_L = 15 \text{ pF}$ $R_L = 2K\Omega$	30	45		MHz
t_{PLH}	Clear, Clock	Q or \bar{Q}			15	20	ns
t_{PHL}					15	20	

* f_{max} = maximum clock frequency

* t_{PLH} = propagation delay time, low-to-high-level output.

* t_{PHL} = propagation delay time, high-to-low-level output.

#For load circuit and voltage wave forms, see page 3-11.

Application Example

HIGH-SPEED 1/3 DIVIDER

