



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL TRANSPARENT LATCH DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2373
IDT54/74FBT2373A

FEATURES:

- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static VOH for improved noise immunity and reduced power dissipation.
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

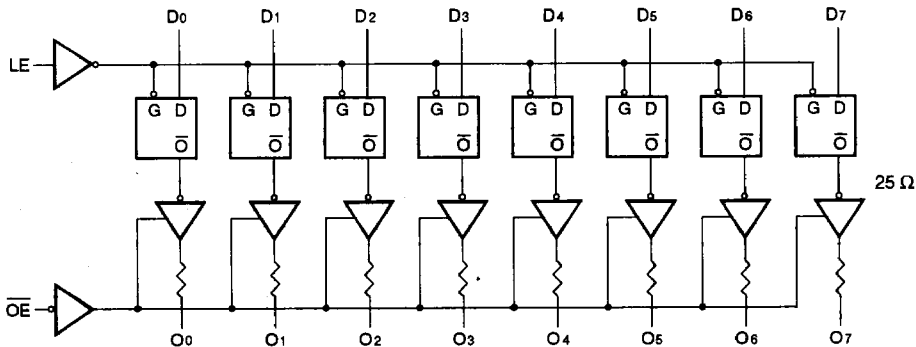
DESCRIPTION:

The FBT series of BiCMOS Latch Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2373 series are 3-state, 8-bit latches where each output is terminated with a 25Ω series resistor. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high-impedance state.

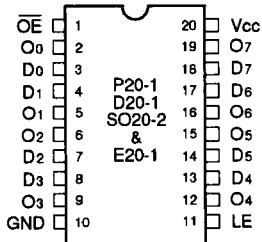
The FBT series of bus interface devices are ideal for driving large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. The output buffers are designed to guarantee a static VOH of 2.7V. This higher output level in the high state will result in a significant reduction in overall system power dissipation and in improved noise immunity when driving DRAMS and SRAMS.

FUNCTIONAL BLOCK DIAGRAM

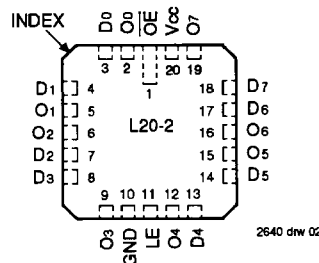


2640 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

2640 drw 02

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1992

PIN DESCRIPTION

Pin Names	Description
D ₀ - D ₇	Data Inputs
LE	Latch Enables Input (Active HIGH)
\overline{OE}	Output Enables Input (Active LOW)
O ₀ - O ₇	3-State Latch Outputs

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FUNCTION TABLE⁽¹⁾

Inputs			Outputs
D _n	LE	\overline{OE}	O _n
H	H	L	H
L	H	L	L
X	L	L	NC
X	X	H	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Type	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

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- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGEFollowing Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$ Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 10\%$; Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_i = 2.7V$		—	—	10	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_i = 0.5V$		—	—	-10	μA
I_{OZH}	High Impedance	$V_{CC} = \text{Max.}$	$V_o = 2.7V$	—	—	50	μA
I_{OZL}	Output Current		$V_o = 0.5V$	—	—	-50	μA
I_i	Input HIGH Current	$V_{CC} = \text{Max.}, V_{CC} (\text{Max.})$		—	—	100	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	$V_{CC} = \text{Min.}, V_o = 2.25V$		-35	—	—	mA
I_{ODL}	Output Drive Current	$V_{CC} = \text{Min.}, V_o = 2.25V$		50	—	—	mA
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = GND^{(3)}$		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A^{(4)}$	V_{HC}	V_{CC}	—	V
			$I_{OH} = -1mA$	2.7	3.8	—	
			$I_{OH} = -8mA$	2.4	3.3	—	
			$I_{OH} = -12mA$	2.0	3.2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A^{(4)}$	—	GND	V_{LC}	V
			$I_{OL} = 1mA$	—	0.1	0.5	
			$I_{OL} = 12mA$	—	0.35	0.8	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = GND \text{ or } V_{CC}$		—	0.2	1.5	mA

NOTES:

2640 tbi 03

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This condition is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	2.0	mA	
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $\overline{OE} = \text{GND}$, $LE = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.3	0.4	mA/ MHz
I_C	Total Power Supply Current ⁽⁵⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_i = 10\text{MHz}$, 50% Duty Cycle $\overline{OE} = \text{GND}$, $LE = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.2	5.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	3.5	6.5	
		$V_{CC} = \text{Max.}$, Outputs Open $f_i = 2.5\text{MHz}$, 50% Duty Cycle $\overline{OE} = \text{GND}$, $LE = V_{CC}$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	6.2	9.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.2	17.5 ⁽⁵⁾	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT5474FBT2373				IDT5474FBT2373A				Unit
			Com'l.		MIL.		Com'l.		MIL.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		2.0	9.3	2.0	10.1	2.0	8.5	2.0	9.8	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.0	1.5	12.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.4	1.5	8.1	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_n to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:

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- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.