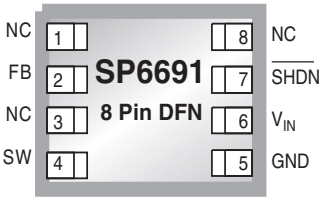
SP6691

Micro Power Boost Regulator Series White LED Driver

FEATURES

- Drives up to 6 LEDs @ 25mA
- Drives up to 8 LEDs @ 20mA
- High Output Voltage: Up to 30V
- Optimized for Single Supply, 2.7V - 4.2V Applications
- Operates Down to 1V
- High Efficiency: Greater Than 75%
- Low Quiescent Current: 20μA
- Ultra Low Shutdown Current: 10nA
- Single Battery Cell Operation
- Programmable Output Voltage
- 1Ω switch (350mV at 350mA)
- Lead Free, RoHS Compliant Packages: 8 Pin DFN, 5 Pin TSOT or 5 Pin SOT23



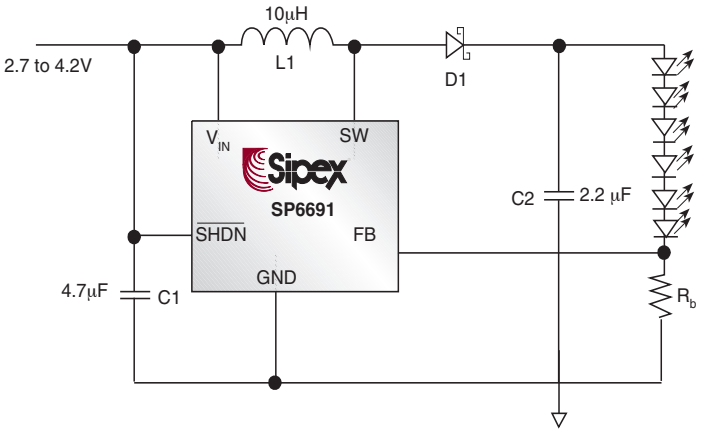
APPLICATIONS

- White LED Driver
- High Voltage Bias
- Digital Cameras
- Cell Phone
- Battery Backup
- Handheld Computers

DESCRIPTION

The SP6691 is a micro power boost regulator that is specifically designed for powering series configuration white LED. The part utilizes fixed off time architecture and consumes only 10nA quiescent current in shutdown. Low voltage operation, down to 1V, fully utilizes maximal battery life. The SP6691 is offered in a 8 Pin DFN, 5-pin SOT-23 or 5 Pin TSOT package and enables the construction of a complete regulator occupying < 0.2 in^2 board space.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

V_{IN} 15V
SW Voltage ..... -0.4 to 30V
FB Voltage 2.5V
All other pins ..... -0.3 to V_{IN} + 0.3V
Current into FB ..... ±1mA
T_J Max ..... 125°C
Operating Temperature Range ..... -40°C to 85°C
Peak Output Current < 10us SW 500mA

Storage Temperature ..... -65°C to +150°C
Power Dissipation. 200mW
ESD Rating ..... 2kV HBM

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C, V_{IN} = 3.3, V_{SHDN} = V_{IN}, ♦ denotes the specifications which apply over the full operating temperature range, unless otherwise specified.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	♦	CONDITIONS
Input Voltage	V_{IN}	1.0		13.5	V		
Supply Current	I_Q		20	30	µA	♦	No Switching
			0.01	1	µA	♦	$\overline{SHDN}$ = 0V (off)
Reference Voltage	V_{FB}	1.17	1.22	1.27	V	♦	
FB Hysteresis	HYST		8		mV		
V_{FB} Input Bias Current	I_{FB}		15	80	nA	♦	V_{FB} = 1.22V
Line Regulation	$\Delta V_o/\Delta V_I$		0.1	0.3	%/V		1.2 ≤ V_{IN} ≤ 13.5V
Switch Off Time	T_{OFF}		250		nS		
Switch Saturation Voltage	V_{CESAT}		170	450	mV	♦	I_{SW} = 325mA
Switch Current Limit	I_{LIM}	325	450	575	mA	♦	
$\overline{SHDN}$ Bias Current	$I_{\overline{SHDN}}$		5	12	µA	♦	$V_{\overline{SHDN}}$ = 3.3V
$\overline{SHDN}$ High Threshold (on)	V_{IH}	0.9			V		
$\overline{SHDN}$ Low Threshold (off)	V_{IL}			0.25	V		
Switch Leakage Current	I_{SWLK}		0.01	5	µA	♦	Switch Off, V_{SW} = 5V

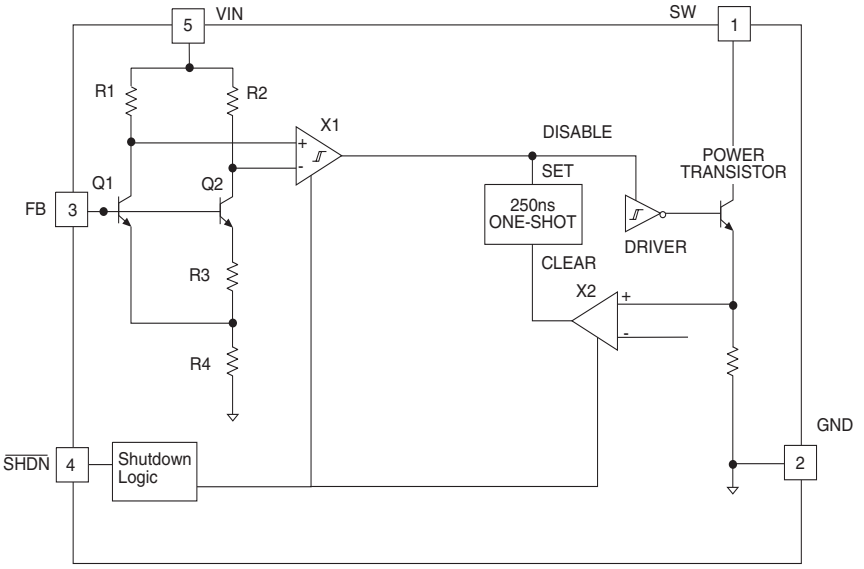
PIN DESCRIPTION

PIN NUMBER	PIN NAME	8 PIN DFN DESCRIPTION
1	NC	No connect.
2	FB	Feedback.
3	NC	No connect.
3	SW	Switch input to the internal power switch
5	GND	Ground
6	V_{IN}	Input Voltage. Bypass this pin with a capacitor as close to the device as possible.
7	$\overline{SHDN}$	Shutdown. Pull high (on) to enable. Pull low (off) for shutdown.
8	NC	No connect.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	DESCRIPTION
1	SW	Switch input to the internal power switch.
2	GND	Ground
3	FB	Feedback
4	$\overline{SHDN}$	Shutdown. Pull high (on) to enable. Pull low (off) for shutdown.
5	V_{IN}	Input Voltage. Bypass this pin with a capacitor as close to the device as possible.

FUNCTIONAL DIAGRAM



THEORY OF OPERATION

Operation can be best understood by referring to the functional diagram above and the typical application circuit in the front page. Q1 and Q2 along with R3 and R4 form a band gap reference. The input to this circuit completes a feedback path from the high voltage output through a voltage divider, and is used as the regulation control input. When the voltage at the FB pin is slightly above 1.22V, comparator X1 disables most of the internal circuitry. Current is then provided by capacitor C2, which slowly discharges until the voltage at the FB pin drops below the lower hysteresis point of X1, about 6mV. X1 then enables the internal circuitry, turns on chip power, and the current in the inductor begins to ramp up. When the current through the driver transistor reaches about 450mA, comparator X2 clears the latch, which turns off the driver transistor for a preset 250nS. At the instant of shutoff, inductor current is diverted to the output through diode D1. During this 250nS time limit, inductor current decreases while its energy charges C2.

At the end of the 250ns time period, driver transistor is again allowed to turn on which ramps the current back up to the 450mA level. Comparator X2 clears the latch, it's output turns off the driver transistor, and this allows delivery of L1's stored kinetic energy to C2. This switching action continues until the output capacitor voltage is charged to the point where FB is at band gap (1.22V). When this condition is reached, X1 turns off the internal circuitry and the cycle repeats.

PERFORMANCE CHARACTERISTICS

Refer to the typical application circuit, T_{AMB} = 25°C, unless otherwise specified.

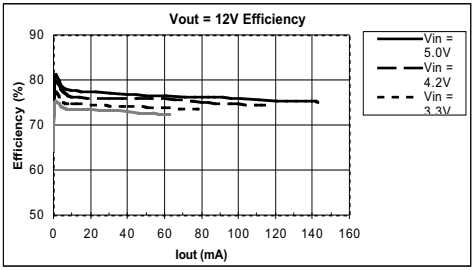


Figure 1. 12V Output Efficiency

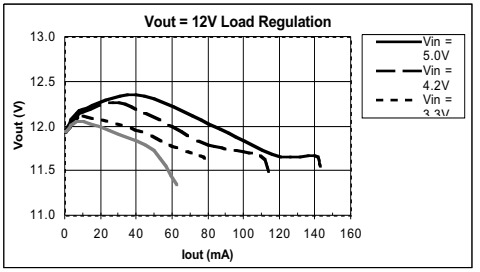


Figure 2. 12V Output Load Regulation

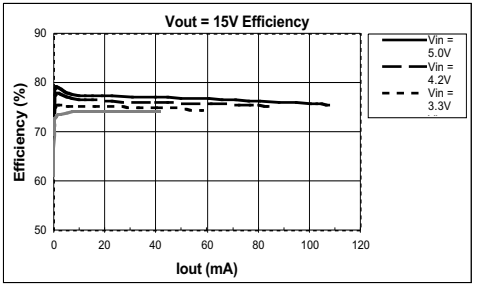


Figure 3. 15V Output Efficiency

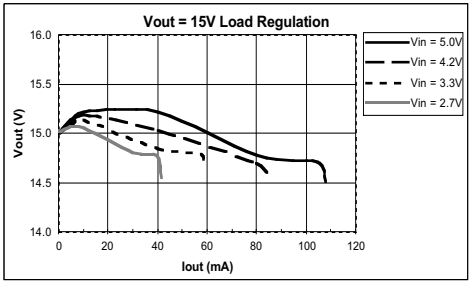


Figure 4. 15V Output Load Regulation

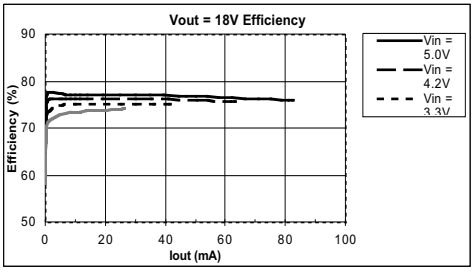


Figure 5. 18V Output Efficiency

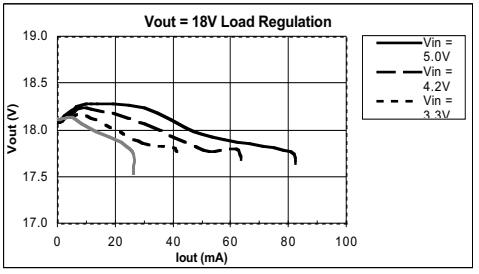


Figure 6. 18V Output Load Regulation

Refer to the typical application circuit, T_{AMB} = 25°C, unless otherwise specified.

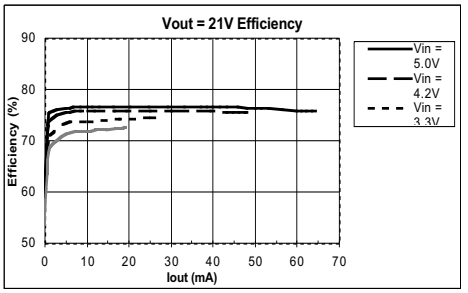


Figure 7. 21V Output Efficiency

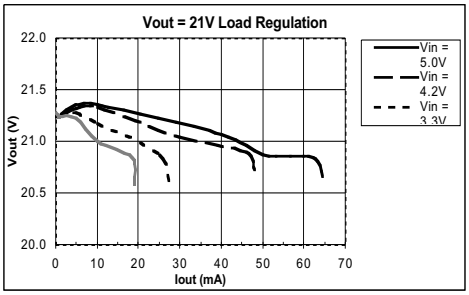


Figure 8. 21V Output Load Regulation

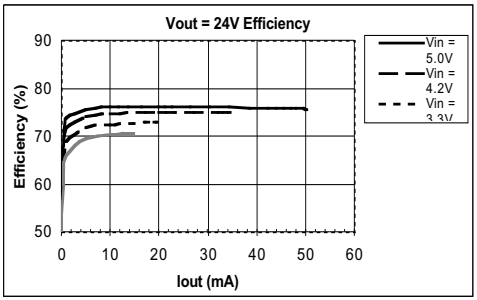


Figure 9. 24V Output Efficiency

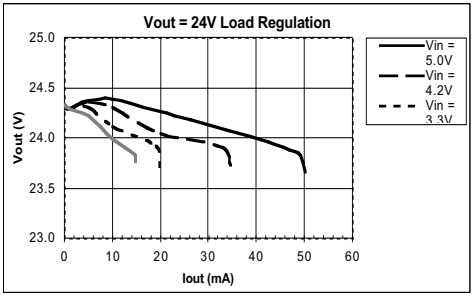


Figure 10. 24V Output Load Regulation

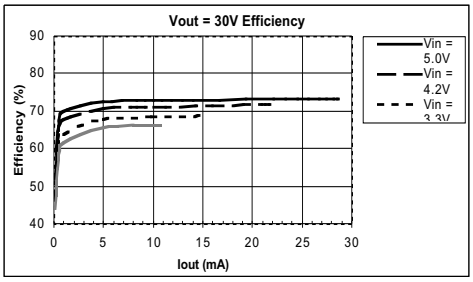


Figure 11. 30V Output Efficiency

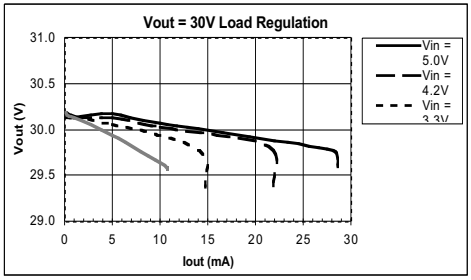


Figure 12. 30V Output Load Regulation

PERFORMANCE CHARACTERISTICS

Refer to the typical application circuit, T_{AMB} = 25°C, unless otherwise specified.

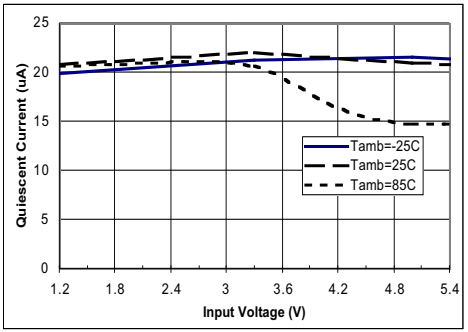


Figure 13. Quiescent Current I_Q vs. V_{IN}

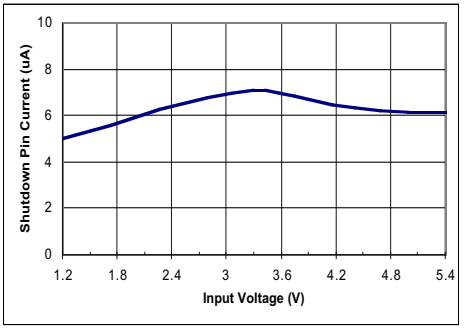


Figure 14. Shutdown Pin Current vs. V_{IN}

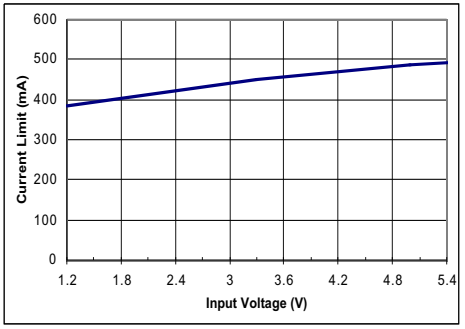


Figure 15. I_{PK} Current Limit vs. V_{IN}

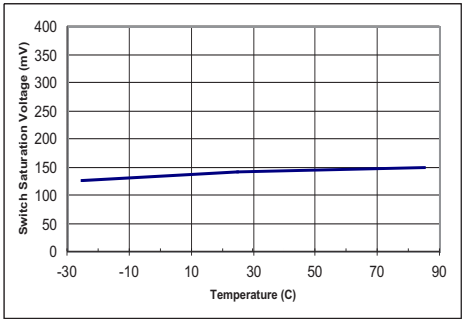


Figure 16. Switch Saturation Voltage V_{CESAT} vs. Temperature (I_{SW} = 450mA)

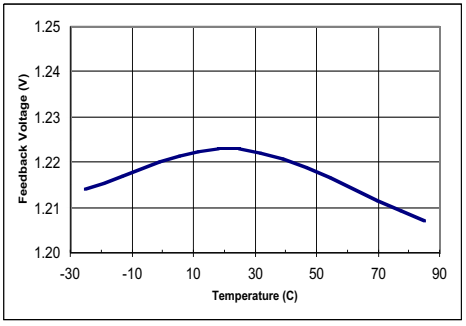


Figure 17. Feedback Voltage vs. Temperature

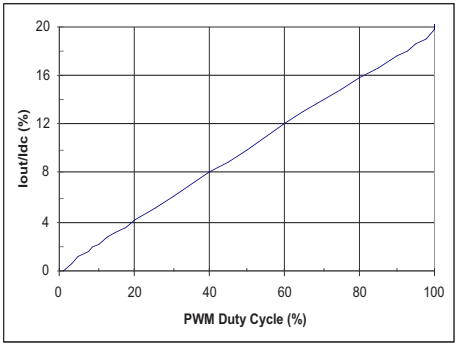


Figure 18. Average I_O vs. SHDN Duty Cycle (V_{IN}=3.3V, Standard 4x20mA WLED Evaluation Board, PWM Frequency 100Hz

Refer to the typical application circuit, T_{AMB} = 25°C, unless otherwise specified.

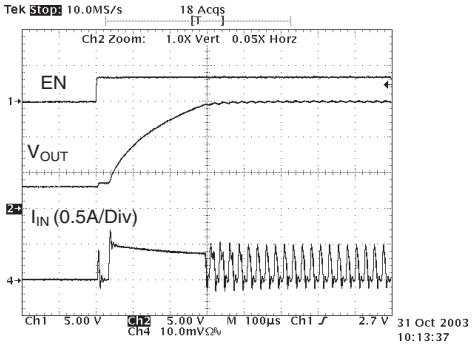


Figure 19. Startup Waveform (V_{IN}=3.3V, V_{OUT}=15V, I_{OUT}=20mA)

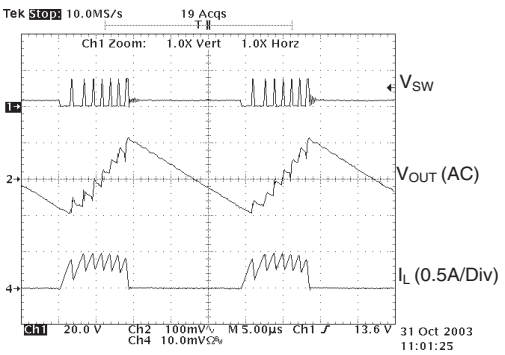


Figure 20. Typical Switching Waveforms (V_{IN}=3V, V_{OUT}=15V, I_{OUT}=20mA)

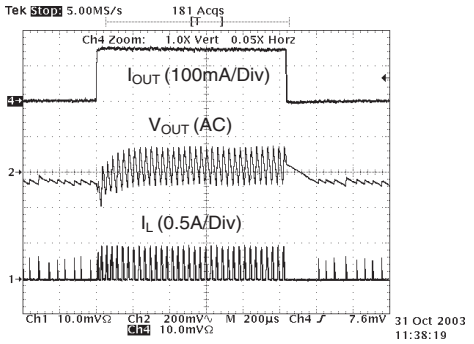


Figure 21. Load Step Transient (V_{IN}=3V, V_{OUT}=21V, 1~15mA Load Step

Inductor Selection

For SP6691, the internal switch will be turned off only after the inductor current reaches the typical dc current limit (I_{LIM}=450mA). However, there is typically propagation delay of 200nS between the time when the current limit is reached and when the switch is actually turned off. During this 200nS delay, the peak inductor current will increase, exceeding the current limit by a small amount. The peak inductor current can be estimated by:

$$I_{PK} = I_{LIM} + \frac{V_{IN(MAX)}}{L} \bullet 200nS$$

The larger the input voltage and the lower the inductor value, the greater the peak current.

In selecting an inductor, the saturation current specified for the inductor needs to be greater than the SP6691 peak current to avoid saturating the inductor, which would result in a loss in efficiency and could damage the inductor.

Choosing an inductor with low DCR decreases power losses and increase efficiency.

Refer to Table 1 for some suggested low ESR inductors.

Table 1. Suggested Low ESR inductor

MANUF.	PART NUMBER	DCR (Ω)	Current Rating (mA)
MURATA 770-436-1300	LQH32CN100K11 (10μH)	0.3	450
TDK 847-803-6100	NLC453232T-100K (10μH)	0.55	500

Diode Selection

A schottky diode with a low forward drop and fast switching speed is ideally used here to achieve high efficiency. In selecting a Schottky diode, the current rating of the schottky diode should be larger than the peak inductor current. Moreover, the reverse breakdown voltage of the schottky diode should be larger than the output voltage.

Capacitor Selection

Ceramic capacitors are recommended for their inherently low ESR, which will help produce low peak to peak output ripple, and reduce high frequency spikes.

For the typical application, 4.7μF input capacitor and 2.2μF output capacitor are sufficient. The input and output ripple could be further reduced by increasing the value of the input and output capacitors. Place all the capacitors as close to the SP6691 as possible for layout. For use as a voltage source, to reduce the output ripple, a small feedforward (47pF) across the top feedback resistor can be used to provide sufficient overdrive for the error comparator, thus reduce the output ripple.

Refer to Table 2 for some suggested low ESR capacitors.

Table 2. Suggested Low ESR Capacitor

MANUF.	PART NUMBER	CAP /VOLTAGE	SIZE /TYPE
MURATA 770-436-1300	GRM32RR71E 225KC01B	2.2μF /25V	1210 /X5R
MURATA 770-436-1300	GRM31CR61A 475KA01B	4.7μF /10V	1206 /X5R
TDK 847-803-6100	C3225X7R1E 225M	2.2μF /25V	1210 /X7R
TDK 847-803-6100	C3216X5R1A 475K	4.7μF /10V	1206 /X5R

LED Current Program

In the white LEDs application, the SP6691 is generally programmed as a current source. The bias resistor R_b, as shown in the typical application circuit is used to set the operating current of the white LED using the equation:

$$R_b = \frac{V_{FB}}{I_F}$$

where V_{FB} is the feedback pin voltage (1.22V), I_F is the operating current of the White LEDs. In order to achieve accurate LED current, 1%

precision resistors are recommended. Table 3 below shows the R_b selection for different white LED currents. For example, to set the operating current to be 20mA, R_b is selected as 60.4 Ω, as shown in the schematic.

Table 3. Bias Resistor Selection

I_F (mA)	R_b (Ω)
5	243
10	121
12	102
15	80.6
20	60.4

Output Voltage Program

The SP6691 can be programmed as either a voltage source or a current source. To program the SP6691 as voltage source, the SP6691 requires 2 feedback resistors R_1 & R_2 to control the output voltage. As shown in Figure 22.

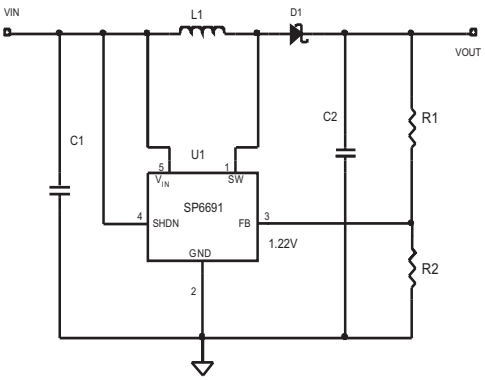


Figure 22. Using SP6691 as Voltage Source

The formula and table for the resistor selection are shown below:

$$R_1 = \left(\frac{V_{OUT}}{1.22} - 1 \right) \bullet R_2$$

Table 4. Divider Resistor Selection

V_{OUT} (V)	R_1 (Ω)	R_2 (Ω)
12	1M	113K
15	1M	88.7K
18	1M	73.2K
21	1M	61.9K
30	1M	42.2K

Brightness Control

Dimming control can be achieved by applying a PWM control signal to the $\overline{SHDN}$ pin. The brightness of the white LEDs is controlled by increasing and decreasing the duty cycle of the PWM signal. A 0% duty cycle corresponds to zero LED current and a 100% duty cycle corresponds to full load current. While the operating frequency range of the PWM control is from 60Hz to 700Hz, the recommended maximum brightness frequency range of the PWM signal is from 60Hz to 200Hz. A repetition rate of at least 60Hz is required to prevent flicker. The magnitude of the PWM signal should be higher than the minimum $\overline{SHDN}$ voltage high.

Open Circuit Protection

When any white LED inside the white LED module fails or the LED module is disconnected from the circuit, the output and the feedback control will be open, thus resulting in a high output voltage, which may cause the SW pin voltage to exceed it maximum rating. In this case, a zener diode can be used at the output to limit the voltage on the SW pin and protect the part. The zener voltage should be larger than the maximum forward voltage of the White LED module.

Layout Consideration

Both the input capacitor and the output capacitor should be placed as close as possible to the IC.

This can reduce the copper trace resistance which directly effects the input and output ripples. The feedback resistor network should be kept close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the feedback resistor network should connect directly to the GND pin or to an analog ground plane that is tied directly to the GND pin. The inductor and the schottky diode should be placed as close as possible to the switch pin to minimize the noise coupling to the other circuits, especially the feedback network.

Power Efficiency

For the typical application circuit, the output efficiency of the circuit is expressed by

$$\eta = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet I_{IN}}$$

Where V_{IN} , I_{IN}, V_{OUT}, I_{OUT} are the input and output voltage and current respectively.

While the white LED efficiency is expressed by

$$\eta = \frac{(V_{OUT} - 1.22) \bullet I_{OUT}}{V_{IN} \bullet I_{IN}}$$

This equation indicates that the white LED efficiency will be much smaller than the output efficiency of the circuit when V_{OUT} is not very large, compared to the feedback voltage (1.22V).

The other power is consumed by the bias resistor. To reduce this power loss, two circuits can be used, as shown in Figure 23 and Figure 24. In Figure 23, a general-purpose diode (for example, 1N4148) is used to bring the voltage across the bias resistor to be around 0.7V. R_1 is used to create a loop that provides around 100μA operating current for the diode. 3% efficiency improvement can be achieved by using this method.

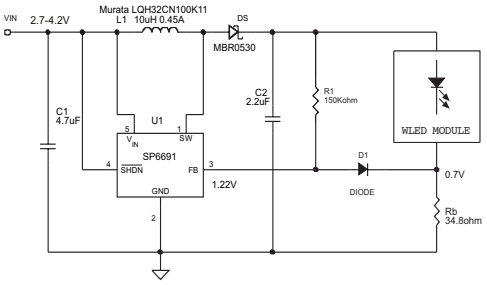


Figure 23. Improve Efficiency with Diode in Feedback Loop

To further improve the efficiency and reduce the effects of the ambient temperature on the diode D1 used in method 1, an op amp circuit can be used as shown in Figure 24. The gain of the op amp circuit can be calculated by:

$$Av = \frac{R_1 + R_2}{R_1}$$

If the voltage across the bias resistor is set to be 0.1V the current through R_1 and R_2 to be around 100μA, R_1 and R_2 can be selected as 1K and 11.2K respectively. LMV341 can be used because of its small supply current, offset voltage and minimum supply voltage. By using this method, the efficiency can be increased around 7%.

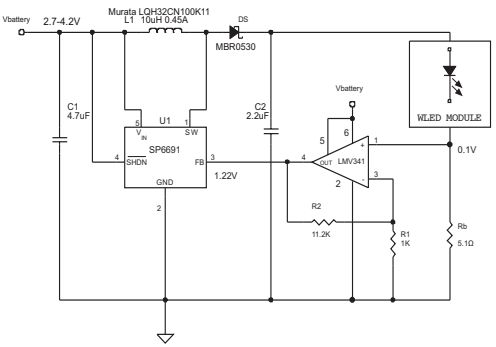
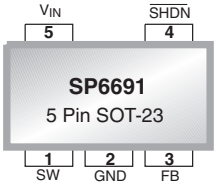
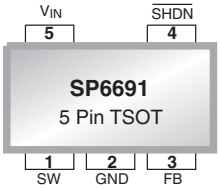
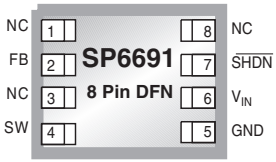


Figure 24. Improve Efficiency with Op Amp in Feedback Loop







Appendix and Web Link Information

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Sipex Application Notes:	http://www.sipex.com/applicationNotes.aspx
Product Change Notices:	http://www.sipex.com/content.aspx?p=pcn

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Milpitas, CA95035
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The following sections contain information which is more changeable in nature and is therefore generated as appendices.

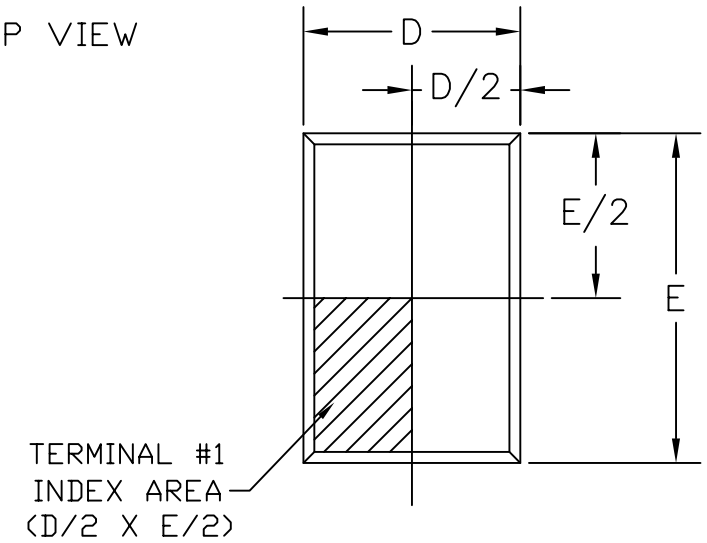
1) **Package Outline Drawings**
2) **Ordering Information**

If Available:

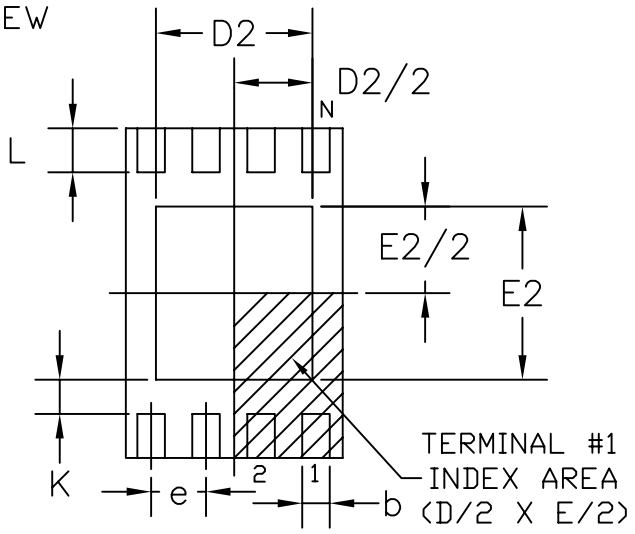
3) **Frequently Asked Questions**
4) **Evaluation Board Manuals**
5) **Reliability Reports**
6) **Product Characterization Reports**
7) **Application Notes for this product**
8) **Design Solutions for this product**

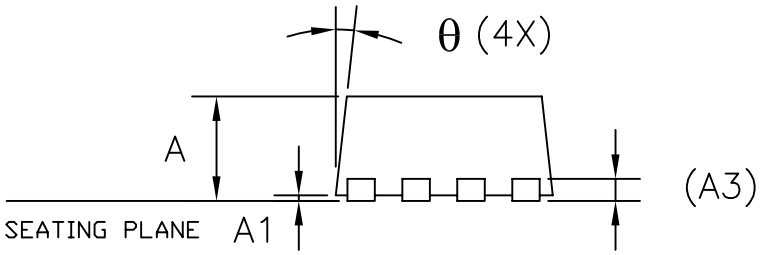
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/18/05	JL
B	MODIFY DRAWING FORMAT	07/17/06	JL

TOP VIEW



BOTTOM VIEW





SIDE VIEW

8LD 2x3 DFN JEDEC MO-229 Variation VCED-2						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.036	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.00 BSC			0.079 BSC		
D2	1.50	—	1.75	0.059	—	0.069
E	3.00 BSC			0.118 BSC		
E2	1.60	—	1.90	0.063	—	0.075
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	—	—	0.008	—	—
θ	0°	—	14°	0°	—	14°
N	8			8		
ND	4			4		

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8 PIN 2x3 DFN PACKAGE OUTLINE

Packaging Approval:

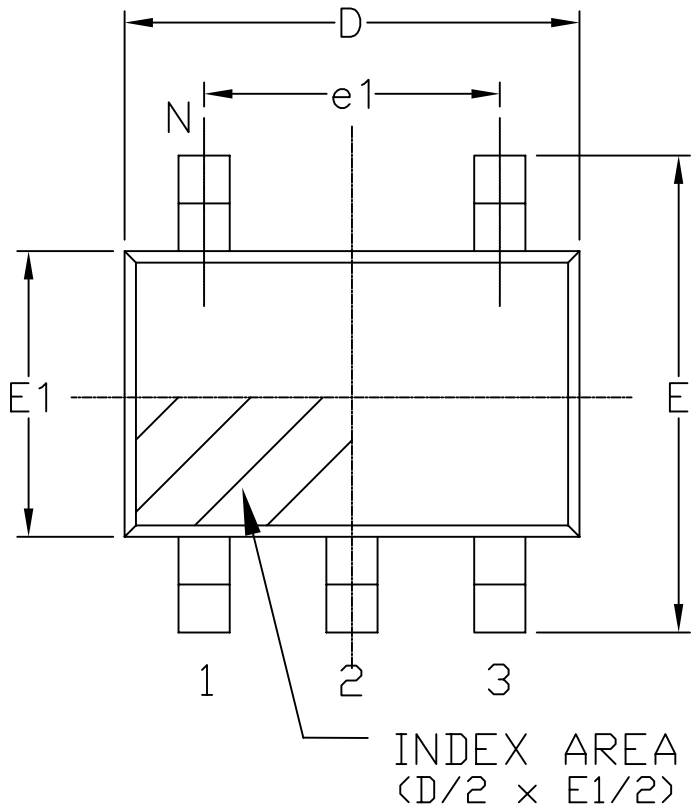
Drawing No: 8-PIN 2x3 DFN

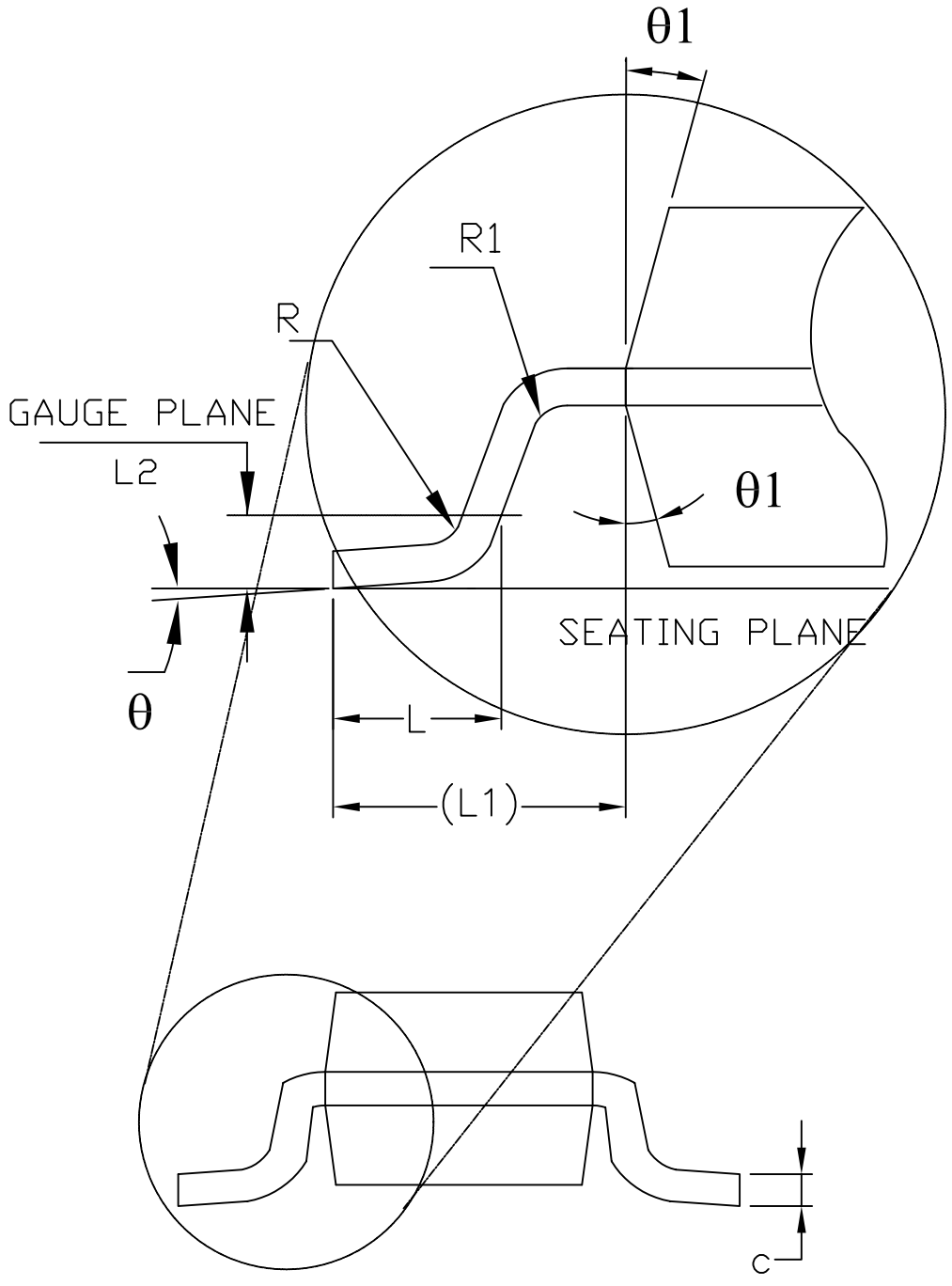
By: JL Date: 07/17/06

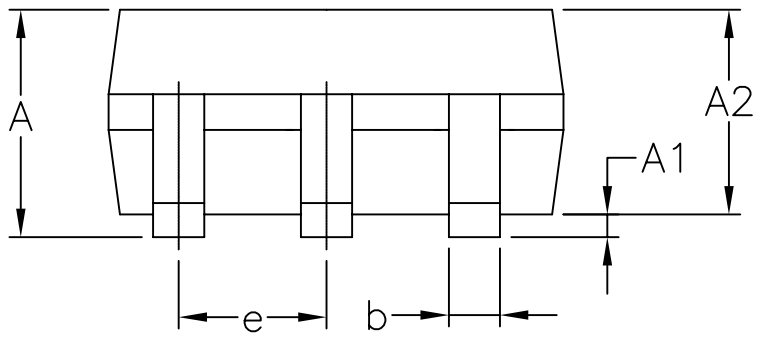
Revision: B Sheet: 1 OF 1

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/3/05	JL
B	DRAWING FORMAT MODIFICATION	07/25/06	JL

Top View







Side View

Front View

5 Pin SOT-23 JEDEC MO-178 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.45	—	—	0.057
A1	0.00	—	0.15	0.000	—	0.006
A2	0.90	1.15	1.30	0.036	0.045	0.051
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.22	0.003	—	0.009
D	2.90 BSC			0.115 BSC		
E	2.80 BSC			0.111 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	5°	10°	15°	5°	10°	15°
N	5			5		

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5 PIN SOT-23 PACKAGE OUTLINE

Packaging Approval:

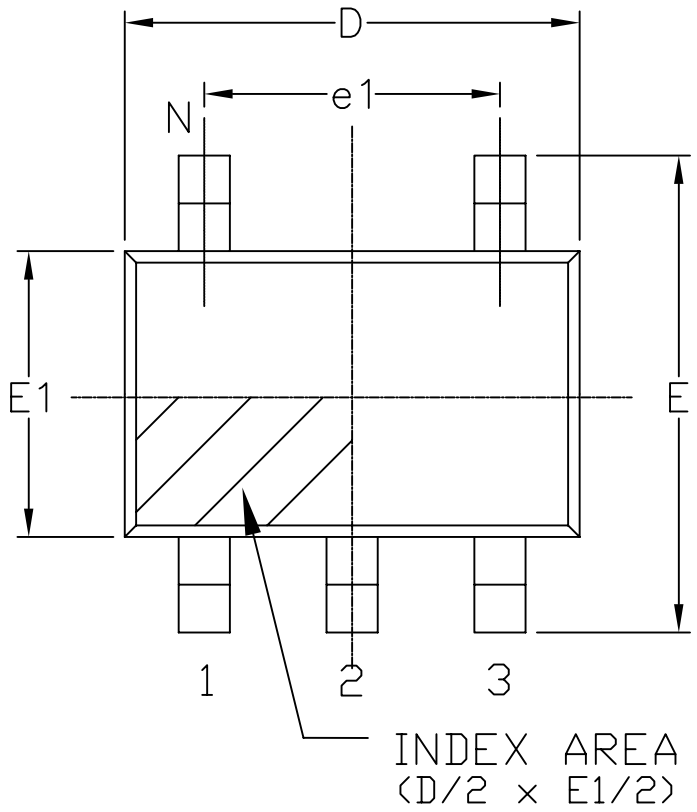
By: JL Date: 07/25/06

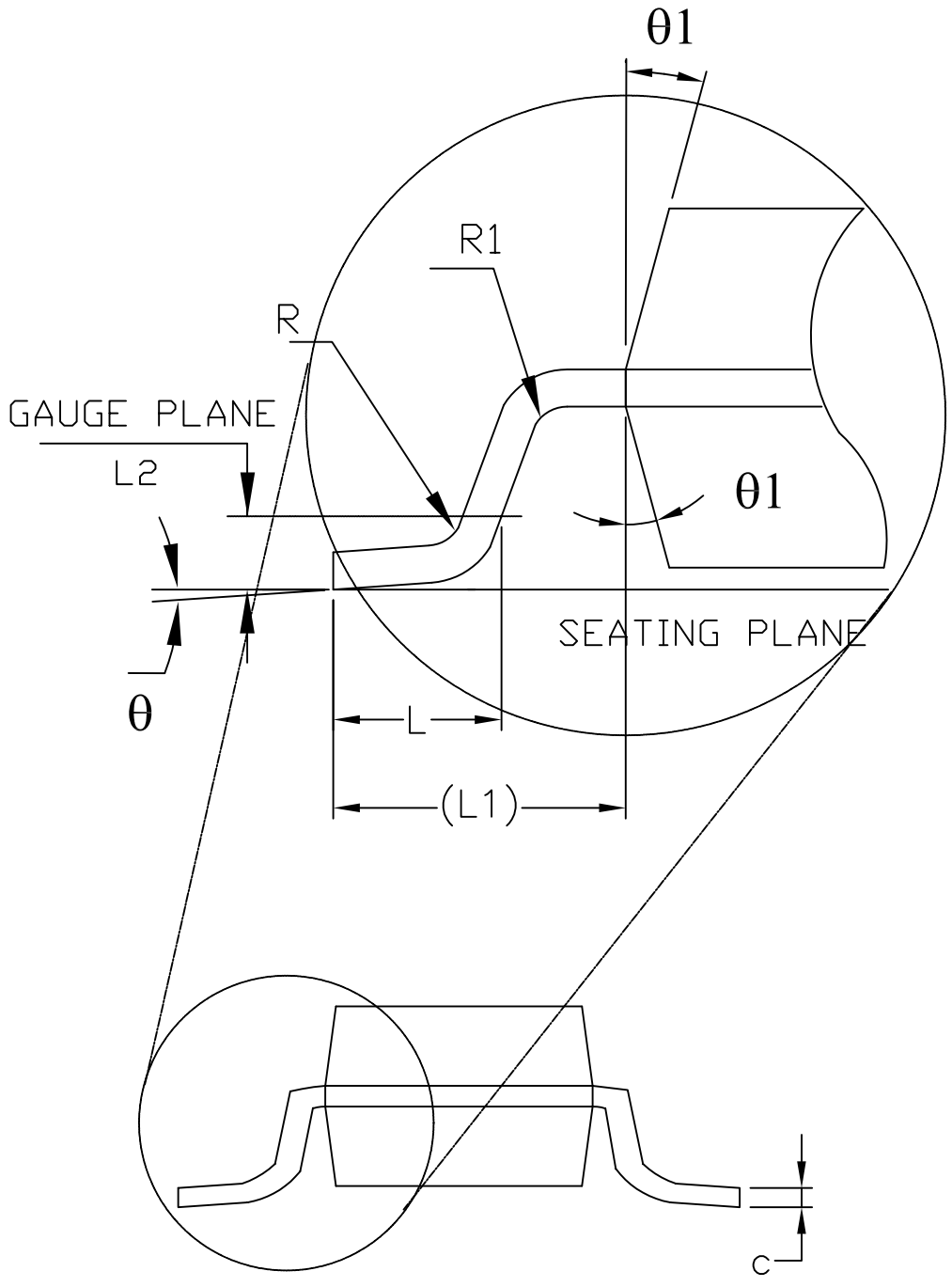
Drawing No: 5-PIN SOT-23

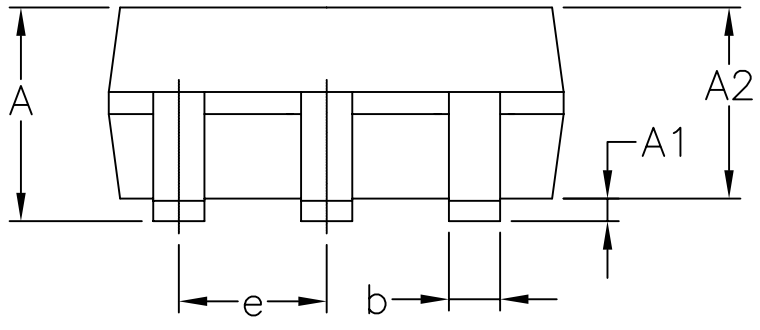
Revision: B Sheet: 1 OF 1

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/04/05	JL
B	DRAWING FORMAT MODIFICATION	09/13/06	JL

Top View







Side View

Front View

5 Pin TSOT JEDEC MO-193 Variation AB						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.10	0.000	—	0.004
A2	0.70	0.90	1.00	0.028	0.036	0.039
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	5			5		

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5 PIN TSOT PACKAGE OUTLINE

Packaging Approval:		Drawing No: 5-PIN TSOT	
By: JL	Date: 09/13/06	Revision: B	Sheet: 1 OF 1

Ordering Information

Part Number	Status	Min Temp ˚C	Max Temp ˚C	RoHS	MSL Level	Pack Type	Quantity	Package
SP6691EB	Active	0	70	N/A	Board	Eval Board. Not Available in Bulk	1	Board
SP6691ER-L	Active	-40	85	Yes	L1 @ 250ºC	Not Available in Bulk	3000	DFN8
SP6691ER-L/TR	Active	-40	85	Yes	L1 @ 250ºC	Tape & Reel	3000	DFN8
SP6691EK-L	Active	-40	85	Yes	L1 @ 260ºC	Not Available in Bulk	2500	SOT-23-5
SP6691EK-L/TR	Active	-40	85	Yes	L1 @ 260ºC	Tape & Reel	2500	SOT-23-5
SP6691EK1-L	Active	-40	85	Yes	L1 @ 260ºC	Not Available in Bulk	2500	TSOT5
SP6691EK1-L/TR	Active	-40	85	Yes	L1 @ 260ºC	Tape & Reel	2500	TSOT5
SP6691ER	EOL	-40	85	No	L1 @ 240ºC	Not Available in Bulk	3000	DFN8
SP6691EK	EOL	-40	85	No	L1 @ 240ºC	Not Available in Bulk	2500	SOT-23-5
SP6691EK/TR	EOL	-40	85	No	L1 @ 240ºC	Tape & Reel	2500	SOT-23-5
SP6691EK1	EOL	-40	85	No	L1 @ 240ºC	Not Available in Bulk	2500	TSOT5
SP6691ER/TR	OBS	-40	85	No	L1 @ 240ºC	Tape & Reel	3000	DFN8
SP6691EK1/TR	OBS	-40	85	No	L1 @ 240ºC	Tape & Reel	2500	TSOT5

Product Characterization Report

for the

SP6690 Family of Products

SP4446, SP6690, and SP6691 Products

Prepared By: Salvador Wu & Greg West
Date: January 23, 2007

Table of Contents

Introduction: This product family characterization was done as part of the qualification of Sipex's fabrication site transfer from Sipex's Hillview Fab in Milpitas, CA, to a contract foundry, Silan, in Hangzhou, China. This characterization report summarizes data for key SP6690 product family characteristics and contains distributions for all parameters. A complete listing of the product numbers covered by the characterization report is included in the "Conclusion" section of this report. The distributions in Appendix A are arranged so that the Hillview and Silan distributions for a given parameter are adjacent. A distribution for a given parameter shows different temperature data which are at -40ºC, 25ºC, and 85ºC.

Wafer Fab: Silan
Fab Location: Hangzhou, China
Process: Silan – bp1
MS: 1136

Characterization Procedure:

Hillview Lot number(s): HV6690CHAR
Silan Lot number(s): 10028
Temperatures: Ambient (25C), 85C, -40C
Tester: LTX
Test Program: SP6690_QUAL_SILAN_00.08/30/2006

Data Summary:

Key Parameter Across Temperature Data Summary

Key Parameter	Units	Hillview Fab Distribution Mean	Hillview Fab Distribution Variance	Hillview Fab Cpk (across temp)		Silan Fab Distribution Mean	Silan Fab Distribution Variance	Silan Fab Cpk (across temp)
10.0: Vfb input current Ivfb, Vin=3.3V, Vfb=1.2V @ -40C	nA	12.488	35.959	0.1065		30.125	13.759	0.7056
14.0: Vin off current, Ven=0V, Vin=3.3 @ -40 C	nA	124.000	90.805	1.5565		177.333	201.716	0.7888
15.0: Shutdown high threshold go-no-go Vsdhdn=0.8 @ 25 C	mA	6.107	258.049E-03	>4.0000		3.294	160.621E-03	>4.0000
16.0: Shutdown low threshold go-no-go Vshdn=0.3 @ -40C	uA	-23.500	3.998	>4.0000		9.333	1.988	>4.0000
17.0: Shutdown input current, Vshdn=5V, Vin=3.3. @ 85C	uA	5.366	58.160E-03	>4.0000		3.956	64.887E-03	>4.0000
18.0: Vfb posttrim rising threshold Vin=3.3 @ -40C	V	1.232	8.063E-03	0.7496		1.234	8.247E-03	1.4619
20.0: Vfb rising threshold, Vin=1.2 @ -40C	V	1.232	8.038E-03	0.7492		1.236	7.772E-03	1.4696
22.0: Vin current SW OFF @ 85C	uA	53.046	178.846	-0.0430		332.921	467.917	-0.2158
25.0: Vfb line regulation, Vin=1.2, to Vin=14 @ 85C	m%	-107.367	14.114E	1.7154		-143.645	21.476	0.5643
31.0: Current limit post trim, Vin=3.3 @ 25C	mA	410.152	16.929	0.6862		303.896	7.978	1.9264
34.0: sw Vcesat Isw=250ma Vin=3.3 @ 25C	mV	148.600	3.013	>4.0000		147.333	2.249	>4.0000
35.0: sw leakage current Vsw=5v Vin=3.3 @ 85C	nA	326.667	63.427	>4.0000		408.710	97.459	>4.0000

Conclusion:

Characterization data over temperature and Vcc range show datasheet parameters meet the spec. Cpk's for most parameters are comparable between Hillview and Silan although many show a strong temperature dependence that tends to produce lower Cpk's in this analysis.

The performance of SP6690 parts fabricated at Silan are comparable to the current SP6690 parts built from the Hillview fab.

This characterization report applies to the following SP6690 family of product part numbers:

SP4446EK
SP4446EK-L
SP6690EK
SP6690EK1
SP6690EK1-L
SP6690EK-L
SP6690ER
SP6690ER-L
SP6691EK
SP6691EK1
SP6691EK1-L
SP6691EK-L
SP6691ER
SP6691ER-L

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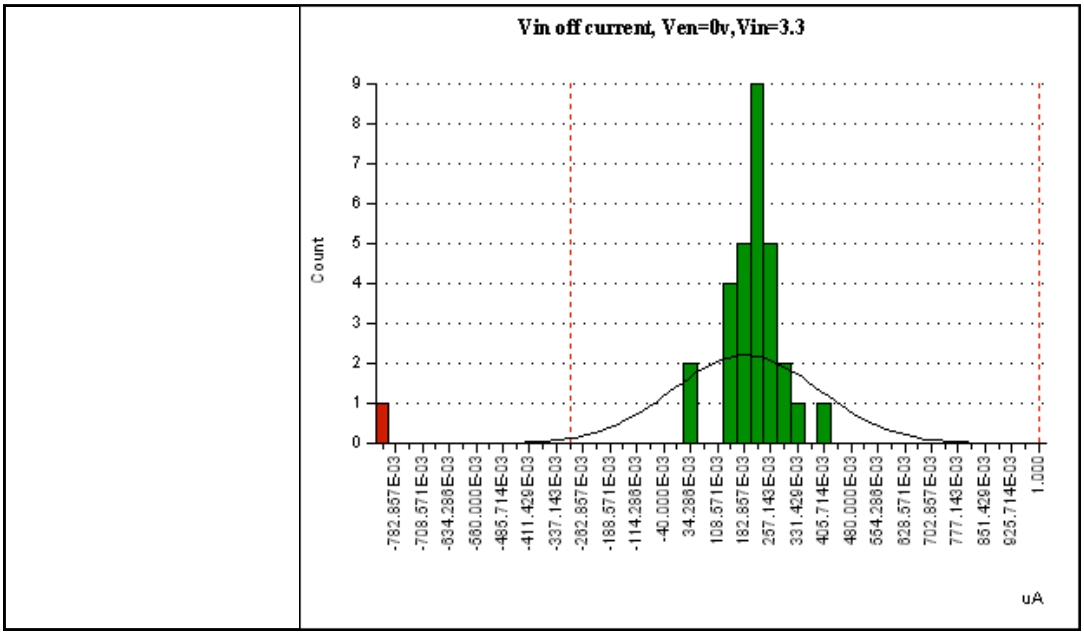
Appendix A
Characterization Data Histograms



Statistics: (uA)

Min	-820.000E-03	**StatLow**	N/A
Max	420.000E-03	**NWithinSpec**	29
Mean	177.333E-03	**NOutsideSpec**	1
StdDev	201.716E-03	**90%**	290.000E-03
25%	180.000E-03	**Range**	1.240
Mean+3*StdDev	782.480E-03	**NOutsideSpec**	1
		Cp	1.0741
Mean-3*StdDev	-427.814E-03	**Cpl**	0.7888
Cpk	0.7888	**Cpu**	1.3594
Skew	-4.3856		
StatHigh	N/A		

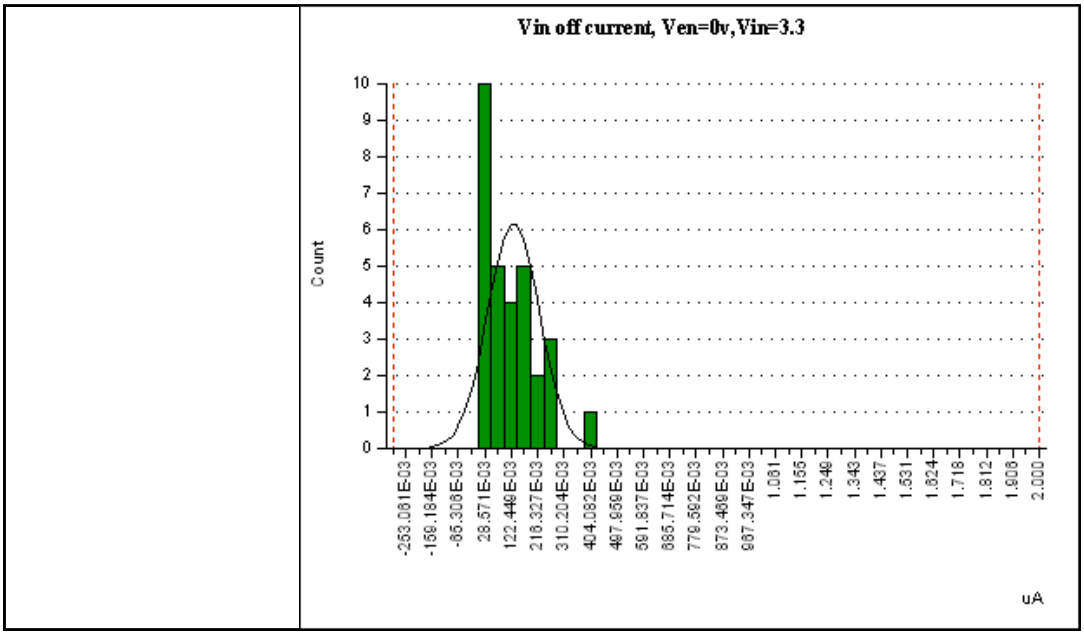
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028coldN40: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
-40C

Data: Raw Data



Statistics: (uA)

Min	30.000E-03	**StatLow**	N/A
Max	410.000E-03	**NWithinSpec**	30
Mean	124.000E-03	**NOutsideSpec**	0
StdDev	90.805E-03	**90%**	240.000E-03
25%	40.000E-03	**Range**	380.000E-03
Mean+3*StdDev	396.414E-03	**NOutsideSpec**	0
		Cp	>4.0000
Mean-3*StdDev	-148.414E-03	**Cpl**	1.5565
Cpk	1.5565	**Cpu**	>4.0000
Skew	1.2350		
StatHigh	N/A		

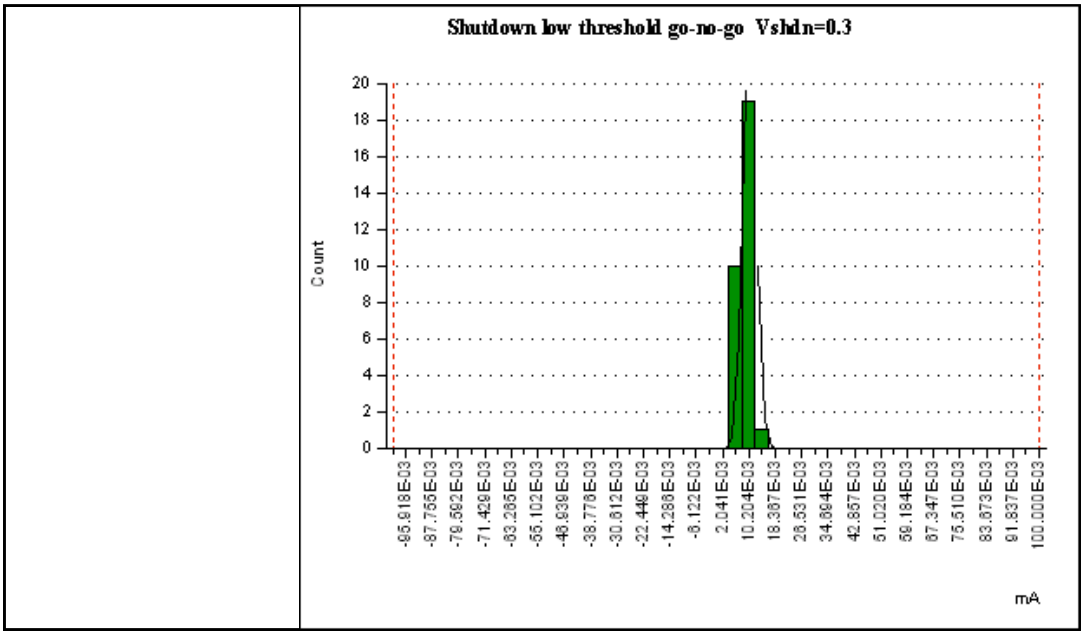
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HV6690CHARcold: N/A	MS1136EW	SP6690	_	char	Silan	BP1	26-SEP-2006	ETS500D	SP6690_QUAL_SILAN_00.08/30/2006	-	0

Conditions

temp
-40C

Data: Raw Data



Statistics: (mA)

Min	6.000E-03	**StatLow**	N/A
Max	13.000E-03	**NWithinSpec**	30
Mean	9.333E-03	**NOutsideSpec**	0
StdDev	1.988E-03	**90%**	12.000E-03
25%	8.000E-03	**Range**	7.000E-03
Mean+3*StdDev	15.299E-03	**NOutsideSpec**	0
Mean-3*StdDev	3.368E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.2151	**Cpu**	>4.0000
StatHigh	N/A		

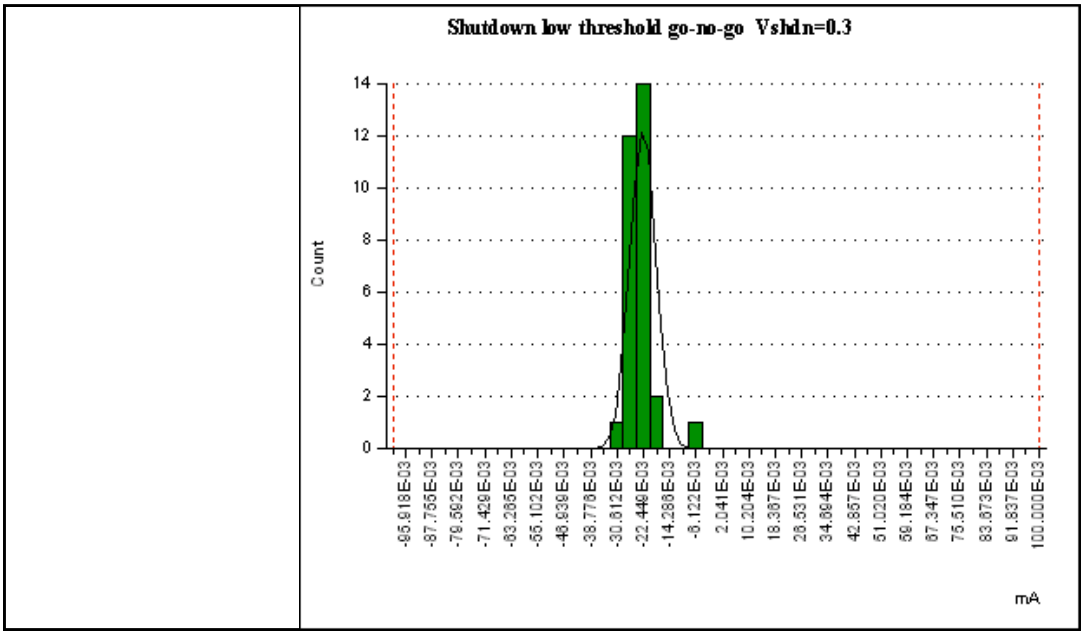
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028coldN40: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
-40C

Data: Raw Data



Statistics: (mA)

Min	-29.000E-03	**StatLow**	N/A
Max	-7.000E-03	**NWithinSpec**	30
Mean	-23.500E-03	**NOutsideSpec**	0
StdDev	3.998E-03	**90%**	-20.500E-03
25%	-25.000E-03	**Range**	22.000E-03
Mean+3*StdDev	-11.506E-03	**NOutsideSpec**	0
Mean-3*StdDev	-35.494E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	2.4701	**Cpu**	>4.0000
StatHigh	N/A		

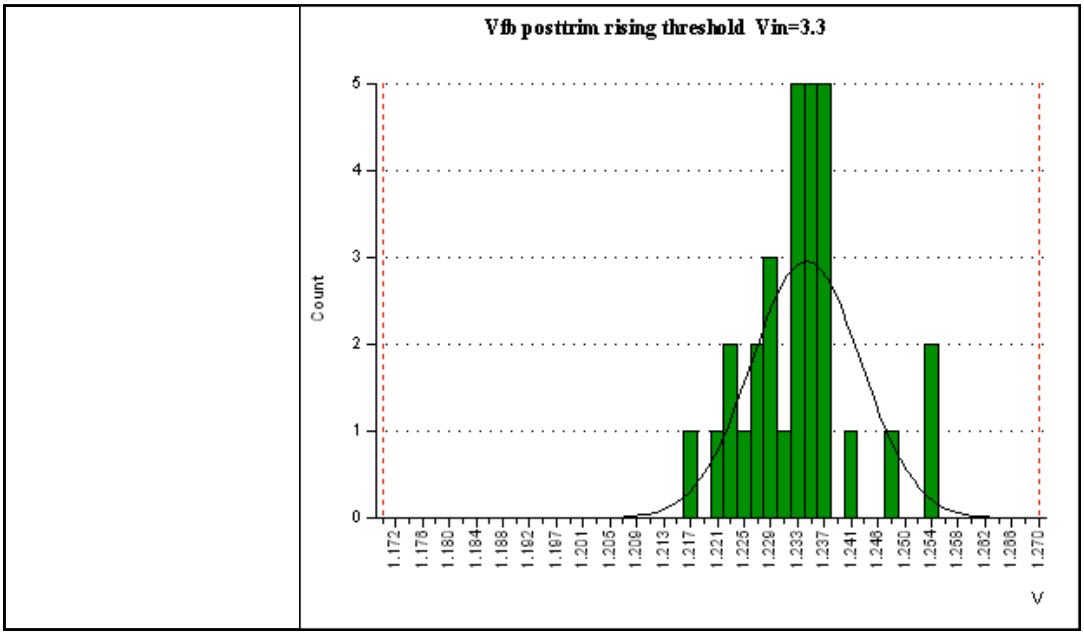
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HV6690CHARcold: N/A	MS1136EW	SP6690	_	char	Silan	BP1	26-SEP-2006	ETS500D	SP6690_QUAL_SILAN_00.08/30/2006	-	0

Conditions

temp
-40C

Data: Raw Data



Statistics: (V)

Min	1.217	**StatLow**	N/A
Max	1.254	**NWithinSpec**	30
Mean	1.234	**NOutsideSpec**	0
StdDev	8.247E-03	**90%**	1.244
25%	1.229	**Range**	37.000E-03
Mean+3*StdDev	1.259	**NOutsideSpec**	0
Mean-3*StdDev	1.209	**Cp**	2.0210
Cpk	1.4619	**Cpl**	2.5802
Skew	0.5002	**Cpu**	1.4619
StatHigh	N/A		

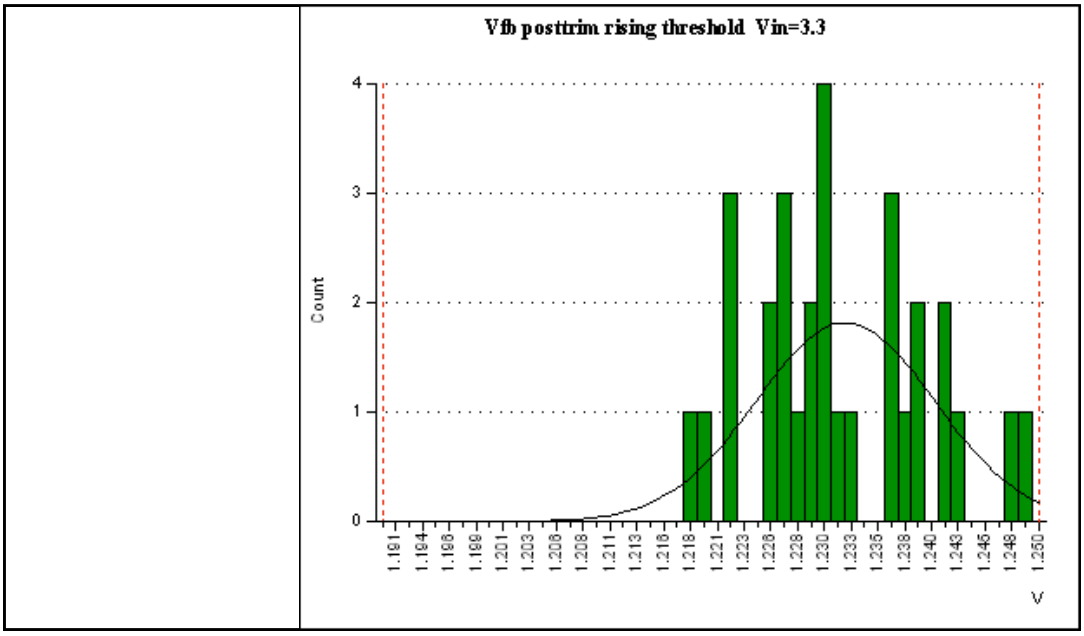
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028coldN40: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
-40C

Data: Raw Data



Statistics: (V)

Min	1.218	**StatLow**	N/A
Max	1.249	**NWithinSpec**	30
Mean	1.232	**NOutsideSpec**	0
StdDev	8.063E-03	**90%**	1.243
25%	1.227	**Range**	31.000E-03
Mean+3*StdDev	1.256	**NOutsideSpec**	0
		Cp	1.2402
Mean-3*StdDev	1.208	**Cpl**	1.7308
		Cpu	0.7496
Cpk	0.7496		
Skew	0.3036		
StatHigh	N/A		

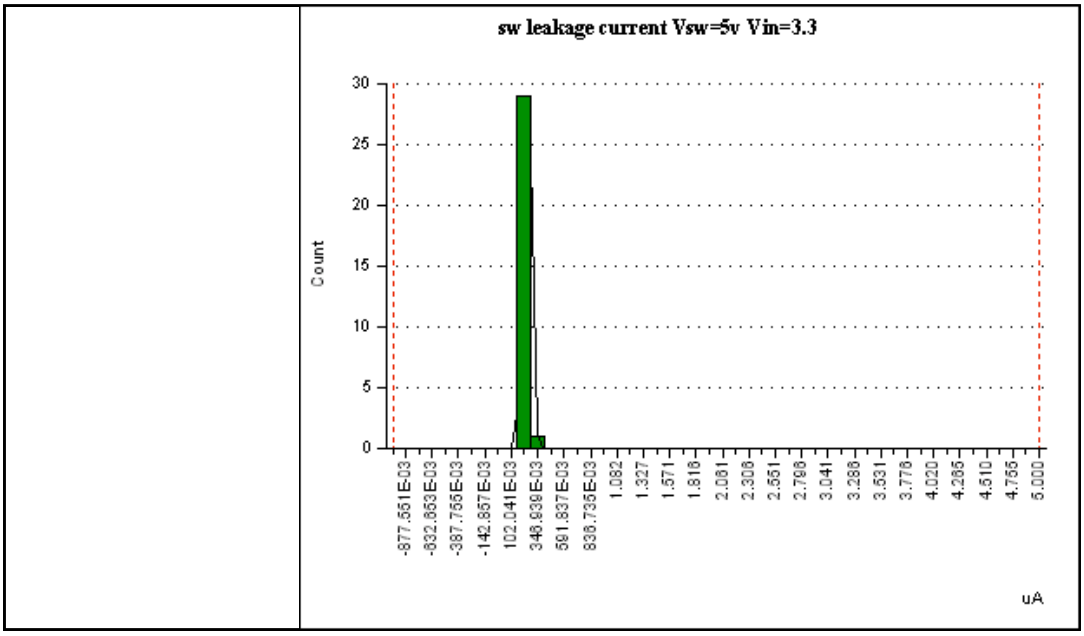
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HV6690CHARcold: N/A	MS1136EW	SP6690	_	char	Silan	BP1	26-SEP-2006	ETS500D	SP6690_QUAL_SILAN_00.08/30/2006	-	0

Conditions

temp
-40C

Data: Raw Data



Statistics: (uA)

Min	170.000E-03	**StatLow**	N/A
Max	290.000E-03	**NWithinSpec**	30
Mean	223.667E-03	**NOutsideSpec**	0
StdDev	36.529E-03	**90%**	275.000E-03
25%	190.000E-03	**Range**	120.000E-03
Mean+3*StdDev	333.254E-03	**NOutsideSpec**	0
Mean-3*StdDev	114.080E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.1621	**Cpu**	>4.0000
StatHigh	N/A		

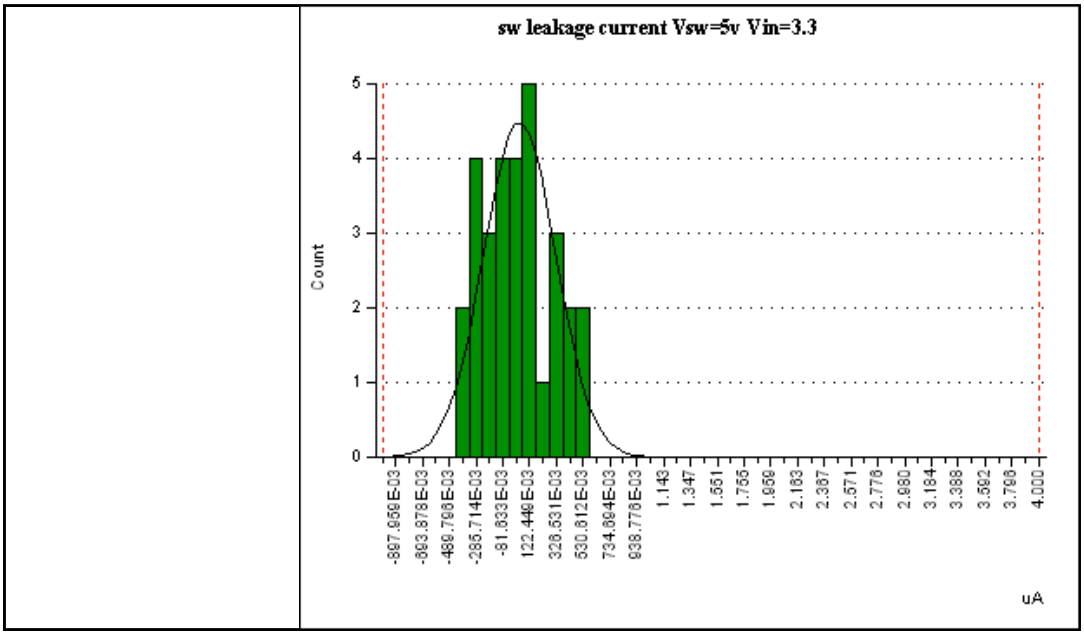
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028coldN40: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
-40C

Data: Raw Data



Statistics: (uA)

Min	-390.000E-03	**StatLow**	N/A
Max	560.000E-03	**NWithinSpec**	30
Mean	31.333E-03	**NOutsideSpec**	0
StdDev	272.191E-03	**90%**	425.000E-03
25%	-190.000E-03	**Range**	950.000E-03
Mean+3*StdDev	847.906E-03	**NOutsideSpec**	0
Mean-3*StdDev	-785.239E-03	**Cp**	3.0616
Cpk	1.2630	**Cpl**	1.2630
Skew	0.2330	**Cpu**	>4.0000
StatHigh	N/A		

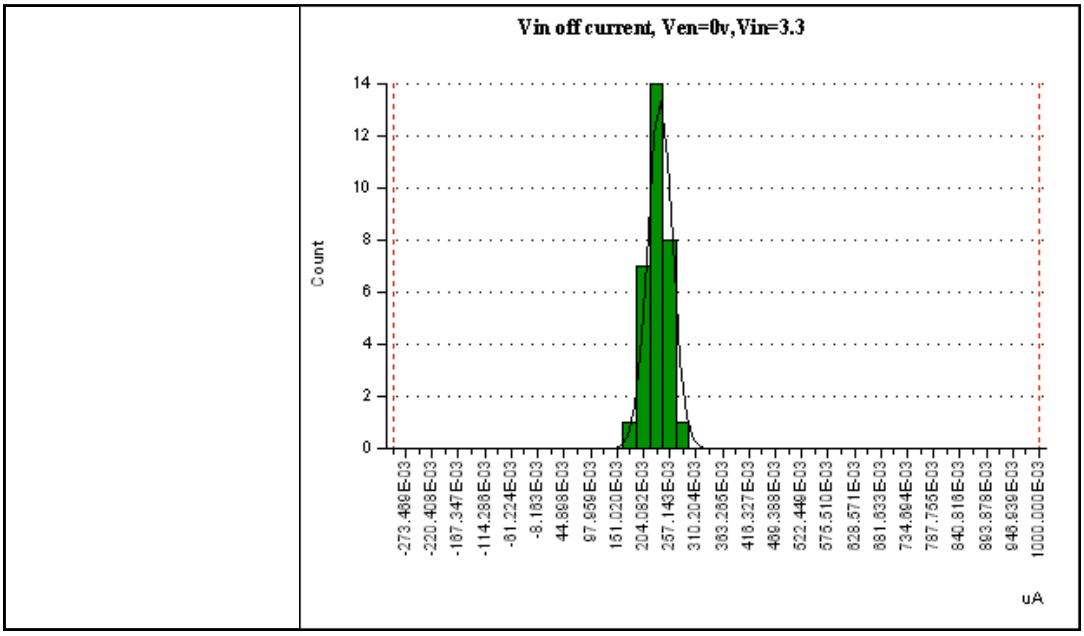
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HV6690CHARcold: N/A	MS1136EW	SP6690	_	char	Silan	BP1	26-SEP-2006	ETS500D	SP6690_QUAL_SILAN_00.08/30/2006	-	0

Conditions

temp
-40C

Data: Raw Data



Statistics: (uA)

Min	190.000E-03	**StatLow**	N/A
Max	290.000E-03	**NWithinSpec**	31
Mean	230.968E-03	**NOutsideSpec**	0
StdDev	24.543E-03	**90%**	260.000E-03
25%	210.000E-03	**Range**	100.000E-03
Mean+3*StdDev	304.597E-03	**NOutsideSpec**	0
Mean-3*StdDev	157.338E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.3869	**Cpu**	>4.0000
StatHigh	N/A		

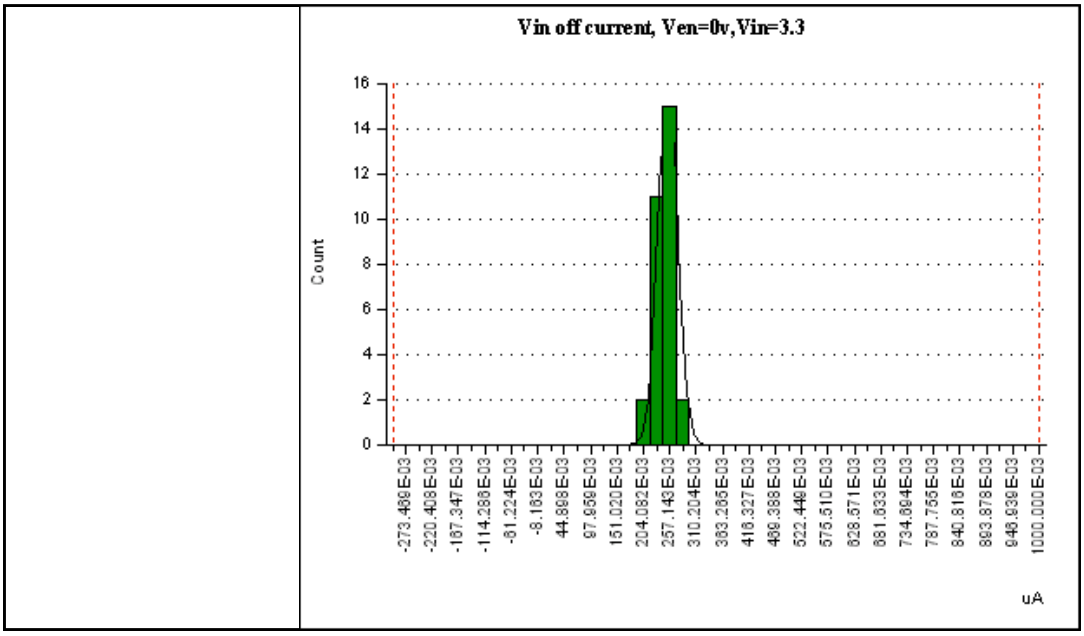
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028hot85: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
85C

Data: Raw Data



Statistics: (uA)

Min	210.000E-03	**StatLow**	N/A
Max	290.000E-03	**NWithinSpec**	30
Mean	246.667E-03	**NOutsideSpec**	0
StdDev	19.357E-03	**90%**	270.000E-03
25%	230.000E-03	**Range**	80.000E-03
Mean+3*StdDev	304.739E-03	**NOutsideSpec**	0
Mean-3*StdDev	188.594E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.0498	**Cpu**	>4.0000
StatHigh	N/A		

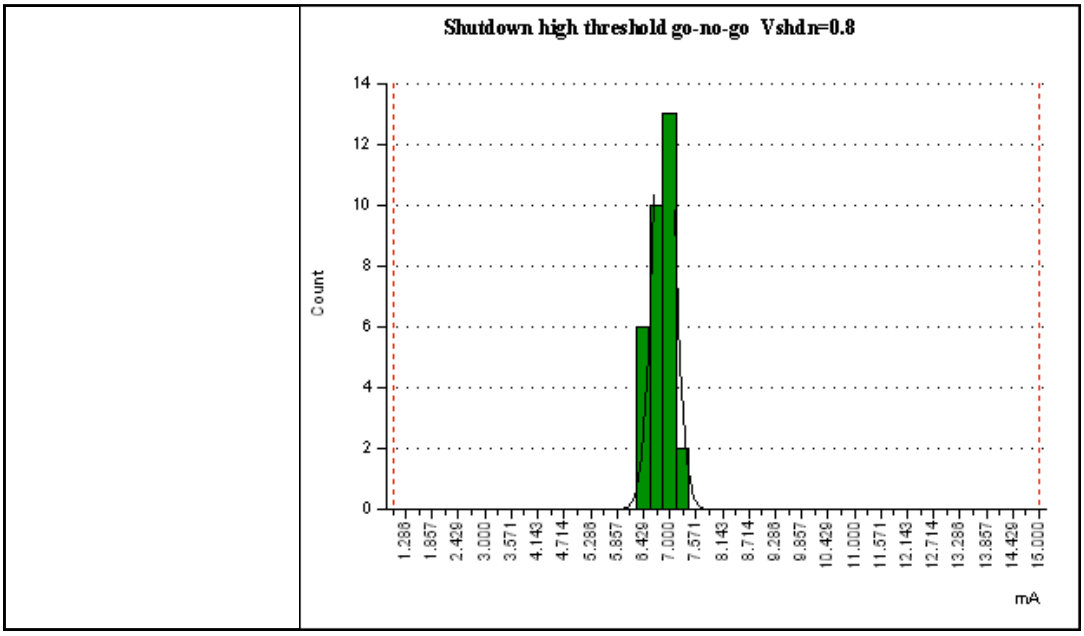
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662CHAR_HOT: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
85C

Data: Raw Data



Statistics: (mA)

Min	6.303	**StatLow**	N/A
Max	7.183	**NWithinSpec**	31
Mean	6.804	**NOutsideSpec**	0
StdDev	233.412E-03	**90%**	7.074
25%	6.601	**Range**	880.000E-03
Mean+3*StdDev	7.504	**NOutsideSpec**	0
Mean-3*StdDev	6.103	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.3847	**Cpu**	>4.0000
StatHigh	N/A		

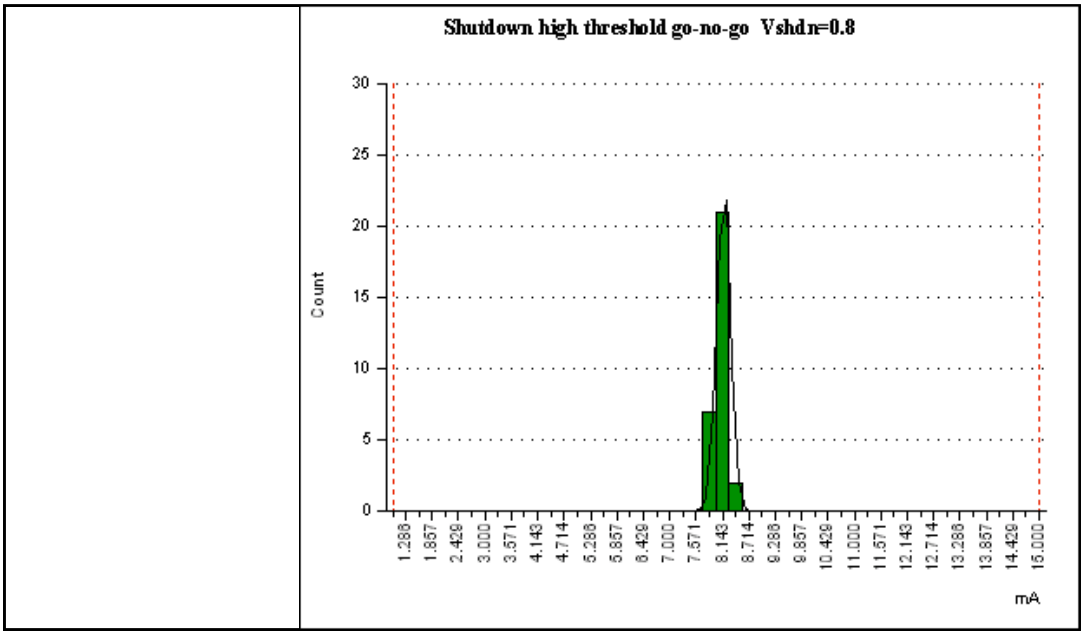
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028hot85: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
85C

Data: Raw Data



Statistics: (mA)

Min	7.796	**StatLow**	N/A
Max	8.417	**NWithinSpec**	30
Mean	8.090	**NOutsideSpec**	0
StdDev	148.215E-03	**90%**	8.272
25%	8.000	**Range**	621.000E-03
Mean+3*StdDev	8.535	**NOutsideSpec**	0
Mean-3*StdDev	7.646	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.0774	**Cpu**	>4.0000
StatHigh	N/A		

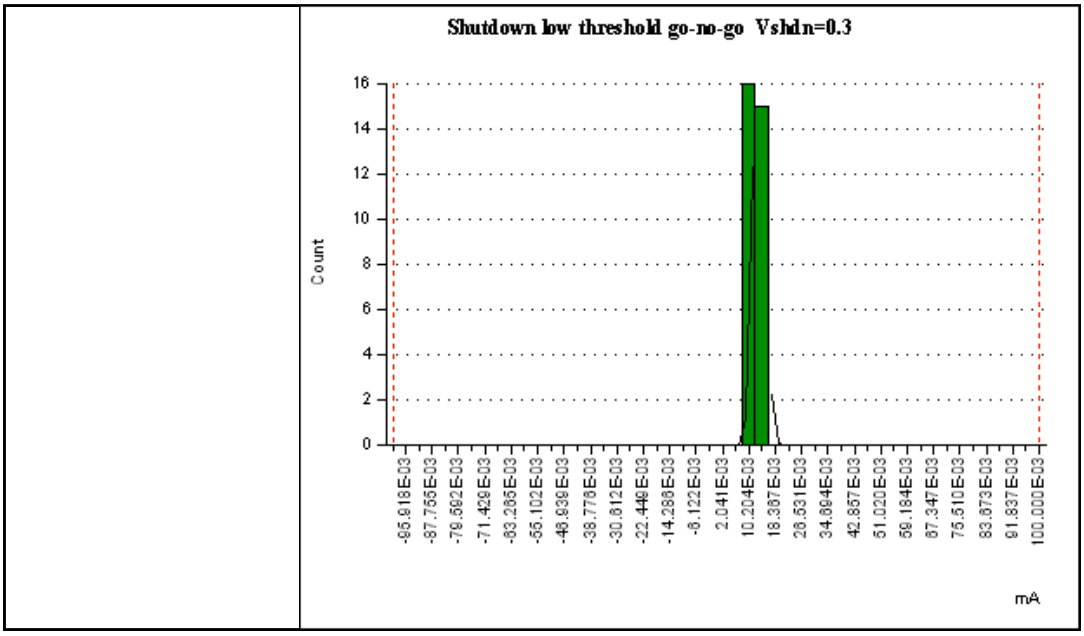
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662CHAR_HOT: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
85C

Data: Raw Data



Statistics: (mA)

Min	9.000E-03	**StatLow**	N/A
Max	15.000E-03	**NWithinSpec**	31
Mean	12.226E-03	**NOutsideSpec**	0
StdDev	1.647E-03	**90%**	14.000E-03
25%	11.000E-03	**Range**	6.000E-03
Mean+3*StdDev	17.168E-03	**NOutsideSpec**	0
Mean-3*StdDev	7.284E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.1953	**Cpu**	>4.0000
StatHigh	N/A		

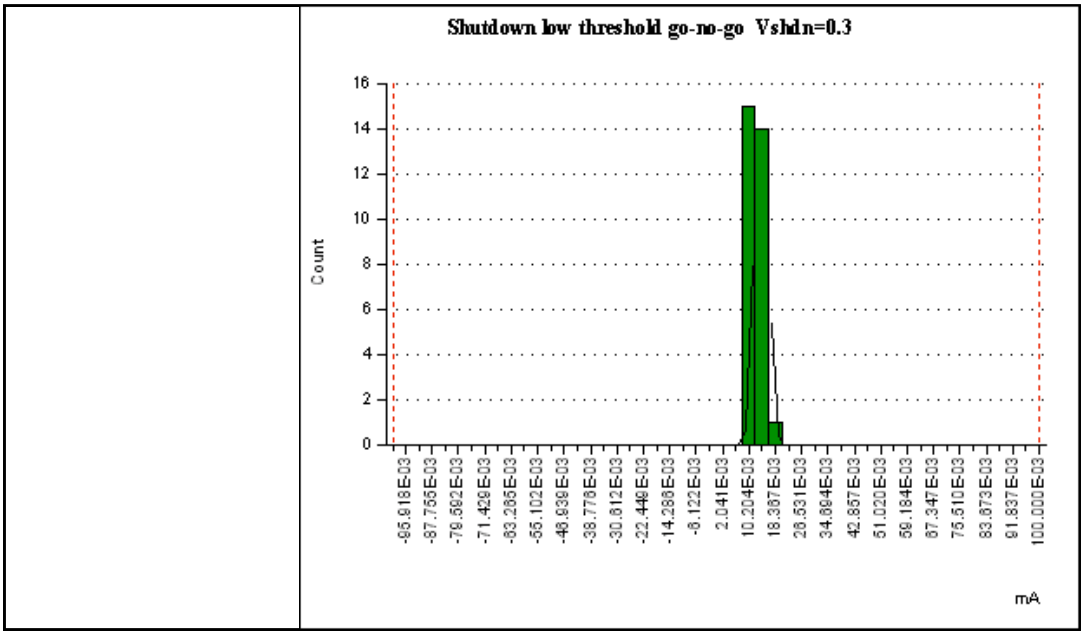
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028hot85: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
85C

Data: Raw Data



Statistics: (mA)

Min	10.000E-03	**StatLow**	N/A
Max	17.000E-03	**NWithinSpec**	30
Mean	12.800E-03	**NOutsideSpec**	0
StdDev	1.769E-03	**90%**	15.500E-03
25%	12.000E-03	**Range**	7.000E-03
Mean+3*StdDev	18.108E-03	**NOutsideSpec**	0
Mean-3*StdDev	7.492E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.4849	**Cpu**	>4.0000
StatHigh	N/A		

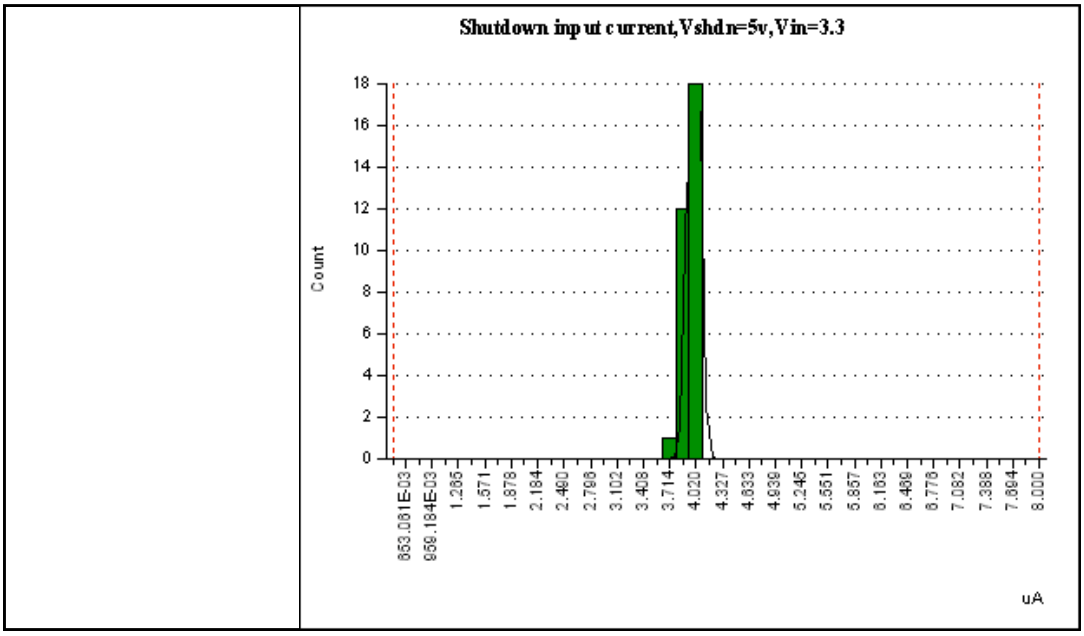
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662CHAR_HOT: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
85C

Data: Raw Data



Statistics: (uA)

Min	3.770	**StatLow**	N/A
Max	4.060	**NWithinSpec**	31
Mean	3.956	**NOutsideSpec**	0
StdDev	64.887E-03	**90%**	4.030
25%	3.930	**Range**	290.000E-03
Mean+3*StdDev	4.151	**NOutsideSpec**	0
		Cp	>4.0000
Mean-3*StdDev	3.762	**Cpl**	>4.0000
Cpk	>4.0000	**Cpu**	>4.0000
Skew	-0.8190		
StatHigh	N/A		

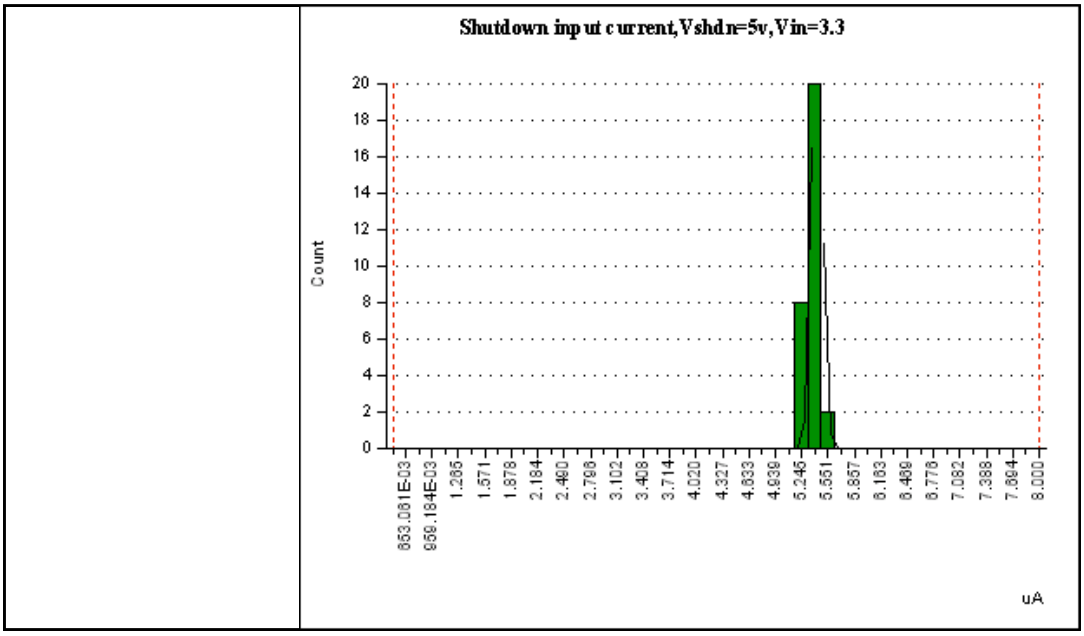
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028hot85: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
85C

Data: Raw Data



Statistics: (uA)

Min	5.260	**StatLow**	N/A
Max	5.480	**NWithinSpec**	30
Mean	5.366	**NOutsideSpec**	0
StdDev	58.160E-03	**90%**	5.455
25%	5.320	**Range**	220.000E-03
Mean+3*StdDev	5.541	**NOutsideSpec**	0
		Cp	>4.0000
Mean-3*StdDev	5.192	**Cpl**	>4.0000
Cpk	>4.0000	**Cpu**	>4.0000
Skew	0.4409		
StatHigh	N/A		

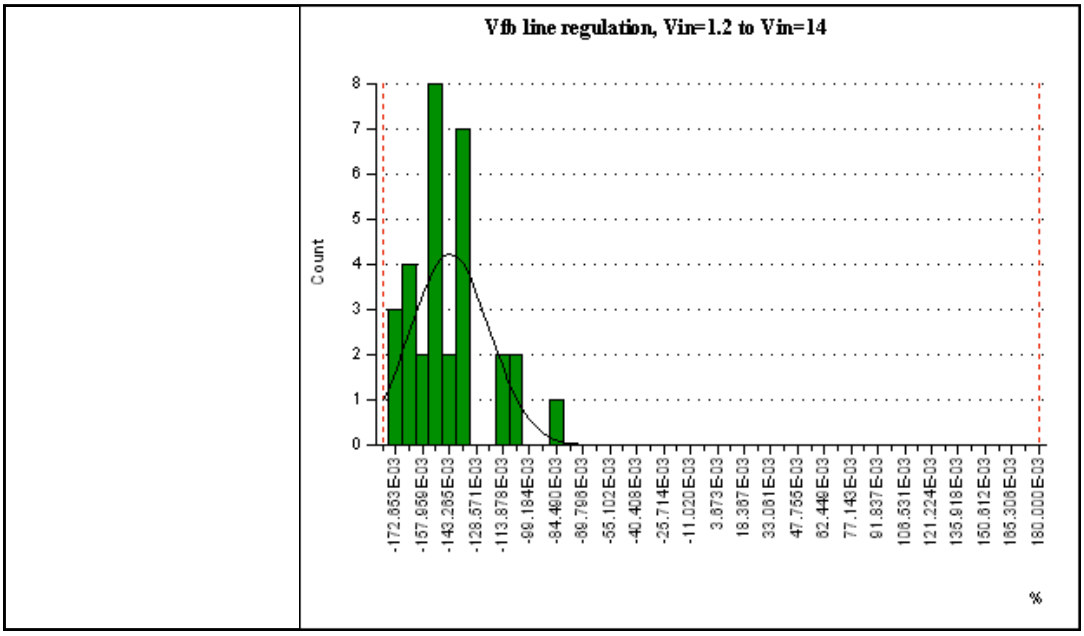
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662CHAR_HOT: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
85C

Data: Raw Data



Statistics: (%)

Min	-174.000E-03	**StatLow**	N/A
Max	-81.000E-03	**NWithinSpec**	31
Mean	-143.645E-03	**NOutsideSpec**	0
StdDev	21.476E-03	**90%**	-111.000E-03
25%	-159.000E-03	**Range**	93.000E-03
Mean+3*StdDev	-79.216E-03	**NOutsideSpec**	0
Mean-3*StdDev	-208.074E-03	**Cp**	2.7938
Cpk	0.5643	**Cpl**	0.5643
Skew	0.9454	**Cpu**	>4.0000
StatHigh	N/A		

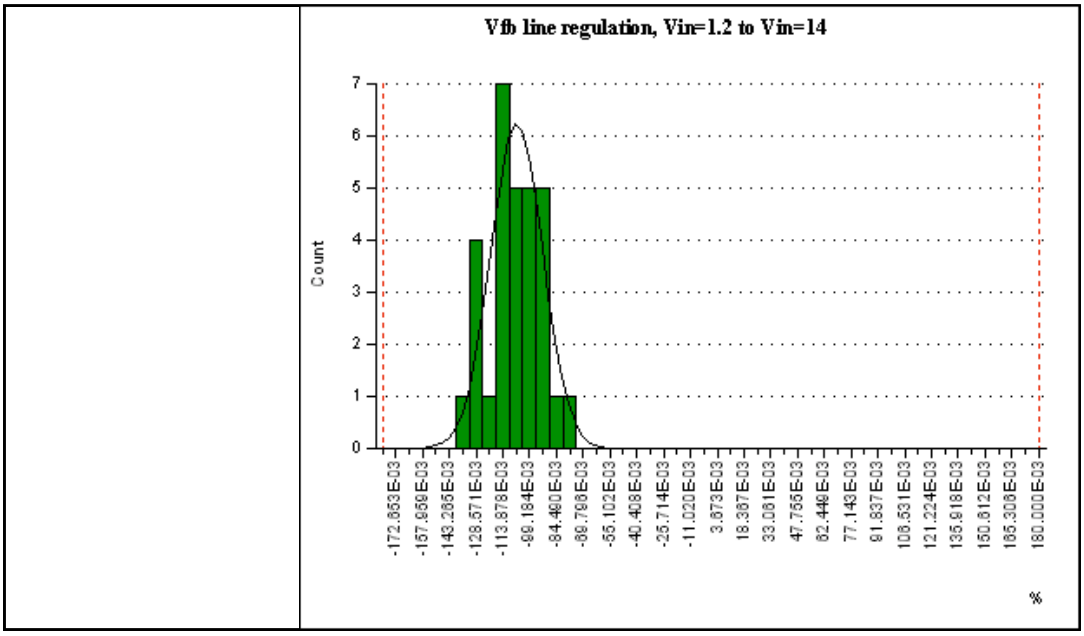
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028hot85: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
85C

Data: Raw Data



Statistics: (%)

Min	-136.000E-03	**StatLow**	N/A
Max	-80.000E-03	**NWithinSpec**	30
Mean	-107.367E-03	**NOutsideSpec**	0
StdDev	14.114E-03	**90%**	-90.000E-03
25%	-116.000E-03	**Range**	56.000E-03
Mean+3*StdDev	-65.025E-03	**NOutsideSpec**	0
Mean-3*StdDev	-149.709E-03	**Cp**	>4.0000
Cpk	1.7154	**Cpl**	1.7154
Skew	-0.0146	**Cpu**	>4.0000
StatHigh	N/A		

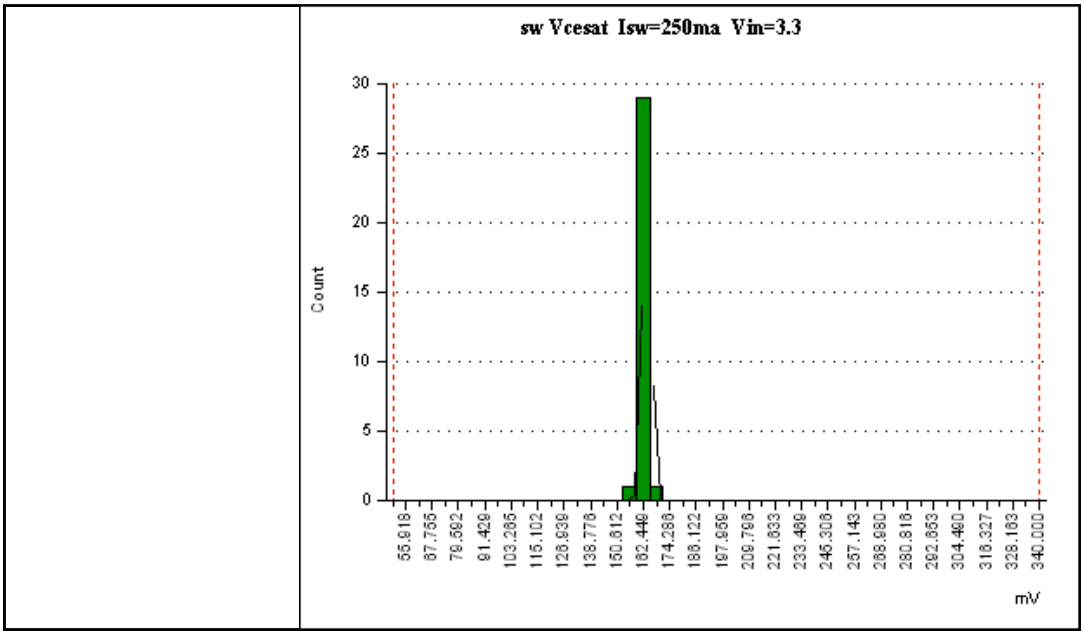
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662CHAR_HOT: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
85C

Data: Raw Data



Statistics: (mV)

Min	158.000	**StatLow**	N/A
Max	167.000	**NWithinSpec**	31
Mean	162.806	**NOutsideSpec**	0
StdDev	1.778	**90%**	165.000
25%	161.000	**Range**	9.000
Mean+3*StdDev	168.140	**NOutsideSpec**	0
Mean-3*StdDev	157.472	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.2200	**Cpu**	>4.0000
StatHigh	N/A		

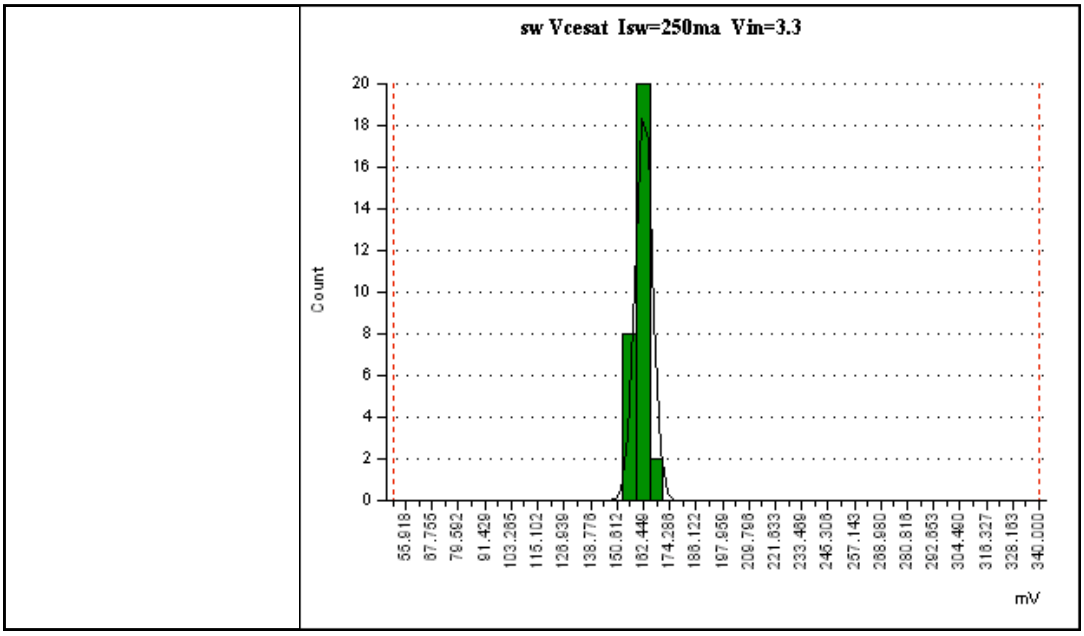
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028hot85: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
85C

Data: Raw Data



Statistics: (mV)

Min	154.000	**StatLow**	N/A
Max	166.000	**NWithinSpec**	30
Mean	161.400	**NOutsideSpec**	0
StdDev	3.663	**90%**	165.000
25%	159.000	**Range**	12.000
Mean+3*StdDev	172.390	**NOutsideSpec**	0
Mean-3*StdDev	150.410	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.7582	**Cpu**	>4.0000
StatHigh	N/A		

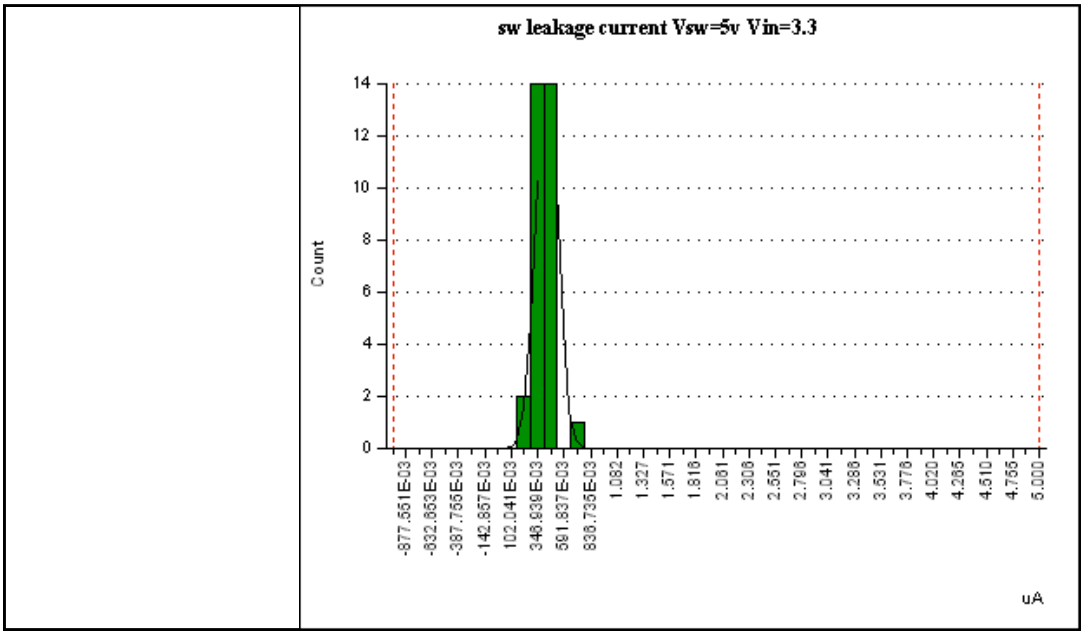
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662CHAR_HOT: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
85C

Data: Raw Data



Statistics: (uA)

Min	230.000E-03	**StatLow**	N/A
Max	750.000E-03	**NWithinSpec**	31
Mean	408.710E-03	**NOutsideSpec**	0
StdDev	97.459E-03	**90%**	510.000E-03
25%	360.000E-03	**Range**	520.000E-03
Mean+3*StdDev	701.087E-03	**NOutsideSpec**	0
Mean-3*StdDev	116.332E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	1.2682	**Cpu**	>4.0000
StatHigh	N/A		

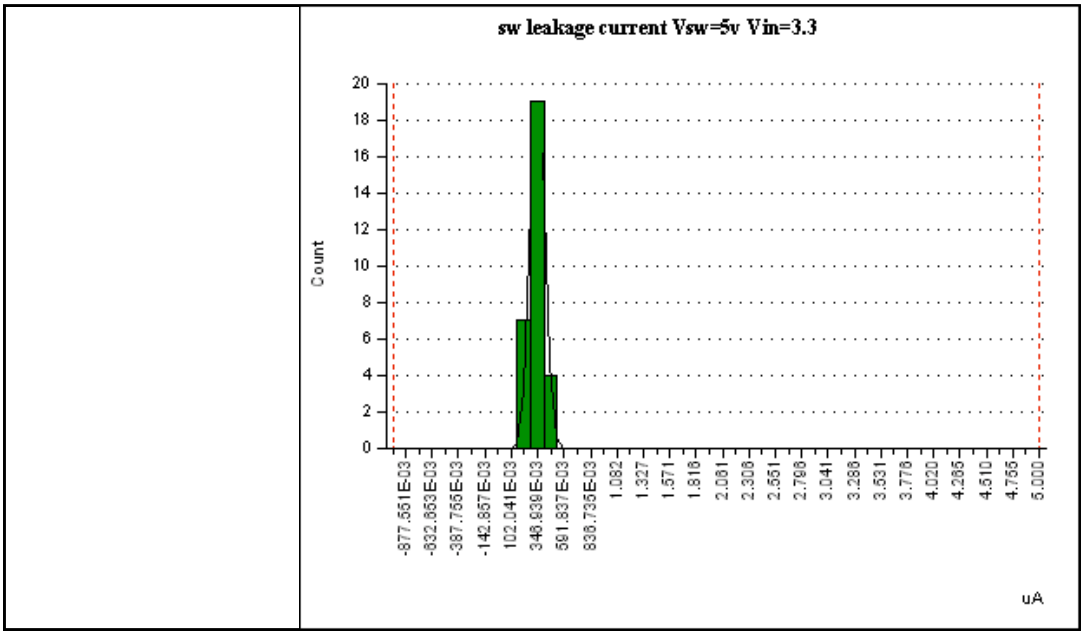
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
silanca10028hot85: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
85C

Data: Raw Data



Statistics: (uA)

Min	200.000E-03	**StatLow**	N/A
Max	460.000E-03	**NWithinSpec**	30
Mean	326.667E-03	**NOutsideSpec**	0
StdDev	63.427E-03	**90%**	435.000E-03
25%	290.000E-03	**Range**	260.000E-03
Mean+3*StdDev	516.948E-03	**NOutsideSpec**	0
Mean-3*StdDev	136.386E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.3370	**Cpu**	>4.0000
StatHigh	N/A		

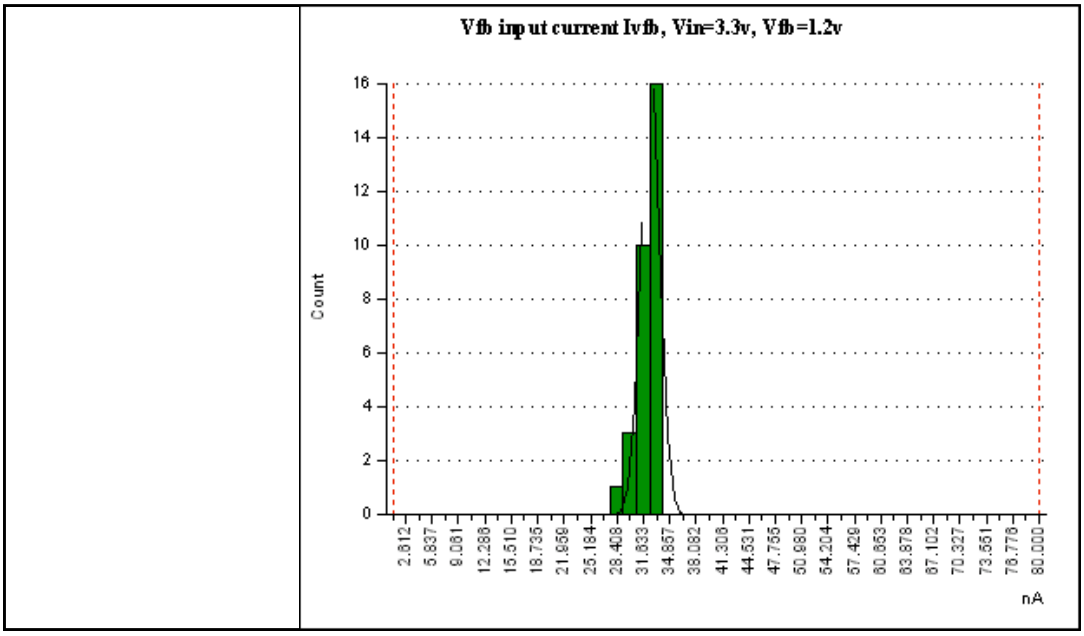
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662CHAR_HOT: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

Temp
85C

Data: Raw Data



Statistics: (nA)

Min	28.430	**StatLow**	N/A
Max	33.530	**NWithinSpec**	30
Mean	32.096	**NOutsideSpec**	0
StdDev	1.100	**90%**	33.405
25%	31.330	**Range**	5.100
Mean+3*StdDev	35.396	**NOutsideSpec**	0
Mean-3*StdDev	28.797	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-1.4342	**Cpu**	>4.0000
StatHigh	N/A		

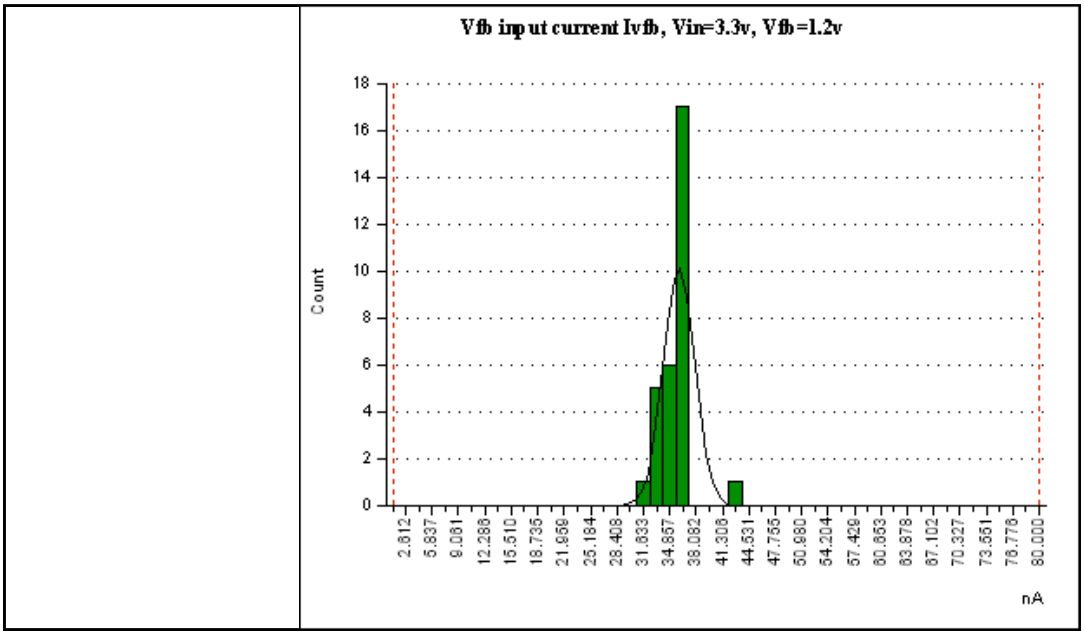
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (nA)

Min	31.340	**StatLow**	N/A
Max	42.150	**NWithinSpec**	30
Mean	35.573	**NOutsideSpec**	0
StdDev	1.897	**90%**	37.020
25%	34.860	**Range**	10.810
Mean+3*StdDev	41.264	**NOutsideSpec**	0
Mean-3*StdDev	29.883	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.8536	**Cpu**	>4.0000
StatHigh	N/A		

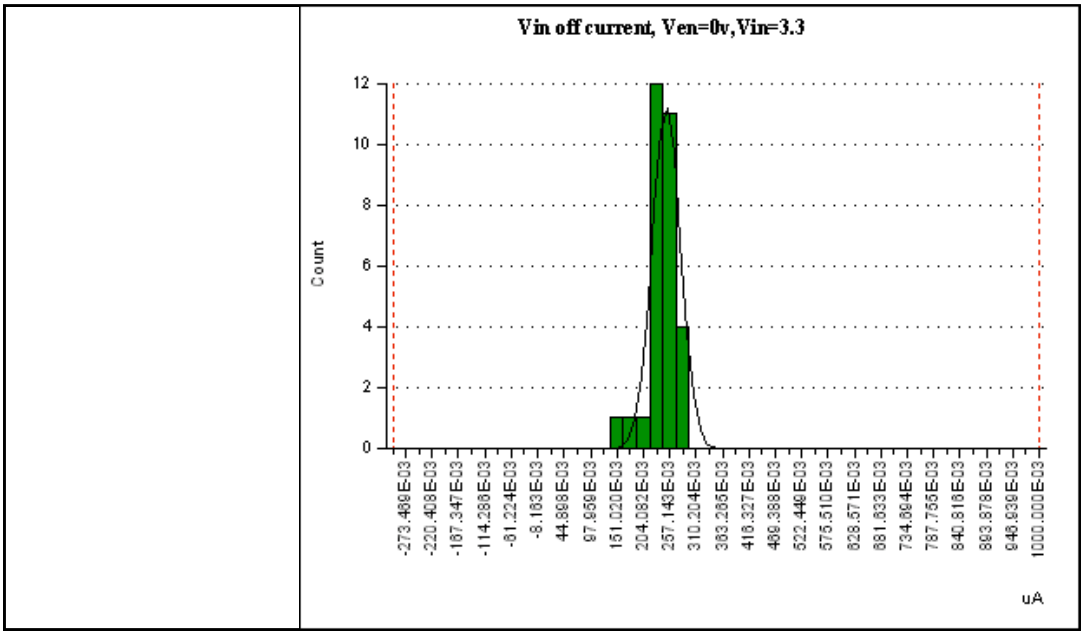
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (uA)

Min	160.000E-03	**StatLow**	N/A
Max	290.000E-03	**NWithinSpec**	30
Mean	243.667E-03	**NOutsideSpec**	0
StdDev	28.221E-03	**90%**	280.000E-03
25%	230.000E-03	**Range**	130.000E-03
Mean+3*StdDev	328.330E-03	**NOutsideSpec**	0
Mean-3*StdDev	159.003E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.7866	**Cpu**	>4.0000
StatHigh	N/A		

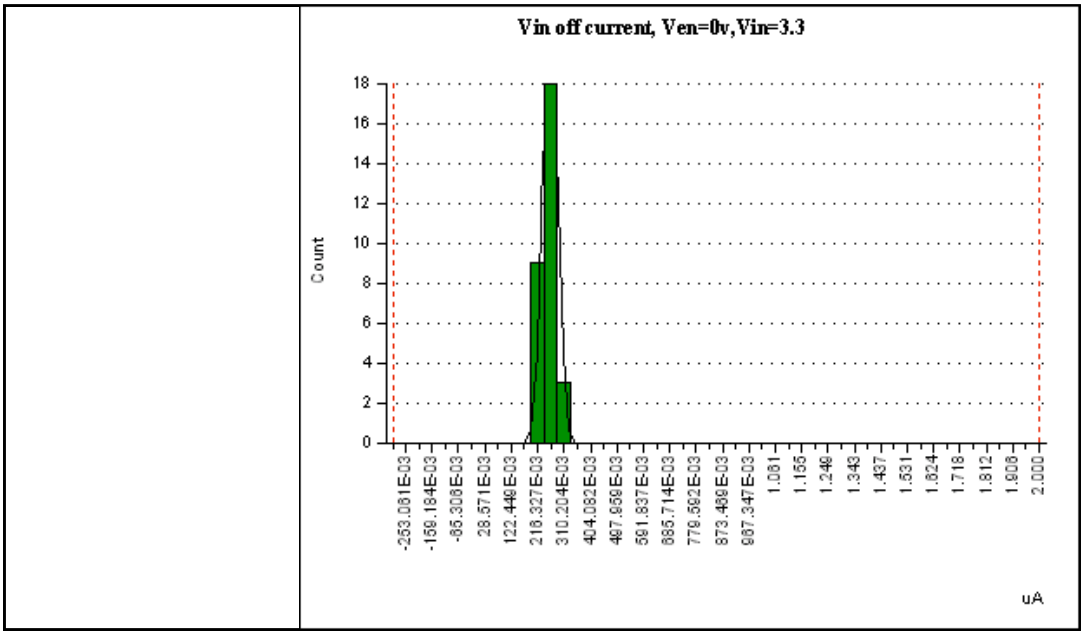
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (uA)

Min	210.000E-03	**StatLow**	N/A
Max	320.000E-03	**NWithinSpec**	30
Mean	252.000E-03	**NOutsideSpec**	0
StdDev	25.918E-03	**90%**	285.000E-03
25%	230.000E-03	**Range**	110.000E-03
Mean+3*StdDev	329.753E-03	**NOutsideSpec**	0
Mean-3*StdDev	174.247E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.4263	**Cpu**	>4.0000
StatHigh	N/A		

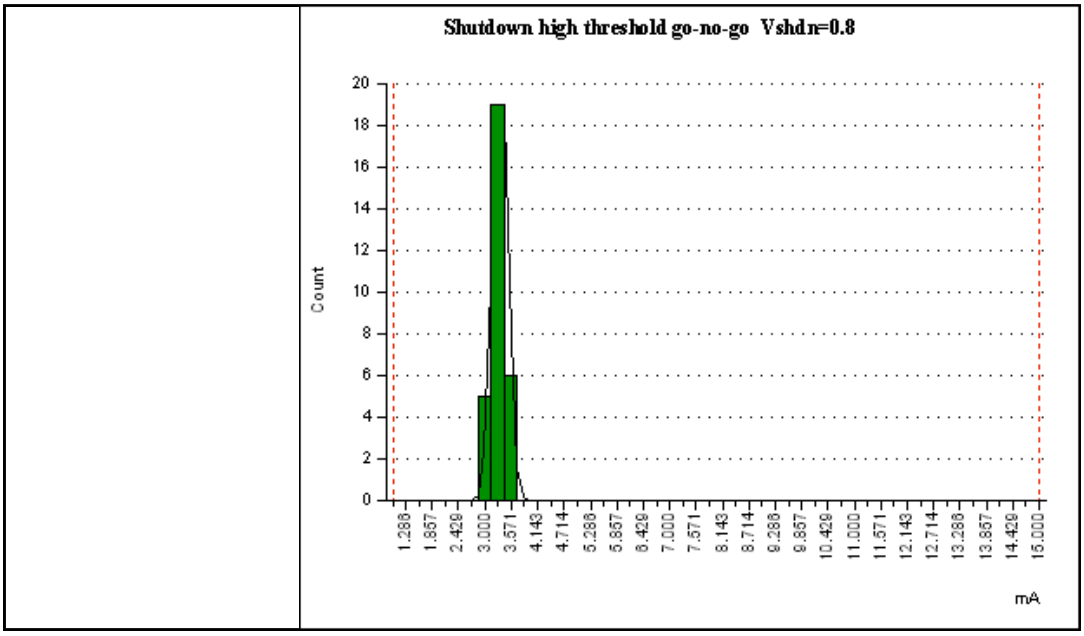
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (mA)

Min	2.934	**StatLow**	N/A
Max	3.622	**NWithinSpec**	30
Mean	3.294	**NOutsideSpec**	0
StdDev	160.621E-03	**90%**	3.526
25%	3.181	**Range**	688.000E-03
Mean+3*StdDev	3.776	**NOutsideSpec**	0
Mean-3*StdDev	2.812	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.0507	**Cpu**	>4.0000
StatHigh	N/A		

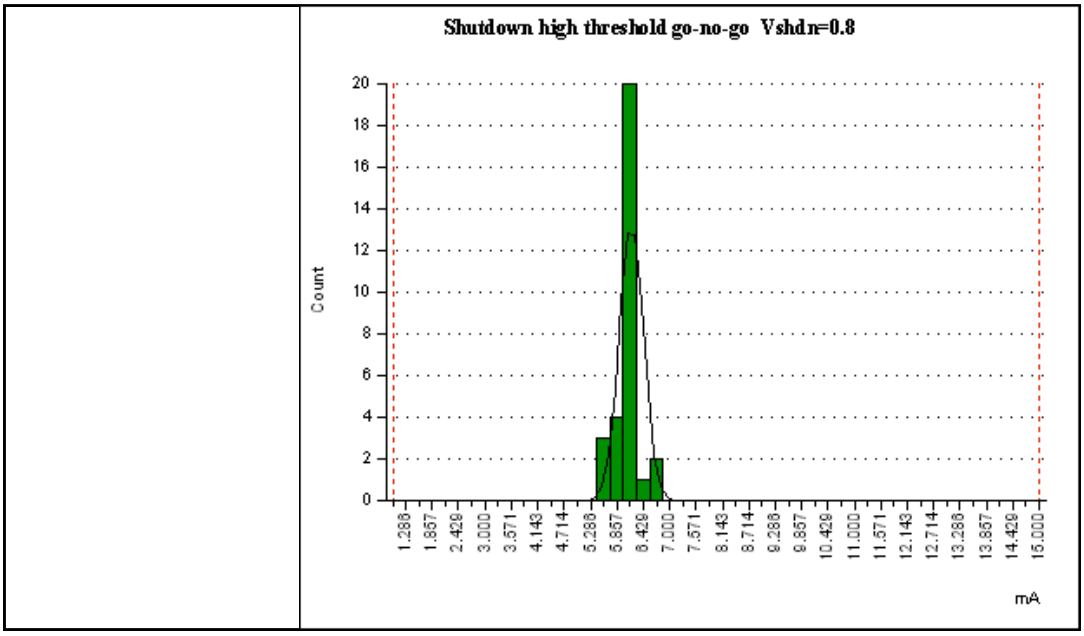
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (mA)

Min	5.696	**StatLow**	N/A
Max	6.822	**NWithinSpec**	30
Mean	6.107	**NOutsideSpec**	0
StdDev	258.049E-03	**90%**	6.401
25%	6.009	**Range**	1.126
Mean+3*StdDev	6.882	**NOutsideSpec**	0
		Cp	>4.0000
Mean-3*StdDev	5.333	**Cpl**	>4.0000
Cpk	>4.0000	**Cpu**	>4.0000
Skew	1.0104		
StatHigh	N/A		

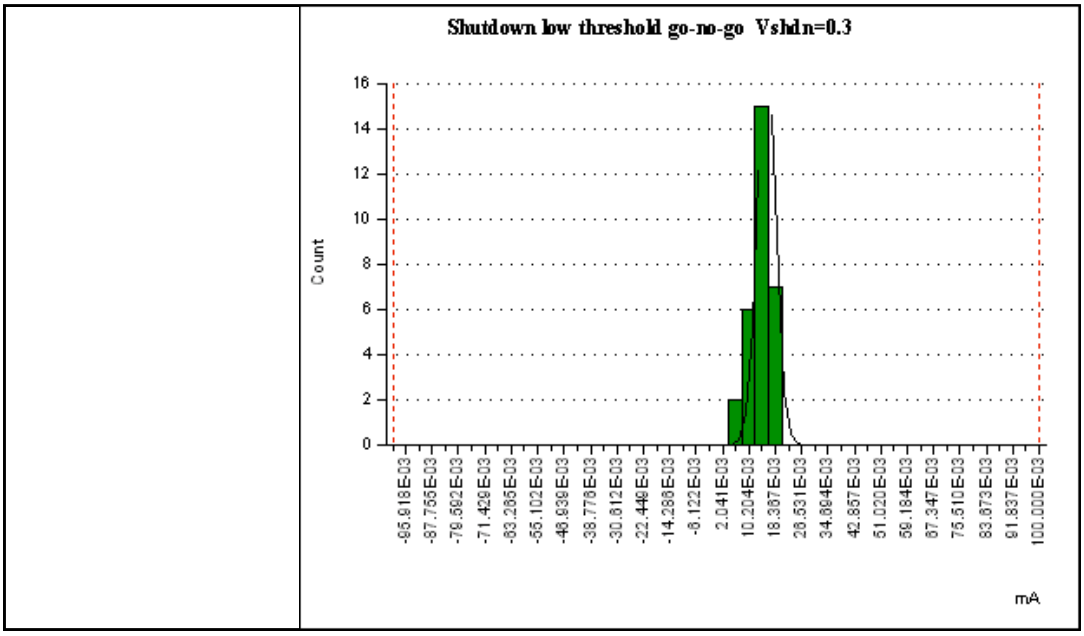
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (mA)

Min	7.000E-03	**StatLow**	N/A
Max	19.000E-03	**NWithinSpec**	30
Mean	14.367E-03	**NOutsideSpec**	0
StdDev	2.822E-03	**90%**	17.500E-03
25%	12.000E-03	**Range**	12.000E-03
Mean+3*StdDev	22.833E-03	**NOutsideSpec**	0
Mean-3*StdDev	5.900E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.7077	**Cpu**	>4.0000
StatHigh	N/A		

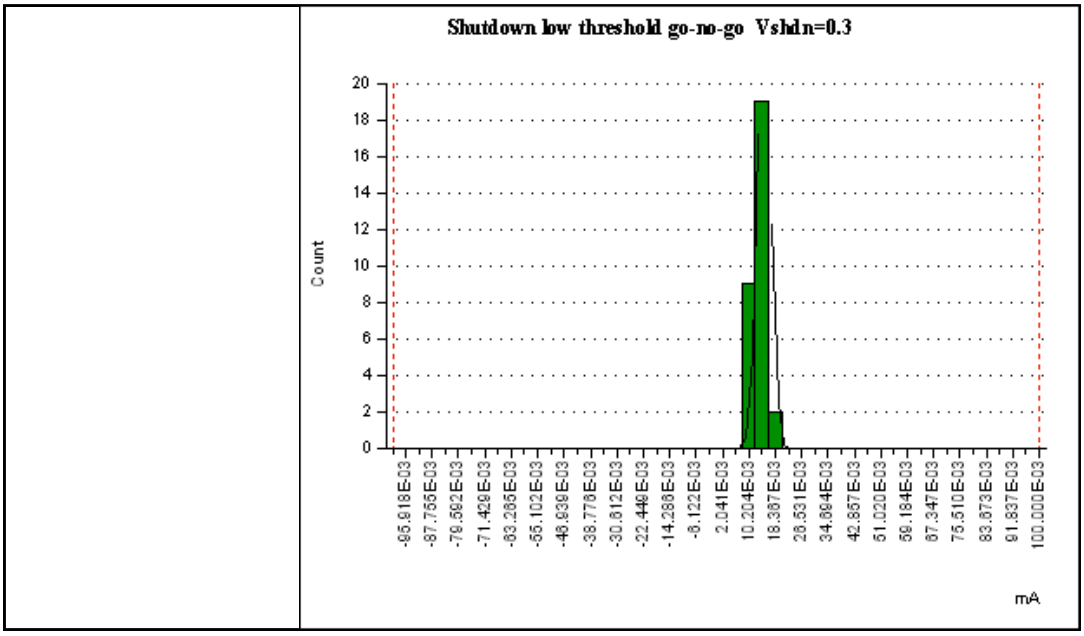
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (mA)

Min	10.000E-03	**StatLow**	N/A
Max	19.000E-03	**NWithinSpec**	30
Mean	13.633E-03	**NOutsideSpec**	0
StdDev	2.076E-03	**90%**	16.000E-03
25%	12.000E-03	**Range**	9.000E-03
Mean+3*StdDev	19.861E-03	**NOutsideSpec**	0
Mean-3*StdDev	7.406E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.4789	**Cpu**	>4.0000
StatHigh	N/A		

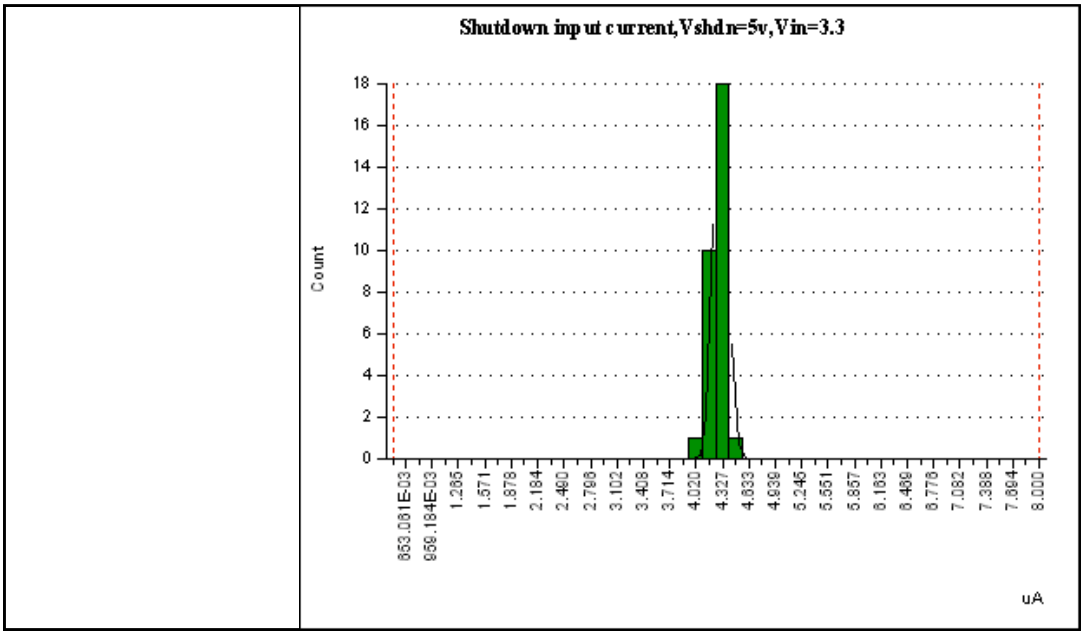
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (uA)

Min	4.080	**StatLow**	N/A
Max	4.410	**NWithinSpec**	30
Mean	4.269	**NOutsideSpec**	0
StdDev	76.309E-03	**90%**	4.375
25%	4.230	**Range**	330.000E-03
Mean+3*StdDev	4.498	**NOutsideSpec**	0
		Cp	>4.0000
Mean-3*StdDev	4.040	**Cpl**	>4.0000
Cpk	>4.0000	**Cpu**	>4.0000
Skew	-0.2844		
StatHigh	N/A		

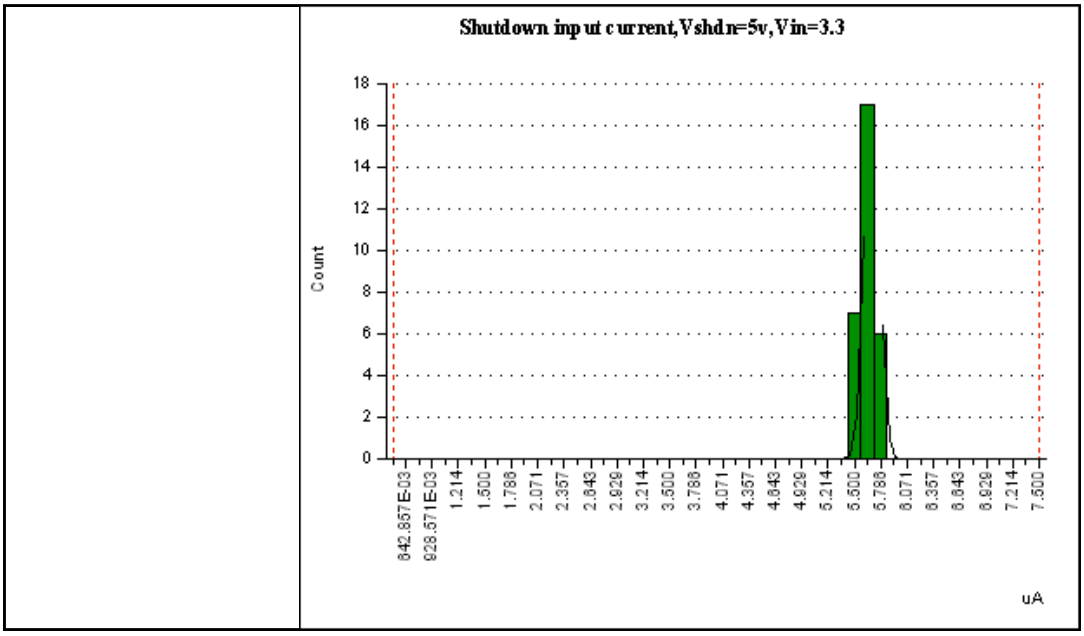
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (uA)

Min	5.540	**StatLow**	N/A
Max	5.810	**NWithinSpec**	30
Mean	5.632	**NOutsideSpec**	0
StdDev	73.597E-03	**90%**	5.750
25%	5.580	**Range**	270.000E-03
Mean+3*StdDev	5.853	**NOutsideSpec**	0
Mean-3*StdDev	5.411	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.9403	**Cpu**	>4.0000
StatHigh	N/A		

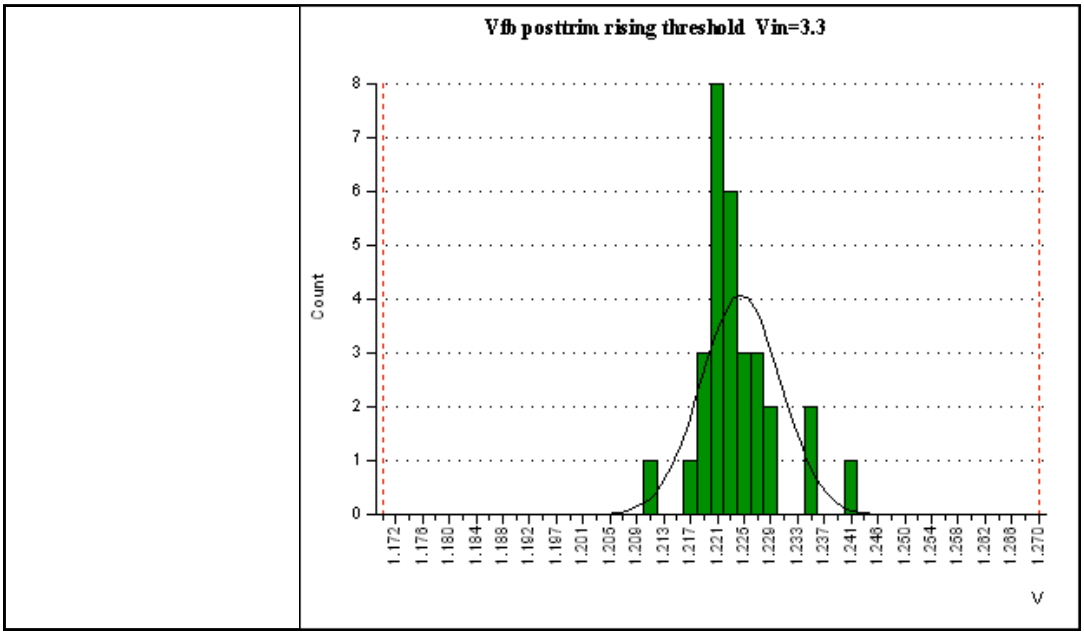
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (V)

Min	1.211	**StatLow**	N/A
Max	1.241	**NWithinSpec**	30
Mean	1.224	**NOutsideSpec**	0
StdDev	5.986E-03	**90%**	1.232
25%	1.221	**Range**	30.000E-03
Mean+3*StdDev	1.242	**NOutsideSpec**	0
Mean-3*StdDev	1.206	**Cp**	2.7845
Cpk	2.5636	**Cpl**	3.0054
Skew	0.8871	**Cpu**	2.5636
StatHigh	N/A		

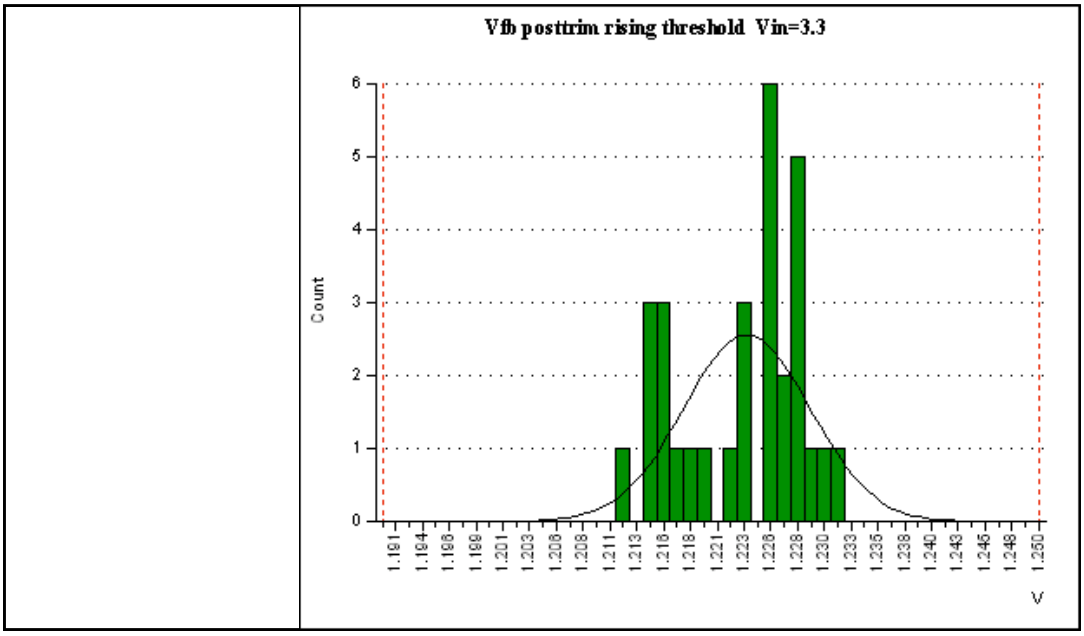
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (V)

Min	1.212	**StatLow**	N/A
Max	1.232	**NWithinSpec**	30
Mean	1.223	**NOutsideSpec**	0
StdDev	5.735E-03	**90%**	1.228
25%	1.217	**Range**	20.000E-03
Mean+3*StdDev	1.240	**NOutsideSpec**	0
		Cp	1.7436
Mean-3*StdDev	1.206	**Cpl**	1.9141
		Cpu	1.5731
Cpk	1.5731		
Skew	-0.4331		
StatHigh	N/A		

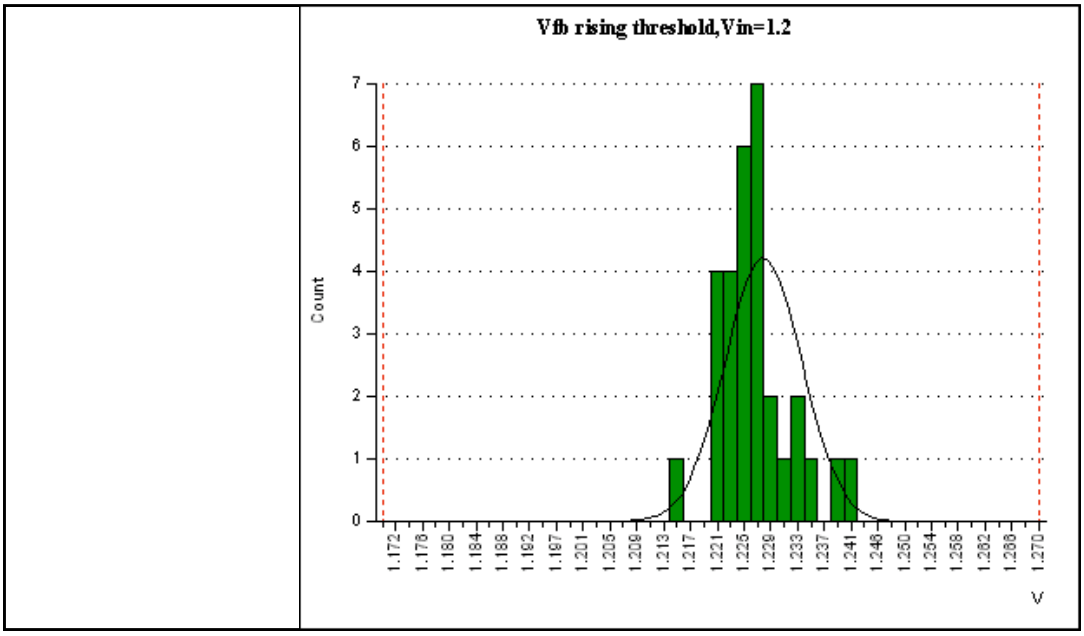
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (V)

Min	1.214	**StatLow**	N/A
Max	1.242	**NWithinSpec**	30
Mean	1.227	**NOutsideSpec**	0
StdDev	5.786E-03	**90%**	1.235
25%	1.224	**Range**	28.000E-03
Mean+3*StdDev	1.245	**NOutsideSpec**	0
Mean-3*StdDev	1.210	**Cp**	2.8804
Cpk	2.4560	**Cpl**	3.3047
Skew	0.5316	**Cpu**	2.4560
StatHigh	N/A		

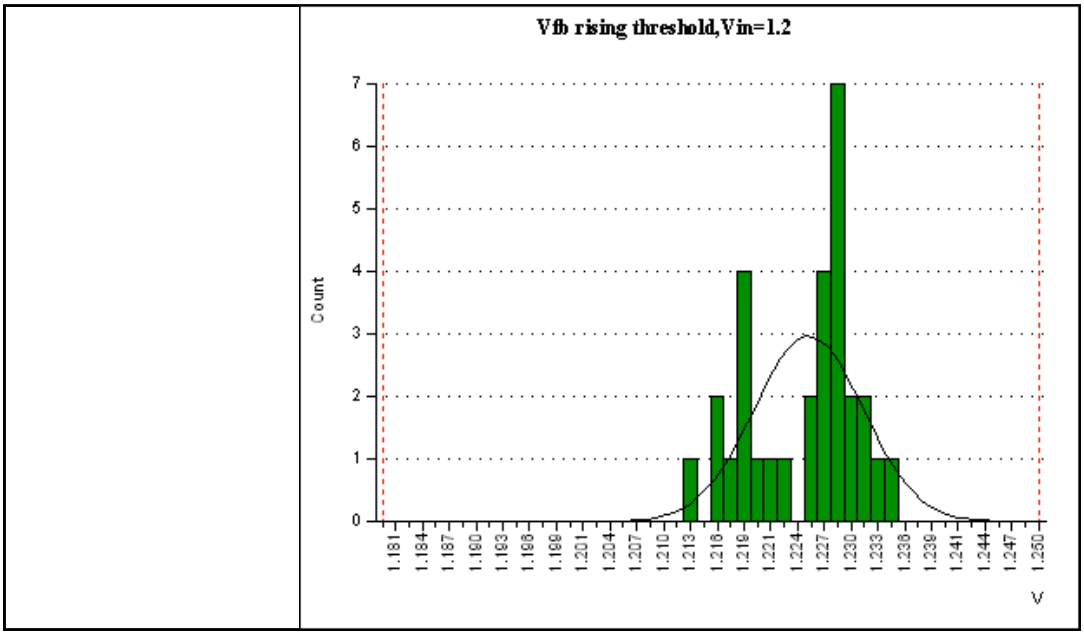
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (V)

Min	1.213	**StatLow**	N/A
Max	1.234	**NWithinSpec**	30
Mean	1.225	**NOutsideSpec**	0
StdDev	5.771E-03	**90%**	1.231
25%	1.219	**Range**	21.000E-03
Mean+3*StdDev	1.242	**NOutsideSpec**	0
		Cp	2.0216
Mean-3*StdDev	1.208	**Cpl**	2.5953
		Cpu	1.4478
Cpk	1.4478		
Skew	-0.5134		
StatHigh	N/A		

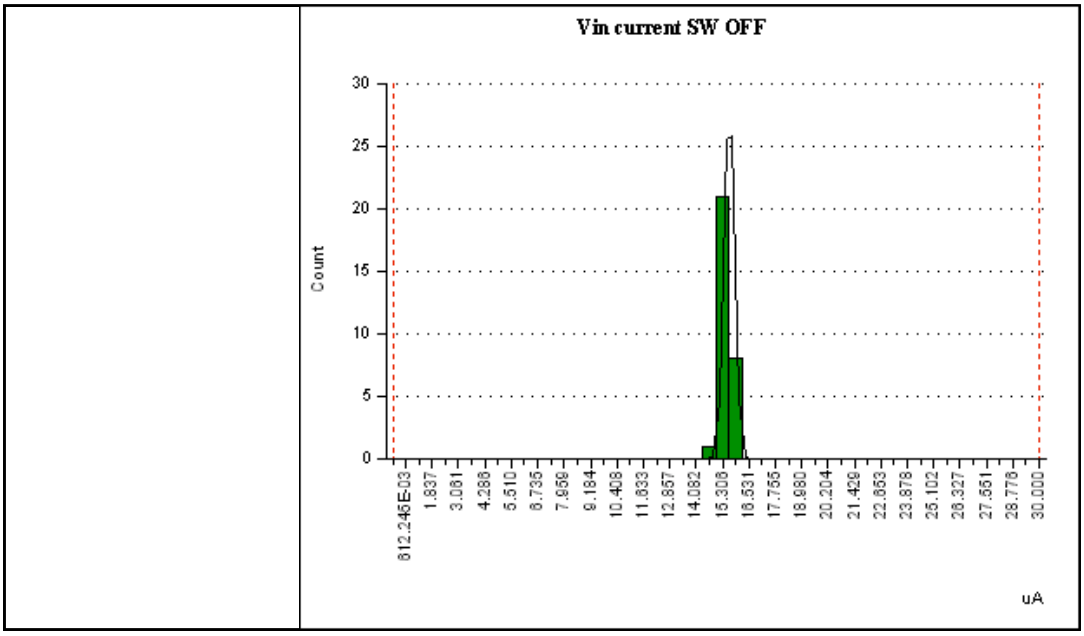
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (uA)

Min	14.800	**StatLow**	N/A
Max	15.780	**NWithinSpec**	30
Mean	15.452	**NOutsideSpec**	0
StdDev	230.981E-03	**90%**	15.740
25%	15.330	**Range**	980.000E-03
Mean+3*StdDev	16.145	**NOutsideSpec**	0
Mean-3*StdDev	14.759	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.7060	**Cpu**	>4.0000
StatHigh	N/A		

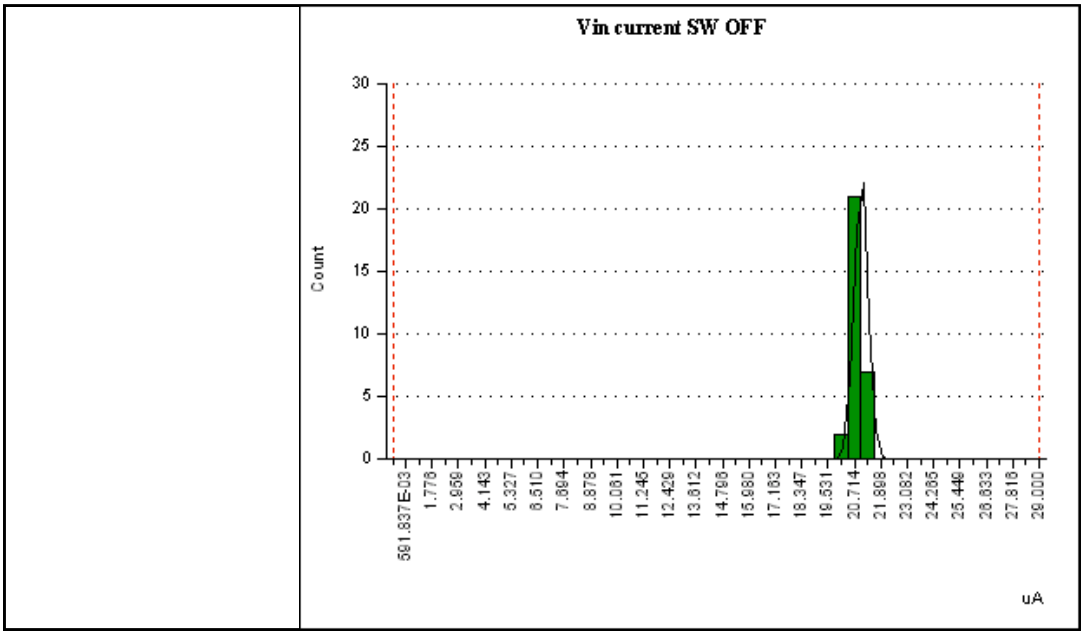
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (uA)

Min	20.210	**StatLow**	N/A
Max	21.440	**NWithinSpec**	30
Mean	20.796	**NOutsideSpec**	0
StdDev	309.322E-03	**90%**	21.295
25%	20.570	**Range**	1.230
Mean+3*StdDev	21.724	**NOutsideSpec**	0
Mean-3*StdDev	19.868	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.5751	**Cpu**	>4.0000
StatHigh	N/A		

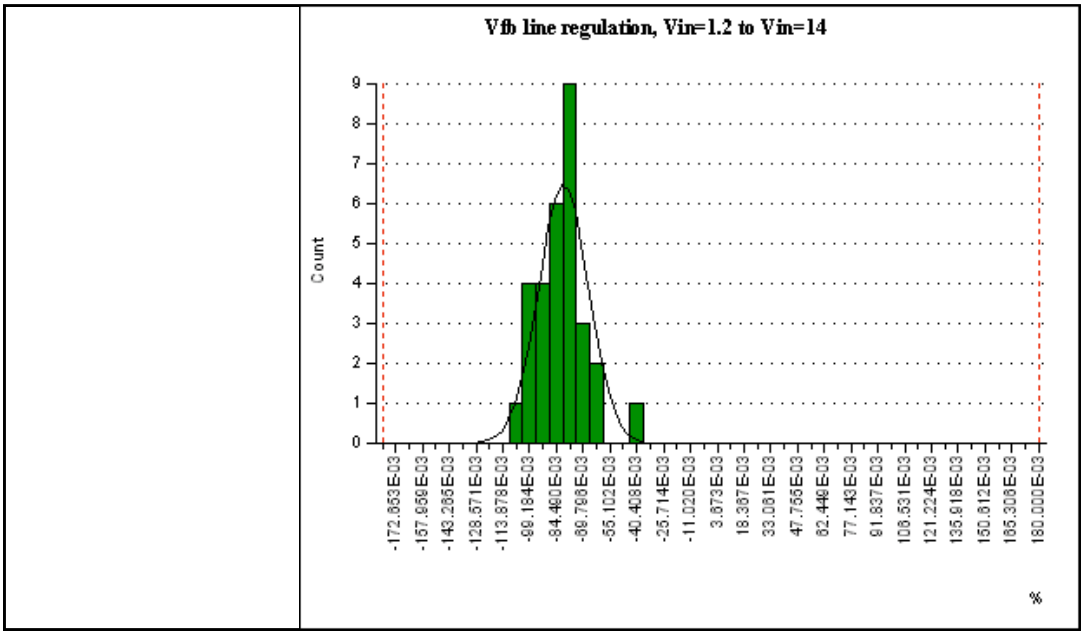
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (%)

Min	-105.000E-03	**StatLow**	N/A
Max	-38.000E-03	**NWithinSpec**	30
Mean	-81.867E-03	**NOutsideSpec**	0
StdDev	13.572E-03	**90%**	-65.500E-03
25%	-89.000E-03	**Range**	67.000E-03
Mean+3*StdDev	-41.152E-03	**NOutsideSpec**	0
Mean-3*StdDev	-122.581E-03	**Cp**	>4.0000
Cpk	2.4103	**Cpl**	2.4103
Skew	0.9609	**Cpu**	>4.0000
StatHigh	N/A		

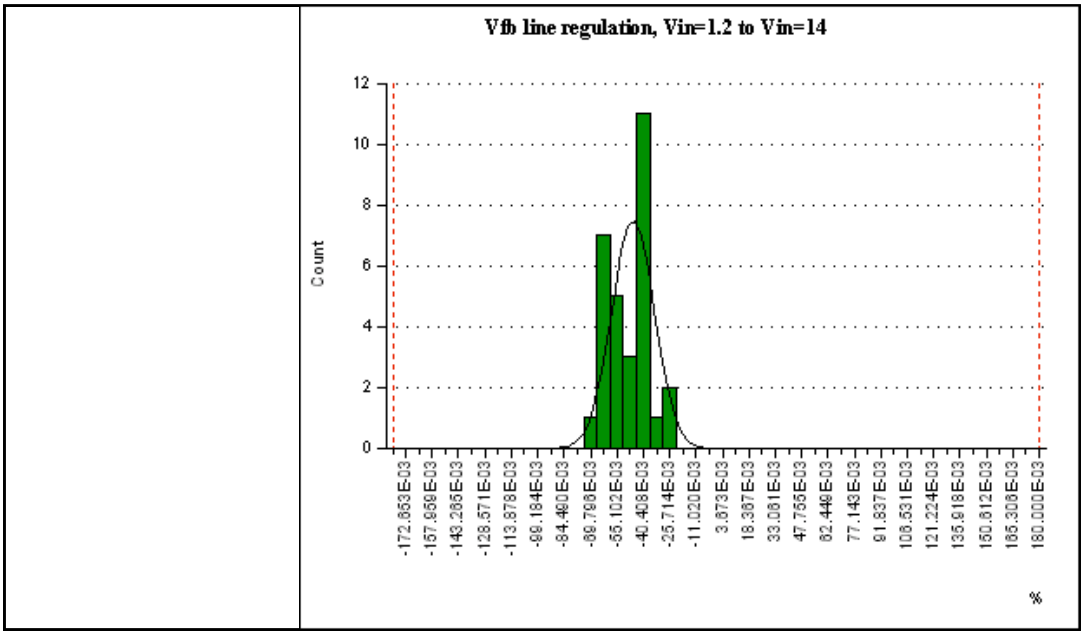
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (%)

Min	-67.000E-03	**StatLow**	N/A
Max	-28.000E-03	**NWithinSpec**	30
Mean	-47.767E-03	**NOutsideSpec**	0
StdDev	11.676E-03	**90%**	-36.500E-03
25%	-59.000E-03	**Range**	39.000E-03
Mean+3*StdDev	-12.739E-03	**NOutsideSpec**	0
Mean-3*StdDev	-82.794E-03	**Cp**	>4.0000
Cpk	3.7752	**Cpl**	3.7752
Skew	-0.1162	**Cpu**	>4.0000
StatHigh	N/A		

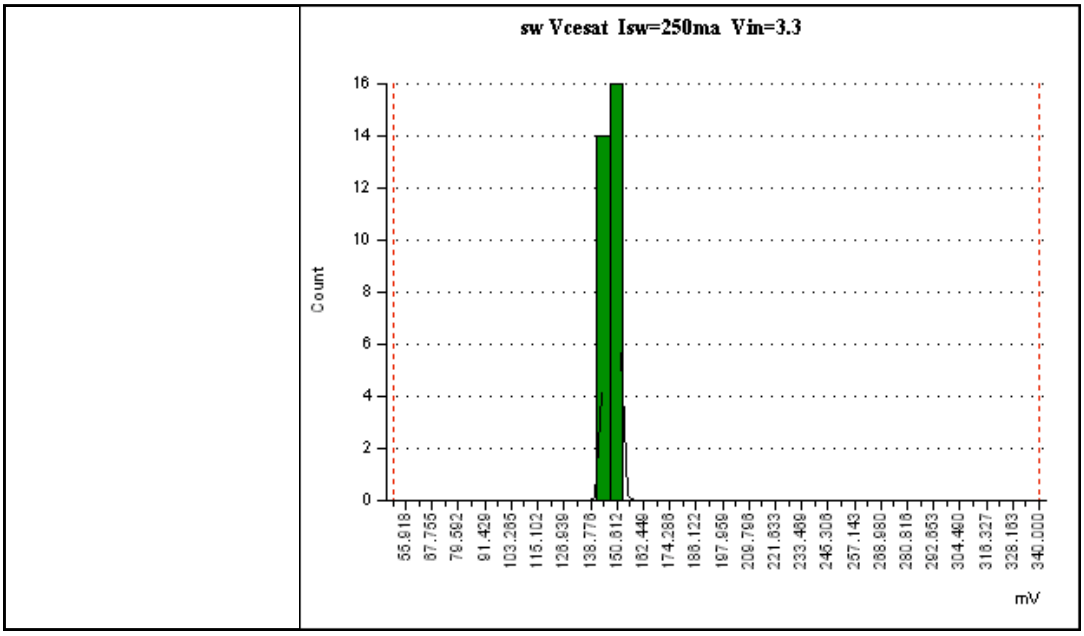
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (mV)

Min	143.000	**StatLow**	N/A
Max	152.000	**NWithinSpec**	30
Mean	147.333	**NOutsideSpec**	0
StdDev	2.249	**90%**	149.500
25%	146.000	**Range**	9.000
Mean+3*StdDev	154.080	**NOutsideSpec**	0
Mean-3*StdDev	140.587	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.1747	**Cpu**	>4.0000
StatHigh	N/A		

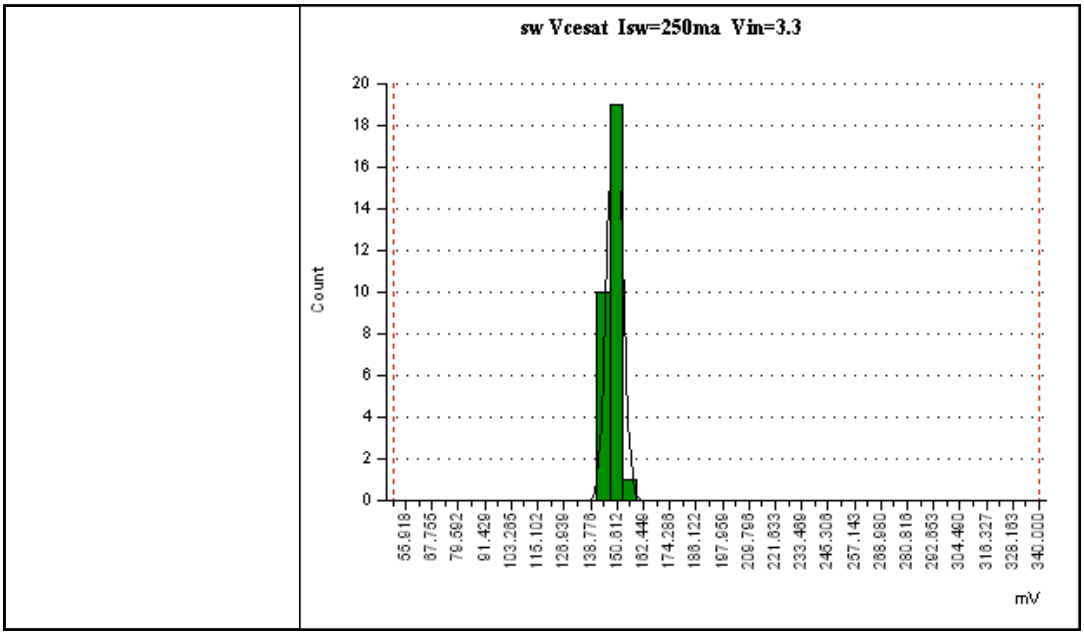
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (mV)

Min	143.000	**StatLow**	N/A
Max	154.000	**NWithinSpec**	30
Mean	148.600	**NOutsideSpec**	0
StdDev	3.013	**90%**	152.000
25%	147.000	**Range**	11.000
Mean+3*StdDev	157.638	**NOutsideSpec**	0
Mean-3*StdDev	139.562	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	-0.3976	**Cpu**	>4.0000
StatHigh	N/A		

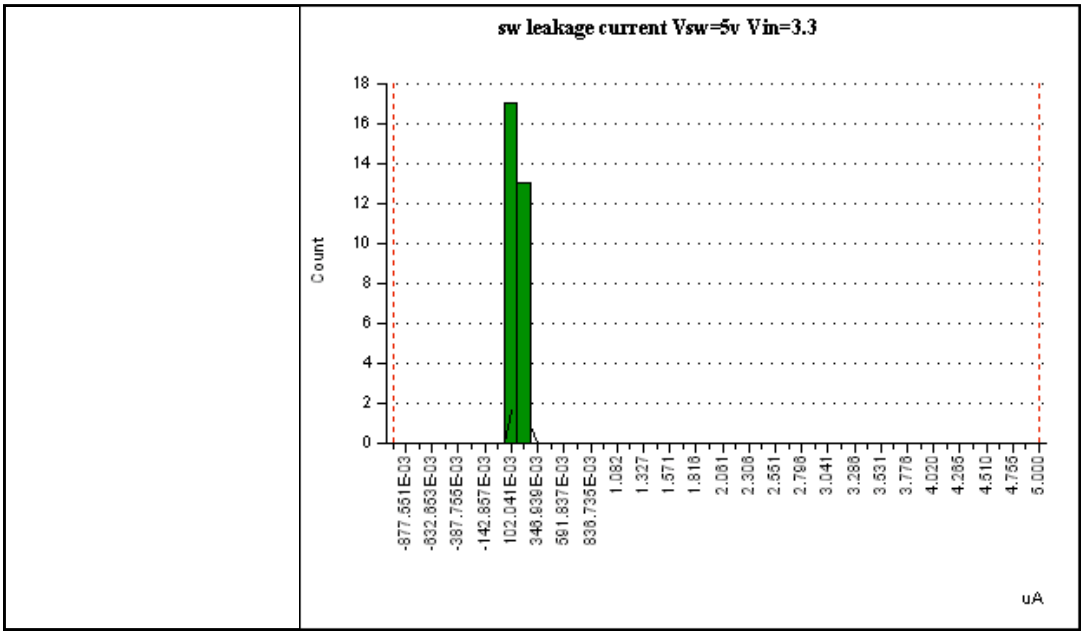
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data



Statistics: (uA)

Min	110.000E-03	**StatLow**	N/A
Max	240.000E-03	**NWithinSpec**	30
Mean	165.667E-03	**NOutsideSpec**	0
StdDev	33.598E-03	**90%**	215.000E-03
25%	140.000E-03	**Range**	130.000E-03
Mean+3*StdDev	266.462E-03	**NOutsideSpec**	0
Mean-3*StdDev	64.872E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.3867	**Cpu**	>4.0000
StatHigh	N/A		

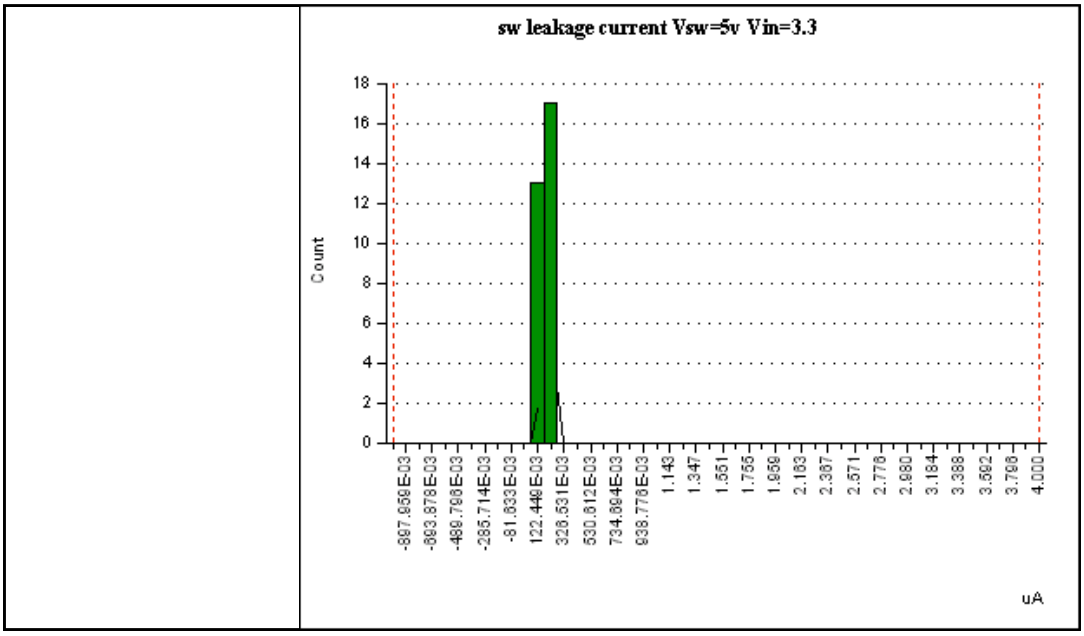
Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
SILANCA10028C HARROOM: N/A	MS1136	SP6690	_	char	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

TEMP
25C

Data: Raw Data



Statistics: (uA)

Min	120.000E-03	**StatLow**	N/A
Max	240.000E-03	**NWithinSpec**	30
Mean	178.667E-03	**NOutsideSpec**	0
StdDev	31.484E-03	**90%**	225.000E-03
25%	150.000E-03	**Range**	120.000E-03
Mean+3*StdDev	273.120E-03	**NOutsideSpec**	0
Mean-3*StdDev	84.214E-03	**Cp**	>4.0000
Cpk	>4.0000	**Cpl**	>4.0000
Skew	0.1670	**Cpu**	>4.0000
StatHigh	N/A		

Attributes

Lot: Wafers	Maskset ID	Device	Device Rev	Operation	Foundry	Process	Date Tested	Tester	Test Program	Sequence	Retest
HVA98662ROOM: N/A	MS1136	SP6690	_	CHAR	Hillview	N/A	06-NOV-2006	ETS500D	SP6690_SINGLE_FT_00.11/06/2006	-	0

Conditions

temp
25

Data: Raw Data

Reliability and Qualification Report

Silan BP1 Process Reliability Qualification using the SPX1117

Prepared By: Salvador Wu & Greg West
QA Engineering
Date: September 15, 2006

Reviewed By: Fred Claussen
VP Quality & Reliability
Date: September 15, 2006

Table Of Contents

Device Description:

The SPX1117 is a low power positive-voltage regulator designed to satisfy moderate power requirements with a cost effective, small footprint solution. This device is an excellent choice for use in battery-powered applications and portable computers. The SPX1117 features very low quiescent current and a low dropout voltage of 1.1V at a full load. As output current decreases, quiescent current flows into the load, increasing efficiency. SPX1117 is available in adjustable or fixed 1.5V, 1.8V, 2.5V,2.5V, 2.85V, 3.0V, 3.3V and 5V output voltages.

The SPX1117 is offered in several 3-pin surface mount packages: SOT-223, TO-252, TO-220 and TO-263. An output capacitor of 10µF provides unconditional stability while a smaller 2.2µF capacitor is sufficient for most applications.

Manufacturing Information:

Product: SPX1117 BP1 Products

Description: 800mA LDO

Mask Set: MS1557 AY

Lot Number(s): SPXBP10C010TC, SPXBP1C011TC, SPXBP1C014TC

Process: silan-bp1

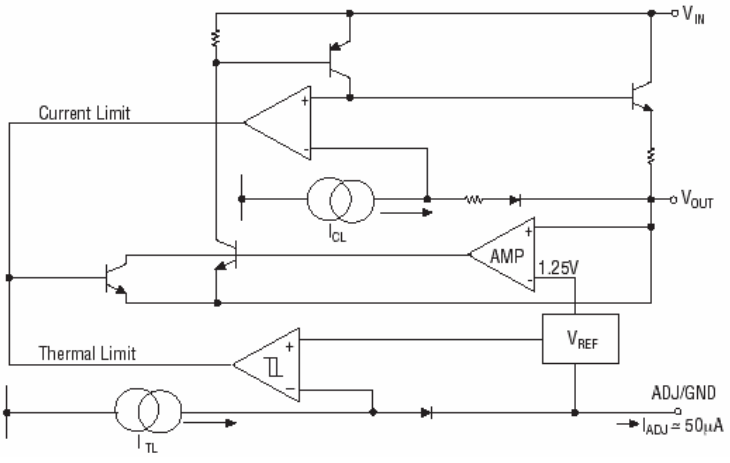
Wafer Fab: Silan

Package Information:

Package Type: SOT 223

Package Code:: JEDEC

PIN OUT SPX1117



Reliability Qualification Test Summary:

Stress Level	Device	Lot Number	Burn-In Temp	Sample Size	No. Fail
168Hrs	SPX1117	SPXBP10C0 10TC	125 °C	77	0
168Hrs	SPX1117	SPXBP1C01 1TC	125 °C	77	0
168Hrs	SPX1117	SPXBP1C01 4TC	125 °C	77	0
1000Hrs	SPX1117	SPXBP10C0 10TC	125 °C	77	0
1000Hrs	SPX1117	SPXBP1C01 1TC	125 °C	77	0
1000Hrs	SPX1117	SPXBP1C01 4TC	125 °C	77	0

Life Test

Life testing is conducted to determine if there are any fundamental reliability related failure mechanism(s) present in the device.

These failure mechanisms can be divided roughly into four groups:

1. Process or die related failures such as oxide defects, metallization defects, and diffusion defects.
2. Assembly related failures such as chip mount defects, wire bond defects, molding defects, and trim/form/singulation defects.
3. Design related defects.
4. Miscellaneous, undetermined, or application induced failures.

125C Operating Life Test Results

As part of the Sipex design qualification program, the Product/Reliability Engineering group subjected 231 parts to 168 hours and 1000 hours of 125° C life stress testing.

168 Hour Timepoint

The 231 parts were subjected to the life test profile and completed the stress with no failures.

1000 Hour Timepoint

231 parts were reintroduced to life stress testing, completing the 1000 hour HTOL time point without any failures or significant shifts in process parameters

FIT Rate Calculations

FIT rate (failures in time) is the predicted number of failures per billion device hours.

This predicted value is based upon,

- The Life Test conditions summarized in the HTOL table (time/temperature, device quantity, failure quantity).
- The Activation Energy (E_a) for potential failure modes. The weighted Activation Energy(E_a) of observed failure mechanisms for Sipex products has been determined to be 0.8eV.

Based on the above criteria SPX1117 product FIT rates for 25°, 55°, and 70°C of operation at 60% and 90% confidence levels have been calculated and listed below.

FIT Failure Rates: SPX1117 BP1 Silan Process

Confidence Level	+25°C	+55°C	+70°C
60%	1.9	28.7	94.5
90%	4.5	69.8	229.6

1 FIT = 1 Failure per Billion Device-Hours

MTBF Calculation: SPX1117 BP1 Silan Process

Confidence Level	+25°C	+55°C	+70°C
60%	5.37E+08	3.48E+07	1.06E+07
90%	2.21E+08	1.43E+07	4.36E+06

ESD Testing

Human Body Model ESD – 45 units were subjected to Human Body Model ESD testing at +/- 2KV. All units passed.

Machine Model ESD – 45 units were subjected to Human Body Model ESD testing at +/- 200V. All units passed.

Early Life Failure Rate Testing

Early Life Test – 600 units were subject to Early Life test. All units passed

Additional Reliability Tests

77 of the units were placed on Unbiased HAST testing, 77 of the units were placed on Thermal Shock testing, and 77 on -65C/+150C Temperature Cycle testing. All units passed testing as summarized in the following table.

Test	Condition	Time	Sample Size	# of rejects
TEMP. Cycles	-65C/+150C	500 Cycles	77	0
HAST Unbiased	130C/85%RH	96hrs	77	0
Thermal Shock	-65C/+150C	500 Cycles	77	0

Design Solution # 28

SP6691 2 Cell Alkaline to 4 WLEDs with I_{OUT} = 20mA

Date: June 21, 2006

Designed by: Brian Kennedy

Part Number: SP6691EK

Application Description: 2 Cell Boost to 13V - 14V out at 20mA

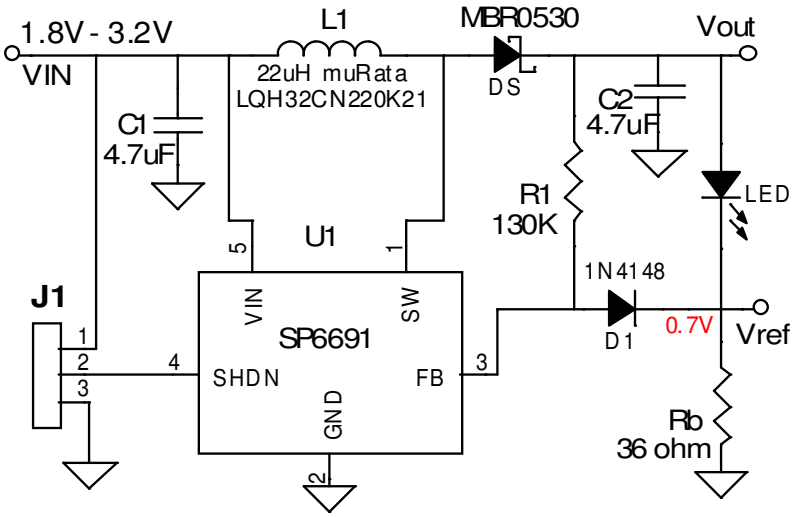
Electrical Requirements:

Input Voltage	1.8V to 3.2V
Output Voltage	13V to 14V
Output Current	20mA

Circuit Description:

This application has been designed for 2 cell alkaline battery inputs with 13V to 14V outputs driving White LEDs that require improved efficiency, small size and moderate output ripple. The input voltage range is from 1.8V to 3.2V and is boosted to a 13V to 14V output. All the external components have been optimized for an output current of approximately 20mA and have been laid out to optimize for small size and to increase efficiency.

This report includes the application schematic complete with component part numbers and figures 1-9 illustrating electrical performance of the design.



Application Schematic

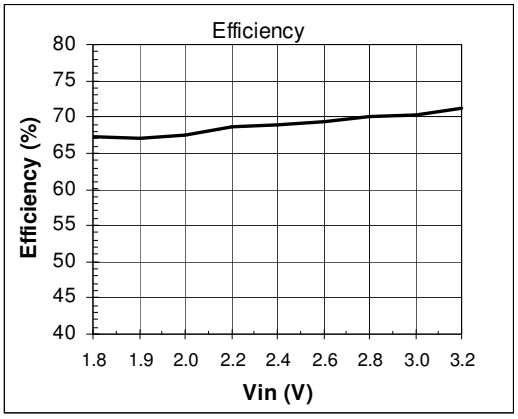


Figure 1: Efficiency Graph

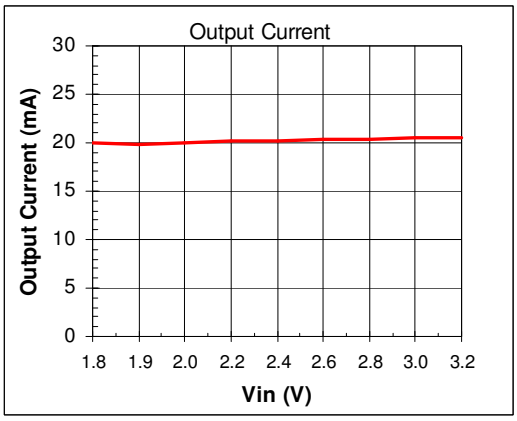


Figure 2: VOUT Regulation Graph

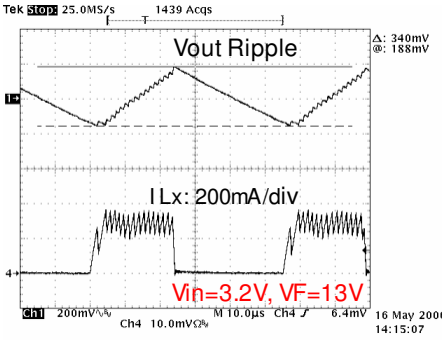


Figure 3: Output Ripple

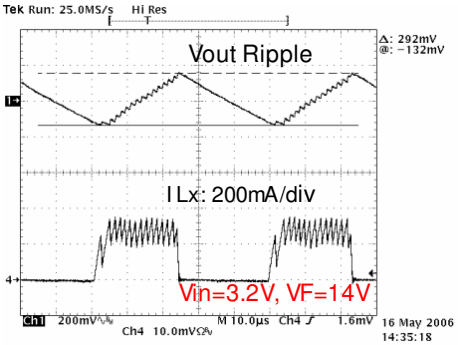


Figure 4: Output Ripple

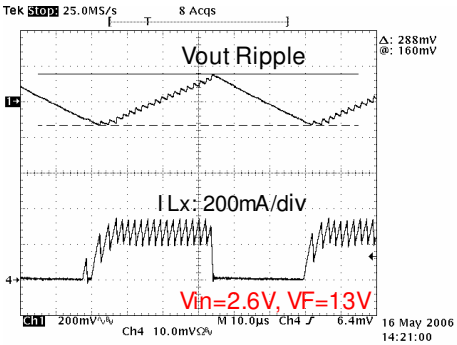


Figure 5: Output Ripple

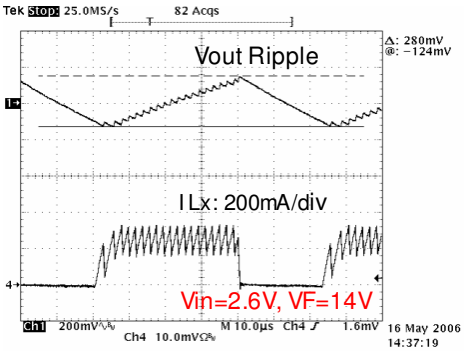


Figure 6: Output Ripple

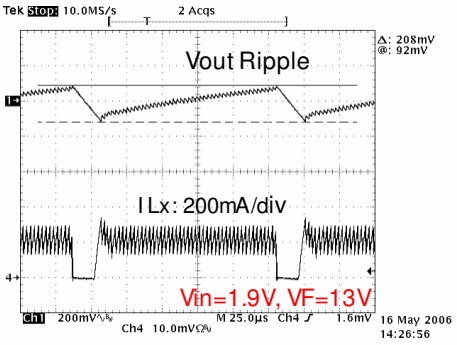


Figure 7: Output Ripple

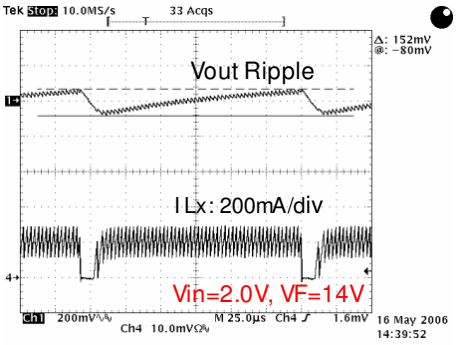


Figure 8: Output Ripple

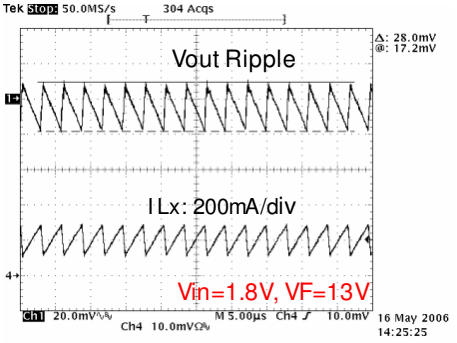


Figure 9: Output Ripple

Design Solution # 34

High Voltage Boost Regulator with Voltage Doubler

Date: Sept 19, 2006

Designed by: Matthew Szaniawski (mszaniawski@sipex.com)

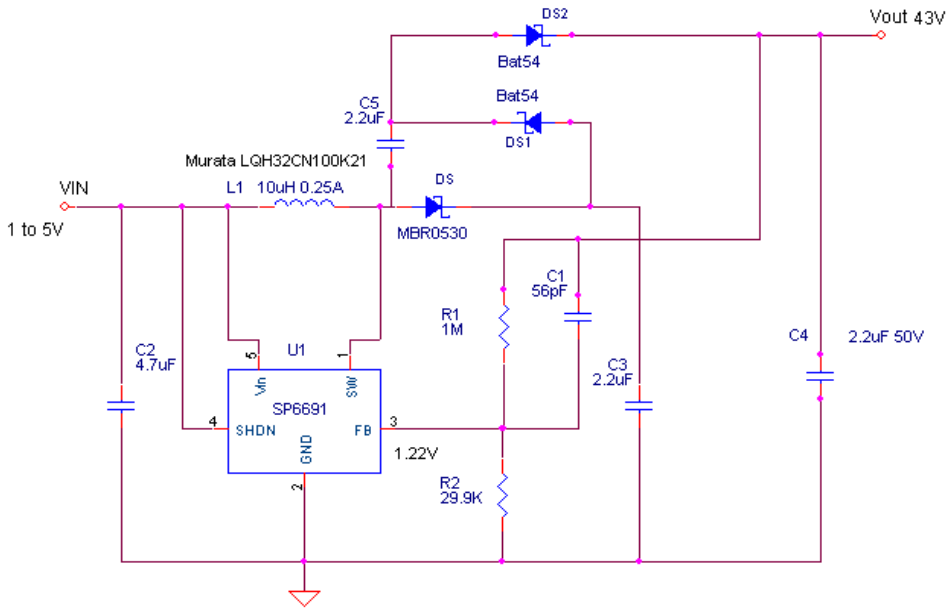
Part Number: SP6691

Application Description: High voltage boost regulator with charge pump voltage doubler

Electrical Requirements:

Input Voltage	1V to 5V
Output Voltage	up to 60V and 1/2VOUT (also available)
Output Current	1uA to 5mA

Circuit Description:
This circuit has been designed to provide a high output voltage with a lower voltage boost regulator by adding a charge pump circuit. This circuit can take a standard 34V boost regulator and make it a 68V boost regulator if needed. All of the testing was done on a VOUT of 43V to demonstrate circuit operation. The other benefit of this circuit is that at the voltage at capacitor C3 is roughly ½ of VOUT. This report includes application schematic, complete Bill of materials and figures 1 through 7 illustrating electrical performance of the design.



Schematic for SP6691@ 43VOUT

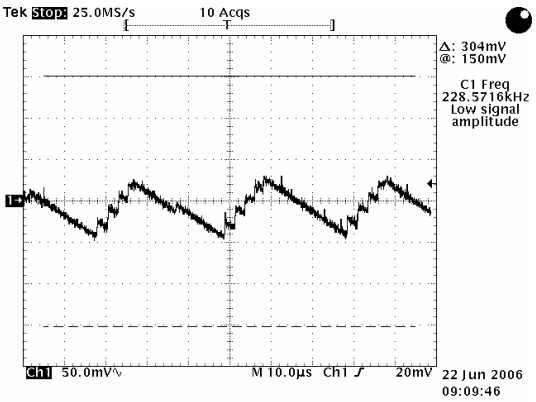


Figure 1. Typical VOUT Ripple at 2VIN and 43VOUT

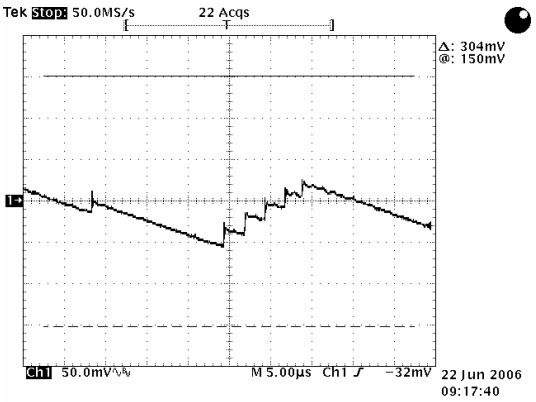


Figure 2. Typical VOUT Ripple at 3VIN and 43VOUT

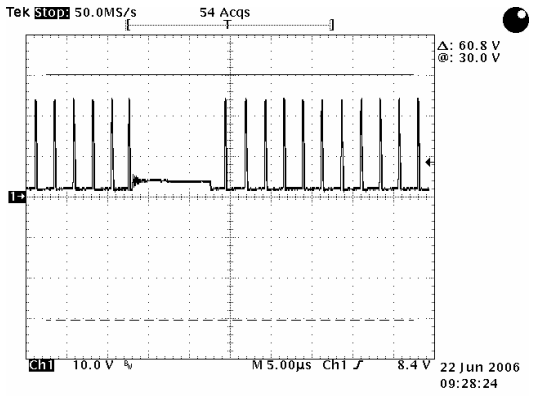


Figure 3. Switch node pin1 heavy load

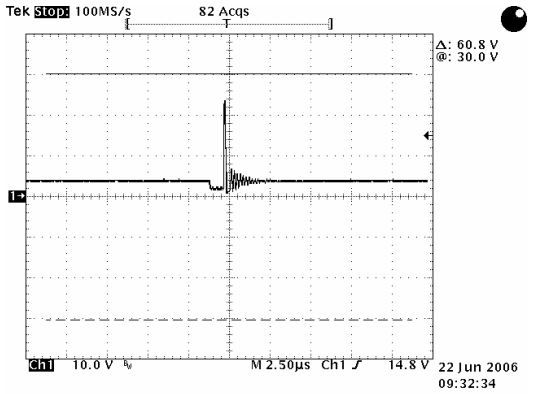


Figure 4. Switch node pin 1 no load

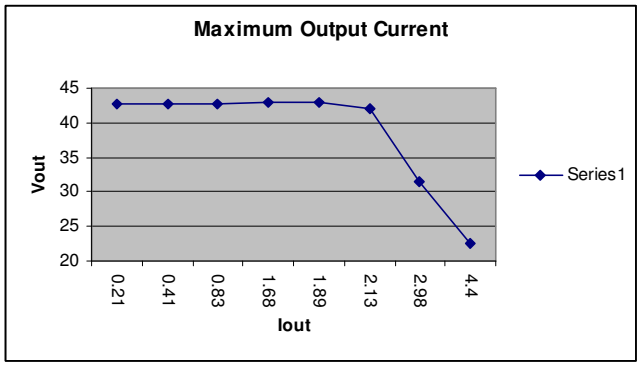


Figure 5. Maximum output current at 1V_{IN}

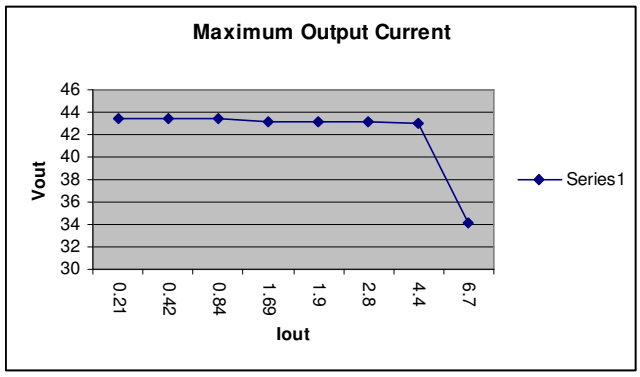


Figure 6. Maximum output current at 2V_{IN}

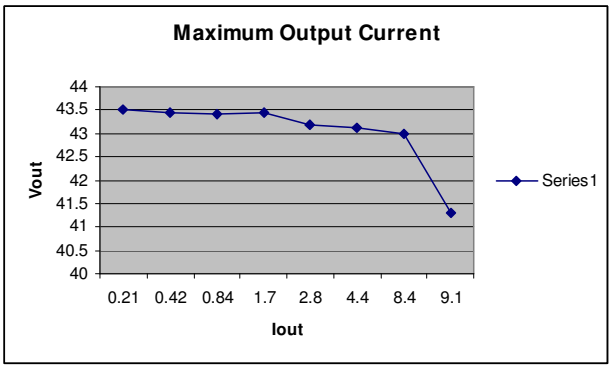


Figure 7. Maximum output current at 3V_{IN}

Evaluation List of Materials							3/3/2006
Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone Number
2	U1	1	Sipex	SP6691EK	SOT-23-5	Boost regulator	978-667-7800
3	DS	1	On Semi	MBR530	SOD-323	Schottky Diode	
4	L1	1	Murata	LQH32CN100K21	3.2X2.5X2mm	10uH Inductor	770-436-1300
5	C3 C4 C5	3	Murata	GRM43ER71H225K	1206	2.2uF Ceramic X7R 50V	770-436-1300
7	C1	1	Murata	GRM1885C1H560JA01B	603	56pF Capacitor	770-436-1300
8	DS1 DS2	1	Central Semi	BAT54C	SOT-23	Dual Diode Schottky	
9	R1	1	Panasonic	ERJ-3EKF1005V	0603	1M Ohm Thick Film Res 1%	800-344-4539
10	R2	1	Panasonic	ERJ-3EKF2992V	0603	29.9K Ohm Thick Film 1%Res 1%	800-344-4539
11	C4	1	Murata	GRM32RR71E225KC01B	1206	4.7uF capacitor	770-436-1300

Figure 8. Bill Of Materials

Design Solution #53

SP6691 : 12V input to 30V output at 40mA

Designed by: Brian Kennedy

Part Number: SP6691EK

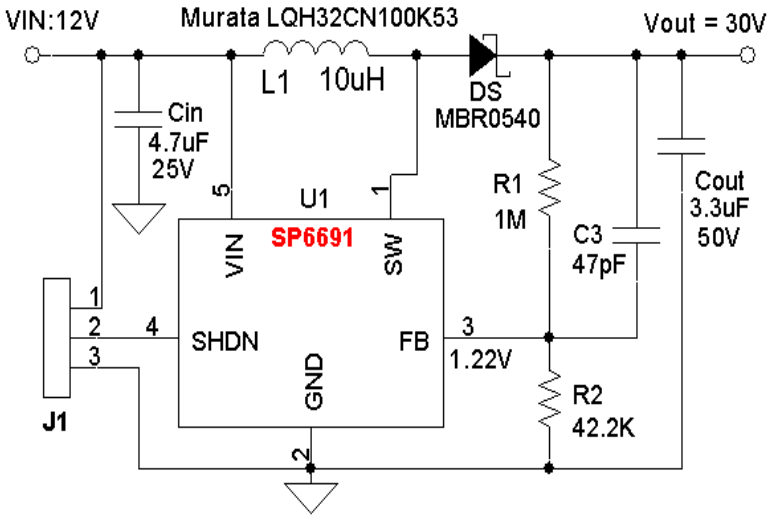
Application Description: 12V input to 30V output at 40mA

Electrical Requirements:

Input Voltage	12V
Output Voltage	30V
Output Current	40mA

Circuit Description:
This application has been designed for 12V input to 30V output at about 40mA load with low output ripple. The SP6691 is a DC/DC switching regulator that can boost from an input as high as 13.5V to an output up to 30V, using 10uH inductor , internal charge switch, external schottky diode and relatively small input and output capacitors. The SP6691 uses Pulse Frequency Modulation (PFM) control for low 20uA quiescent current and a simple comparator driven voltage mode output control that can work with ceramic, tantalum or electrolytic capacitors without any external compensation components needed. The results were a relatively low output ripple for the large 30V output level, which can be very useful for tuner or other low noise applications. To lower the ripple, an additional 3.3uF ceramic capacitor can be added to the output or if cost is more of a concern than size, a 22uF electrolytic can be added. This report includes data in figures 1-6 showing the input and output ripple for the various output capacitors added as well as efficiency data and BOM.

Schematic:



Vin	Iin	Vout	Iout	Ripple	Effi
(V)	(mA)	(V)	(mA)	(mV)	(%)
12.0	3.28	30.56	1.00	430	77.6
12.0	32.13	30.79	10.00	480	79.9
12.0	64.30	30.92	20.00	500	80.1
12.0	95	30.95	30.03	304	81.5
12.0	126	30.71	40.00	356	81.2

Table 1: Ripple & Efficiency Data

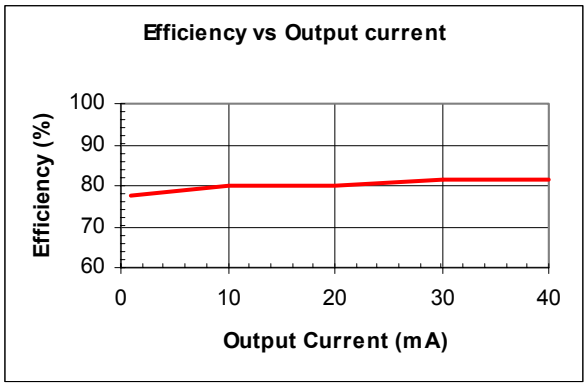


Figure 1: Efficiency Curve

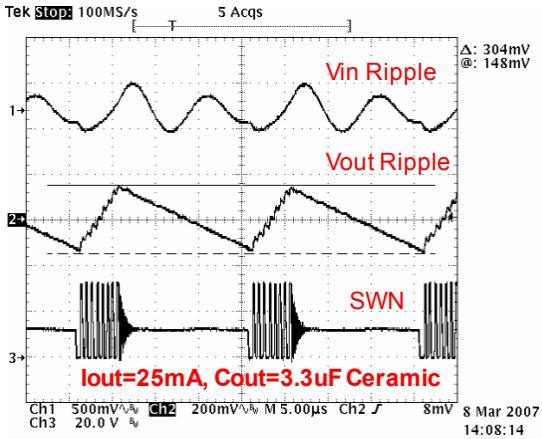


Figure 2. Ripple with 25mA load

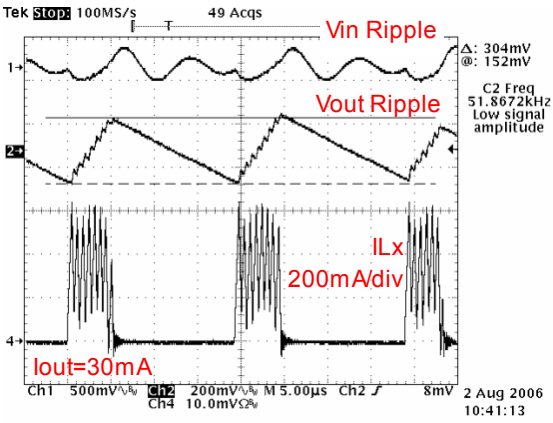


Figure 3. Ripple with 30mA Load

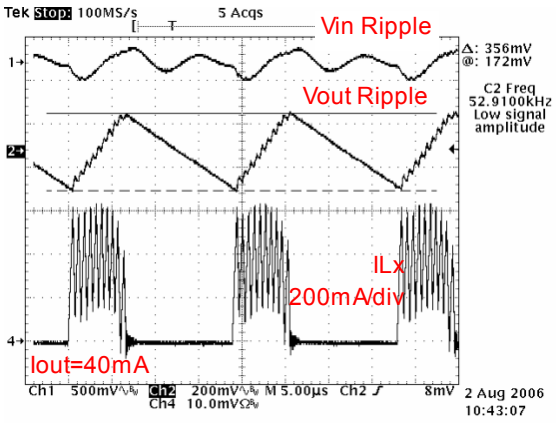


Figure 4. Ripple with 40mA Load

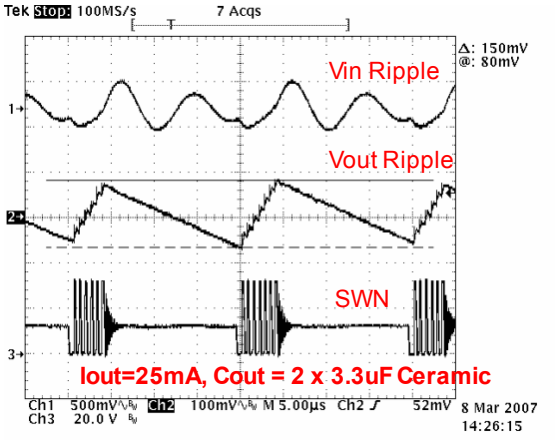


Figure 5. Ripple with Cout = 2 parallel 3.3uF Cer.

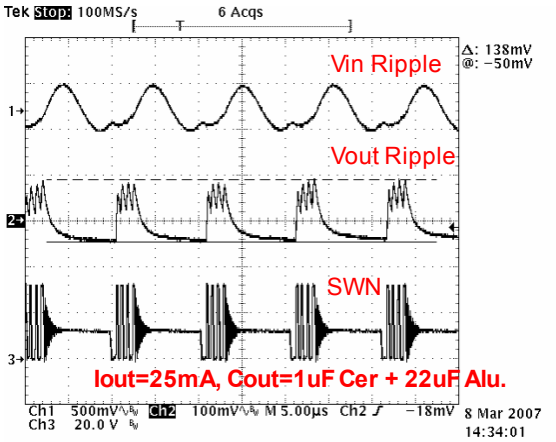


Figure 6. Ripple with Cout = 1uF cer. in parallel with 22uF Aluminum Electrolytic

Table 2. BOM

SP6691 Evaluation Board Rev. 00 List of Materials							3/23/07
Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone Number
2	U1	1	Sipex	SP6691EK	SOT-23-5	Boost regulator	408-934-7500
3	DS	1	On Semi	MBR540	SOD-323	Schottky Diode 0.5A 40V	
4	L1	1	Murata	LQH32CN100K21	3.2x2.5x1.55mm	10uH Inductor	770-436-1300
5	Cin	3	Murata	-	0805	4.7uF Ceramic X5R 25V	770-436-1300
7	C3	1	Murata	-	603	47pF Capacitor	770-436-1300
9	R1	1	Any	-	0603	1M Ohm Thick Film Res 1%	-
10	R2	1	Any	-	0603	42.2K Ohm Thick Film 1%Res 1%	-
11	COUT	1	TDK	-	1210	3.3uF X5R	-
11	COUT	1	TDK	-	1206	1uF X5R	-
11	COUT	1	Any	-	-	22uF Al El	-

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Sipex Application Notes:	http://www.sipex.com/applicationNotes.aspx

Sipex Corporation
Headquarters and
Sales Office
233 South Hillview Drive
Milpitas, CA95035
tel: (408) 934-7500
faX: (408) 935-7600

Design Solution # 59

SP6136: 12V input to 3.3V output at 15A

Designed by: Shahin Maloyan

Part Number: SP6136ER1

Application Description: 12V input to 3.3V output at 15mA

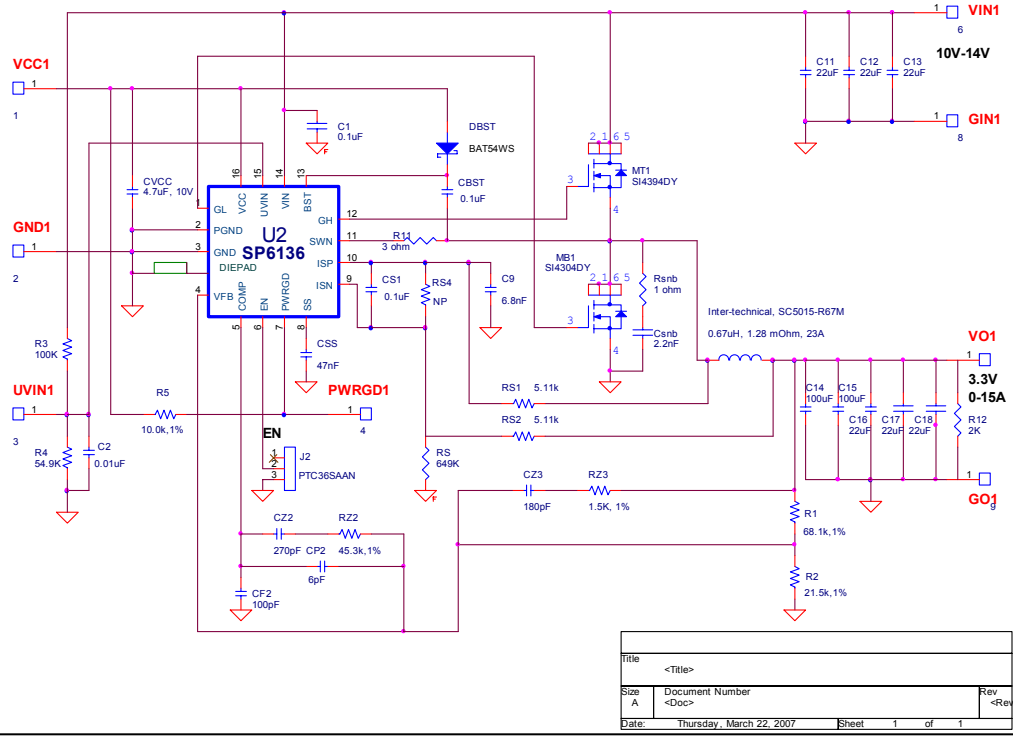
Electrical Requirements:

Input Voltage	12V
Output Voltage	3.3V
Output Current	15A
Step Load	60mV response to 15A step

Circuit Description:
This buck converter has been designed to provide 3.3V output at 15A with a low 60mV transient response to a 15A step. The SP6136 is a high performance buck regulator controller that provides all necessary functions required by a buck regulator: over-current protection, power-good output, adjustable UVLO and Enable input. High switching frequency (600kHz) minimizes solution cost and size.

This report includes the application schematic complete with component part numbers and figures 1-4 illustrating electrical performance of the design.

Schematic:



Vin (V)	Iin (A)	Vout (V)	Iout (A)	Efficiency(%)
12.000	0.098	3.335	0	
12.000	0.240	3.335	0.5	57.9
12.000	0.383	3.335	1	72.5
12.000	0.672	3.335	2	82.7
12.000	1.254	3.335	4	88.6
12.000	1.835	3.335	6	90.8
12.000	2.422	3.336	8	91.8
12.000	3.019	3.336	10	92
12.000	3.324	3.336	11	92
12.000	3.630	3.336	12	91.9
12.000	4.247	3.337	14	91.6
12.000	4.562	3.337	15	91.4

Table 1: Efficiency and regulation Data

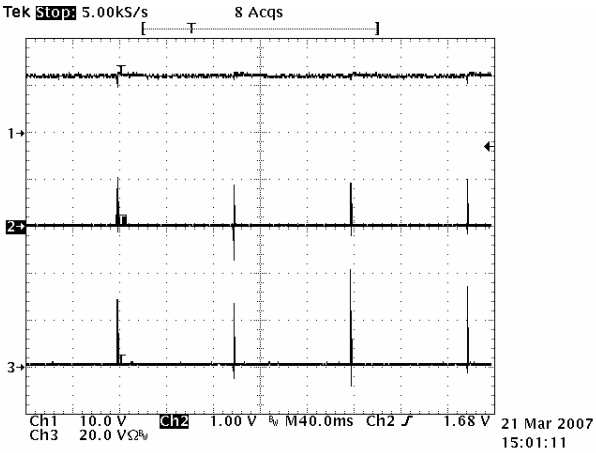


Figure 1: Hiccup at Overcurrent
Ch1: Vin, ch2: Vout, ch3: Iout

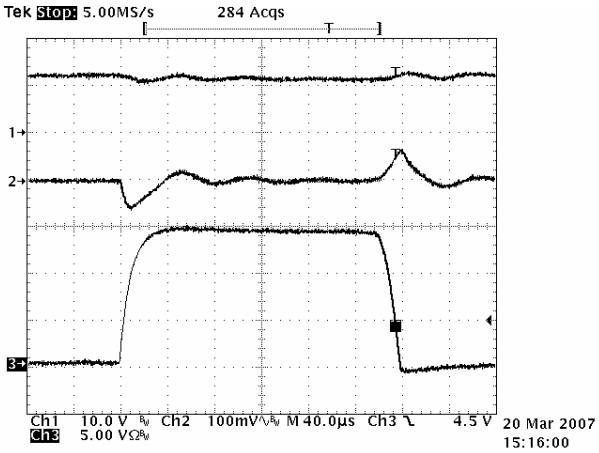


Figure 2. 60mV response to 0-15A Step
Ch1: Vin, ch2: Vout, ch3: Iout

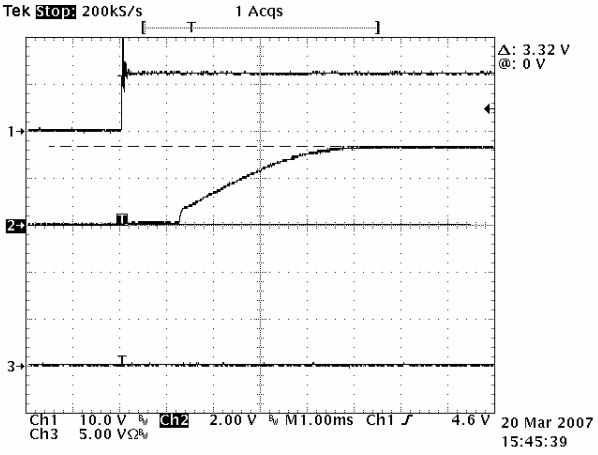


Figure 3. Startup at no Load
Ch1: Vin, ch2: Vout, ch3: Iout

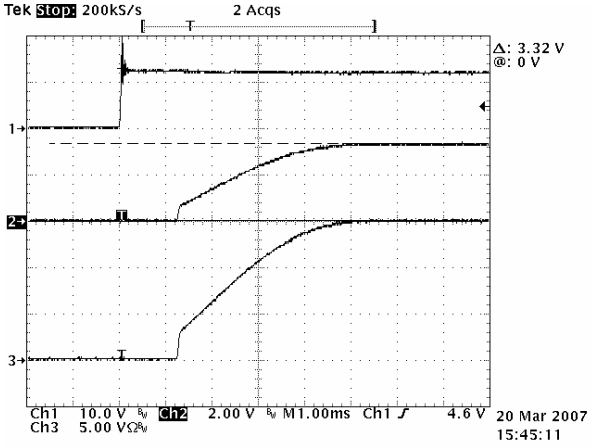
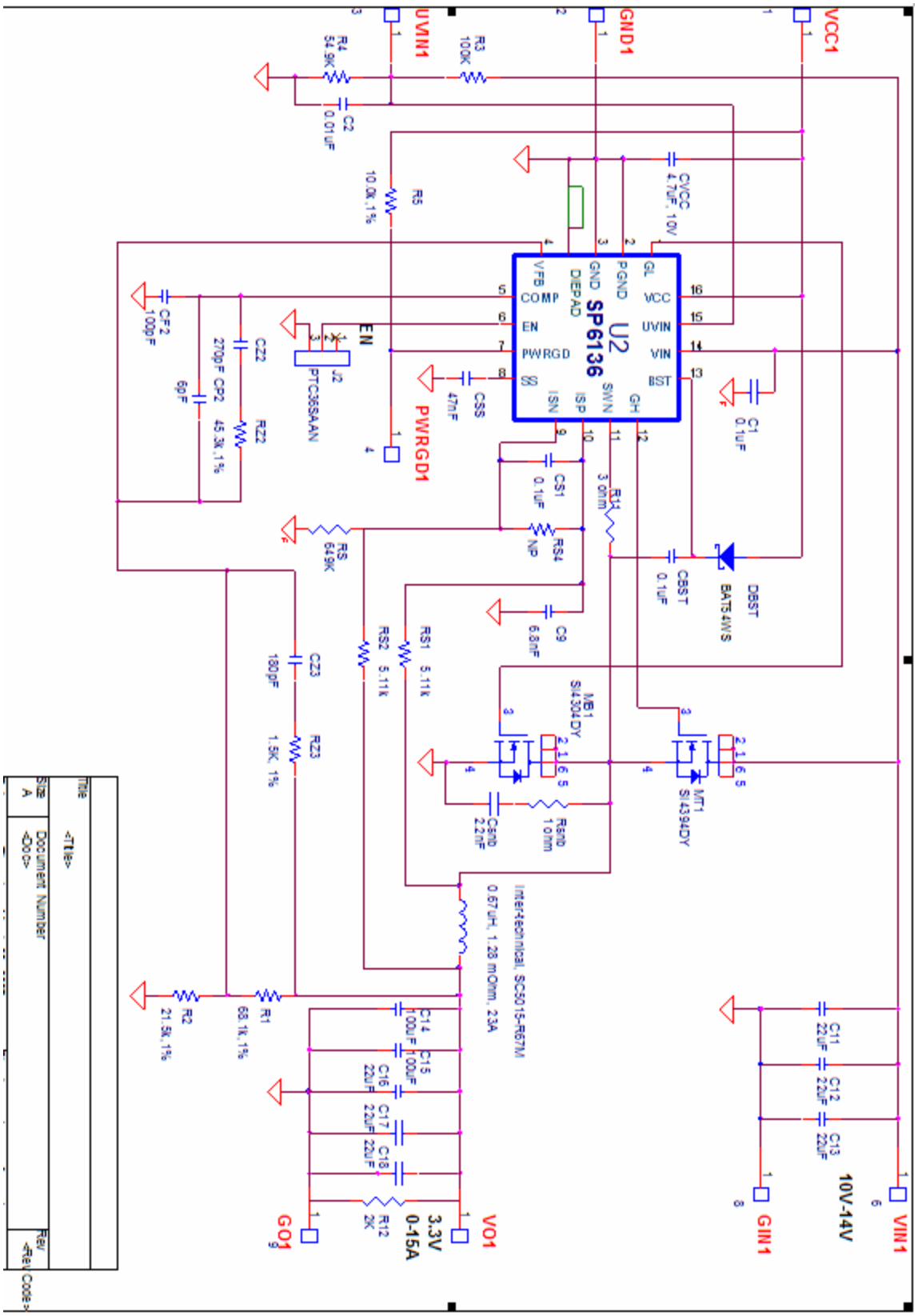


Figure 4. Startup at 15A
Ch1: Vin, ch2: Vout, ch3: Iout

Circuit Schematic



For further assistance:

Email: Sipexsupport@sipex.com
WWW Support page: http://www.sipex.com/content.aspx?p=support
Sipex Application Notes: http://www.sipex.com/applicationNotes.aspx

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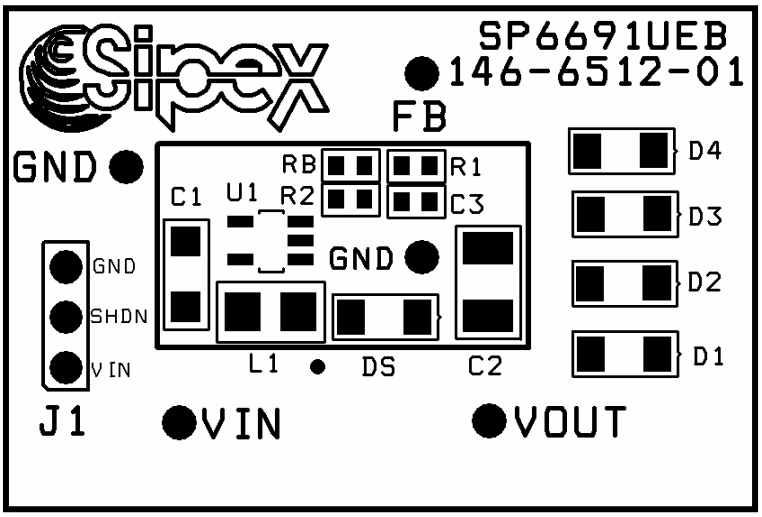
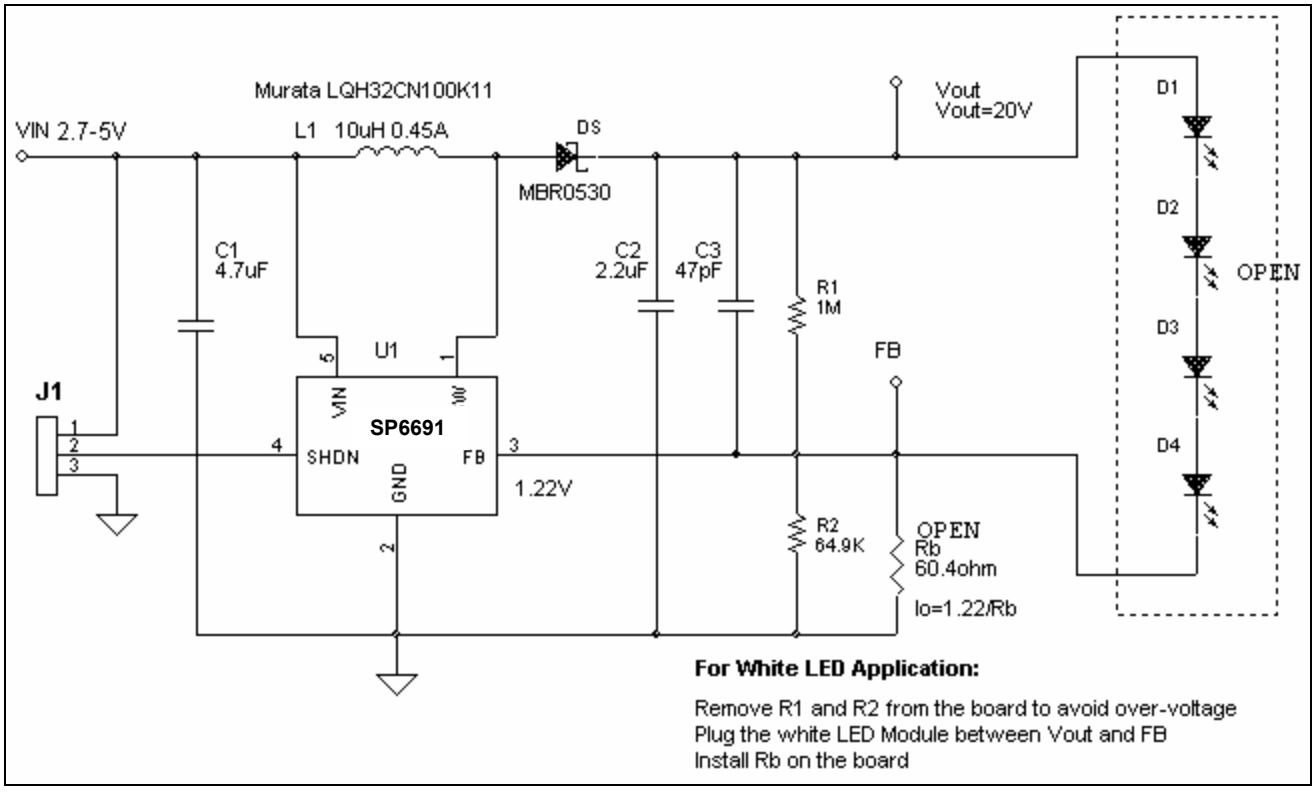
SP6691EB
Evaluation Board Manual

- Ideal for series white LED driver
- High output voltage, up to 30V
- Low quiescent current: 20uA
- Ultra low shutdown current: 10nA
- High Efficiency: up to 80%
- SOT23-5 Package & SMT components for small, low profile Power Supply



DESCRIPTION AND BOARD SCHEMATIC

The **SP6691EB Evaluation Board** is designed to help the user evaluate the performance of the SP6691EB as a series white LED driver. The evaluation board is a completely assembled and tested surface mount board which provides easy probe access points to all SP6691EB Inputs and Outputs so that the user can quickly connect and measure electrical characteristics and waveforms.



USING THE EVALUATION BOARD

1) Powering Up the SP6691EB Circuit

The SP6691EB Evaluation Board can be powered from inputs from a +1.2V to +5.0V. Connect with short leads directly to the "VIN" and "GND" posts. Monitor the Output Voltage and connect the Load between the "VOUT" post and the "GND" post.

2) Using the J1 Jumper: Enabling the SP6691EB Output and using the Shutdown Mode

The SP6691EB output will be enabled if the J1 Jumper is in the bottom or pin 1 to 2 position. If J1 is in the pin 2 to 3 or top position, the Shutdown pin is brought to GND, which puts the SP6691EB in the low quiescent Shutdown Mode.

3) Using the Posts

Since the part might get damaged when the output is open loop, two divider resistors (R_1=1M, R_2=64.9K) are used to provide the feedback loop and set the output voltage. For the white LEDs application, these two resistors (R_1, R_2) need to be removed from the evaluation board first to avoid over-voltage and then plug the white LED module between "VOUT" and "FB" posts. The bias resistor R_b should also be installed on the board.

4) Inductor Selection

For SP6691EB, the internal switch will be turned off only after the inductor current reaches the typical dc current limit (I_{LIM}=450mA). However, there is typically propagation delay of 200nS between the time when the current limit is reached and when the switch is actually turned off. During this 200nS delay, the peak inductor current will increase, exceeding the current limit by a small amount. The peak inductor current can be estimated by:

$$I_{pk} = I_{LIM} + \frac{V_{in(max)}}{L} \cdot 200nS$$

The larger the input voltage and the lower the inductor value, the greater the peak current.

In selecting an inductor, the saturation current specified for the inductor needs to be greater than the SP6691EB peak current to avoid saturating the inductor, which would result in a loss in efficiency and could damage the inductor.

Choosing an inductor with low DCR decreases power losses and increase efficiency.

Refer to Table 1 for some suggested low ESR inductors.

Table 1. Suggested Low ESR inductor

MANUFACTURE	PART NUMBER	DCR (Ω)	Current Rating (mA)
MURATA 770-436-1300	LQH32CN100K11 (10uH)	0.3	450
TDK 847-803-6100	NLC453232T-100K (22uH)	0.55	500

5) Diode Selection

A schottky diode with a low forward drop and fast switching speed is ideally used here to achieve high efficiency. In selecting a Schottky diode, the current rating of the schottky diode should be larger than the peak inductor current. Moreover, the reverse breakdown voltage of the schottky diode should be larger than the output voltage.

6) Capacitor Selection

Ceramic capacitors are recommended for their inherently low ESR, which will help produce low peak to peak output ripple, and reduce high frequency spikes.

For the typical application, 4.7uF input capacitor and 2.2uF output capacitor are sufficient. The input and output ripple could be further reduced by increasing the value of the input and output capacitors. Place all the capacitors as close to the SP6691EB as possible for layout. For use as a voltage source, to reduce the output ripple, a small feedforward (47pF) across the top feedback resistor can be used to provide sufficient overdrive for the error comparator, thus reducing the output ripple.

Refer to Table 2 for some suggested low ESR capacitors.

Table 2. Suggested Low ESR capacitor

MANUFACTURE	PART NUMBER	CAP /VOLTAGE	SIZE /TYPE
MURATA 770-436-1300	GRM32RR71E 225KC01B	2.2uF /25V	1210 /X5R
MURATA 770-436-1300	GRM31CR61A 475KA01B	4.7uF /10V	1206 /X5R
TDK 847-803-6100	C3225X7R1E 225M	2.2uF /25V	1210 /X7R
TDK 847-803-6100	C3216X5R1A 475K	4.7uF /10V	1206 /X5R

7) LED Current Program

In the white LEDs application, the SP6691EB is generally programmed as a current source. The bias resistor R_b is used to set the operating current of the white LED using the equation:

$$R_b = \frac{V_{FB}}{I_F}$$

where V_{FB} is the feedback pin voltage (1.22V), I_F is the operating current of the White LEDs. In order to achieve accurate LED current, 1% precision resistors are recommended. Table 3 below shows the R_b selection for different white LED currents. For example, to set the operating current to be 20mA, R_b is selected as 60.4 Ohm, as shown in the schematic.

Table 3. Bias Resistor Selection

I_F (mA)	R_b (Ω)
5	243
10	121
12	102
15	80.6
20	60.4

8) Vout Programming

The SP6691EB can be programmed as either a voltage source or a current source. To program the SP6691 as voltage source, the SP6691 requires 2 feedback resistors R_1 & R_2 to control the output voltage. The formula for the resistor selection are shown below.

$$R_1 = \left(\frac{V_{out}}{1.22} - 1\right) \bullet R_2$$

9) Open Circuit Protection

When any white LED inside the white LED module fails or the LED module is disconnected from the circuit, the output and the feedback control will be open, thus resulting in a high output voltage, which may cause the SW pin voltage to exceed it maximum rating. In this case, a zener diode can be used at the output to limit the voltage on the SW pin and protect the part. The zener voltage should be larger than the maximum forward voltage of the White LED module.

10) Brightness Control

Dimming control can be achieved by applying a PWM control signal to the EN/PWM pin. The brightness of the white LEDs is controlled by increasing and decreasing the duty cycle of The PWM signal. A 0% duty cycle corresponds to zero LED current and a 100% duty cycle corresponds to full load current. While the operating frequency range of the PWM control is from 60Hz to 700Hz, the recommended maximum brightness frequency range of the PWM signal is from 60Hz to 200Hz. A repetition rate of at least 60Hz is required to prevent flicker. The magnitude of the PWM signal should be higher than the minimum SHDN voltage high.

11) Layout Consideration

Both the input capacitor and the output capacitor should be placed as close as possible to the IC. This can reduce the copper trace resistance which directly affects the input and output ripples. The feedback resistor network should be kept close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the feedback resistor network should connect directly to the GND pin or to an analog ground plane that is tied directly to the GND pin. The inductor and the schottky diode should be placed as close as possible to the switch pin to minimize the noise coupling to the other circuits, especially the feedback network.

POWER SUPPLY DATA

For the standard evaluation board (4x20mA series white LEDs application), in which the output voltage is around 15V and output current is 20mA, the power supply data is provided in Fig 1. to Fig. 4. The white LEDs used here were from LUMEX (Part Number: SML-LX2832UWC-TR).

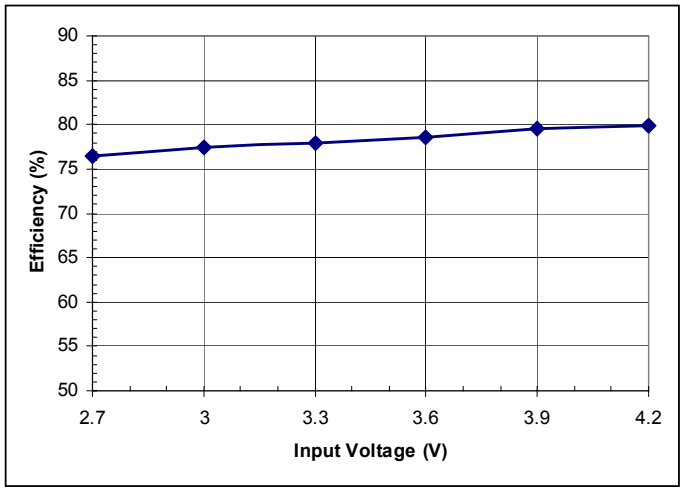


Fig. 1 Efficiency vs Input Voltage

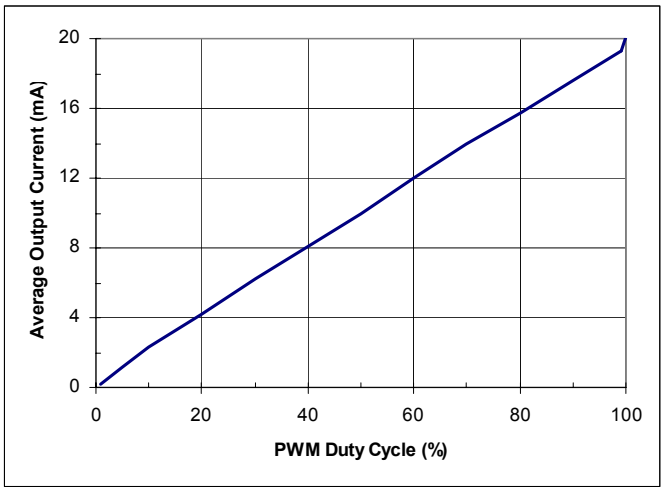


Fig. 2 Average Io vs SHDN duty cycle

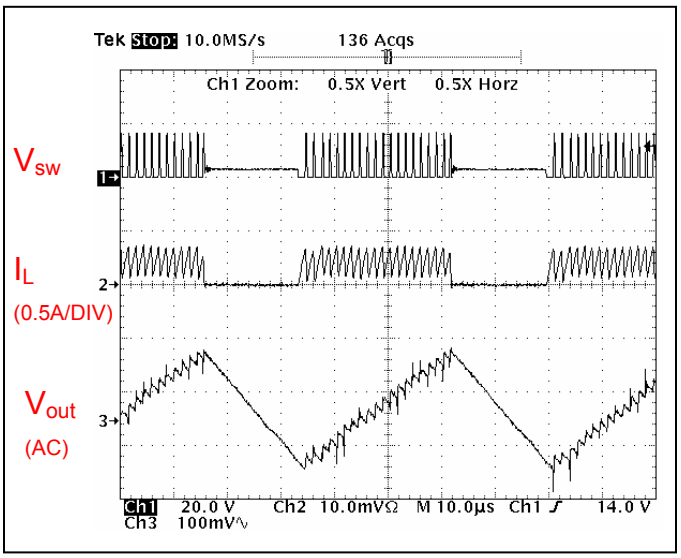


Fig. 3 Typical Switching Waveform (V_{in}=3.3V)

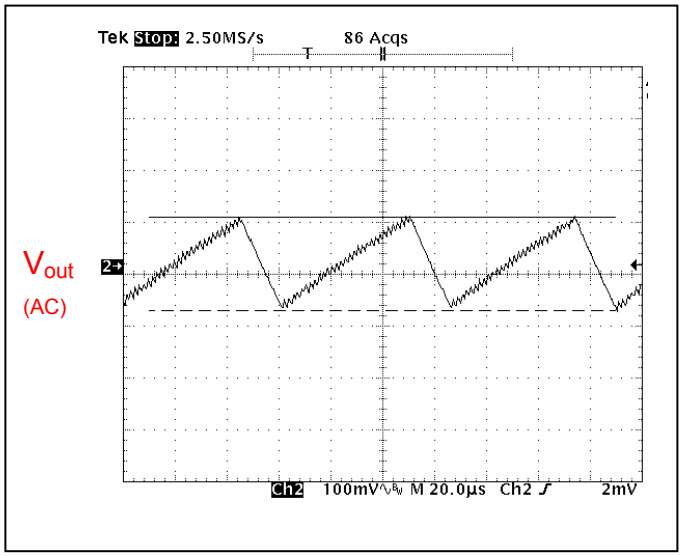


Fig. 4 Output Ripple (V_{in}=2.7V)

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EVALUATION BOARD LAYOUT

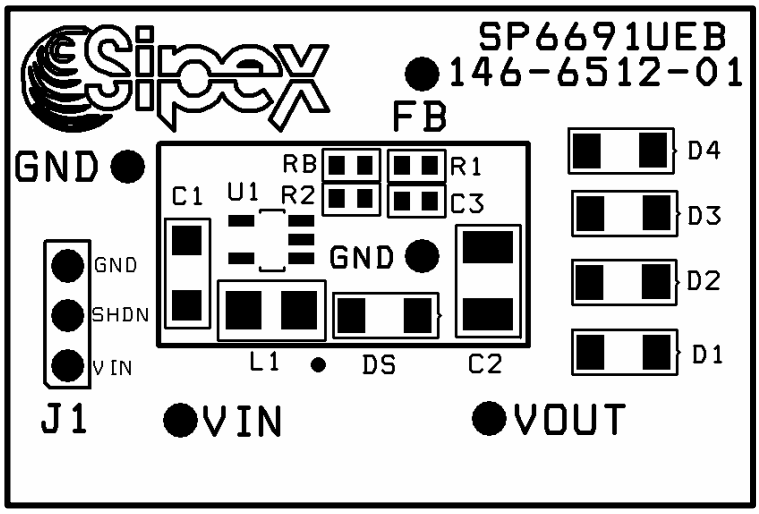

FIGURE 1: SP6691EB COMPONENT PLACEMENT

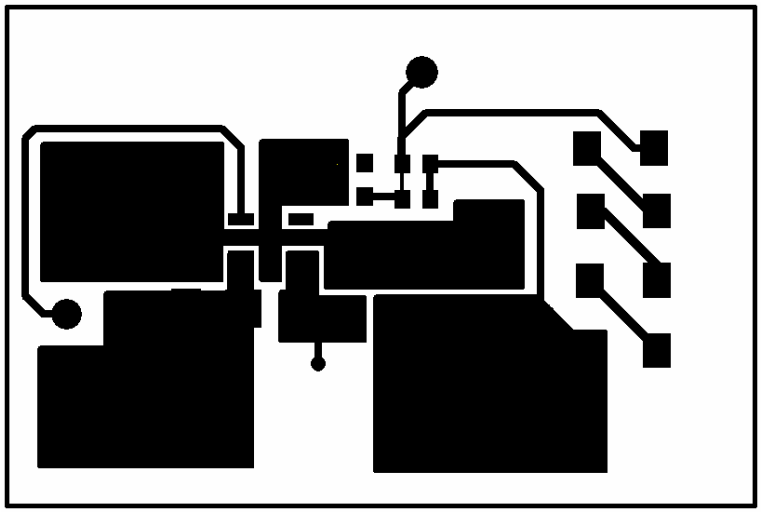

FIGURE 2: SP6691EB PC LAYOUT TOP SIDE

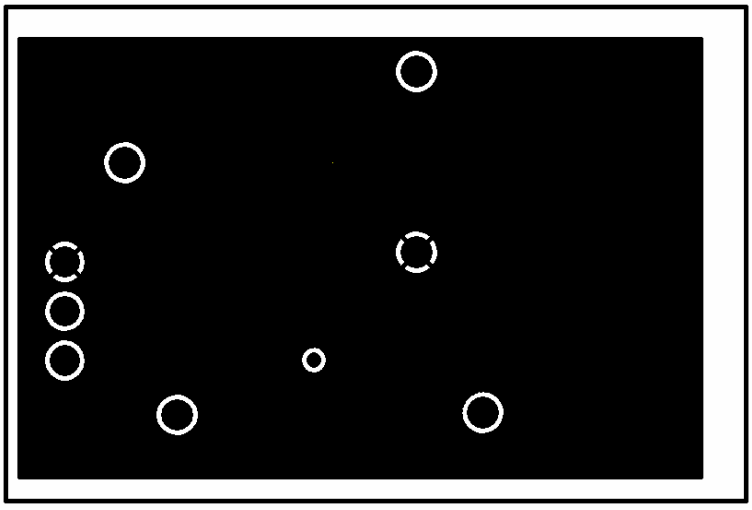

FIGURE 3: SP6691EB PC LAYOUT BOTTOM SIDE

TABLE1: SP6691EB LIST OF MATERIALS

SP6691 Evaluation Board List of Materials						
Ref. Des.	Qty.	Manufacturer	Part Number	Layout Size LxWxH	Component	Vendor
	1	Sipex Corp.	146-6512-00	1"x1.5"	SP6690 Eval PC Board	Sipex 978-667-8700
U1	1	Sipex Corp.	SP6691EK	SOT23-5	5-pin SOT23 Step-Up DC/DC Conv	Sipex 978-667-8700
C1	1	Murata	GRM31CR61A475KA01B	1206	Ceramic 10V 4.7uF SM	Murata 770-436-1300
C2	1	Murata	GRM32RR71E225KC01B	1210	Ceramic 25V 2.2uF SM	Murata 770-436-1300
C3	1	Murata	GRM1885C1H470JA01B	603	Ceramic 47pF SM	Murata 770-436-1300
L1	1	Murata	LQH32CN100K11	3.2X2.5X2mm	10uH, 0.45A, 0.3 Ohm, SM Inductor	Murata 770-436-1300
R1	1	Panasonic	ERJ-3EKF1004	603	1M Ohm 1/16W 1% 0603 SM	800-Digi-Key
R2	1	Panasonic	ERJ-3EKF6492	603	64.9K Ohm 1/16W 1% 0603 SM	800-Digi-Key
Rb	1	Panasonic	ERJ-3EKF60R4V	603	Open	800-Digi-Key
DS	1	On-Semi	MBR-0530	SOD-123	Schottky Diode 30V, 0.5A	Onsemi
D1-D4	1			SOD-123	Open	
TP	5	Mill-Max	0300-115-01-4727100	.042 Dia	Test Point Female Pin	800-Digi-Key
J1	1	Sullins	PTC36SAAN	.23x.12	2-Pin Header	800-Digi-Key

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6691EB	-40°C to +85°C	SP6691 Evaluation Board
SP6691EU	-40°C to +85°C	5-pin SOT-23