



Integrated Device Technology, Inc.

3.3V CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT3373/A
IDT54/74FCT3533/A
IDT54/74FCT3573/A
PRODUCT PREVIEW

FEATURES:

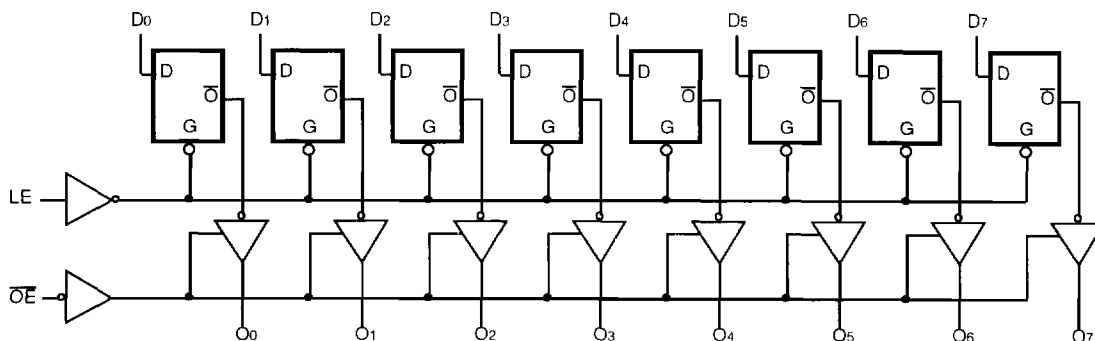
- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or
Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (10µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

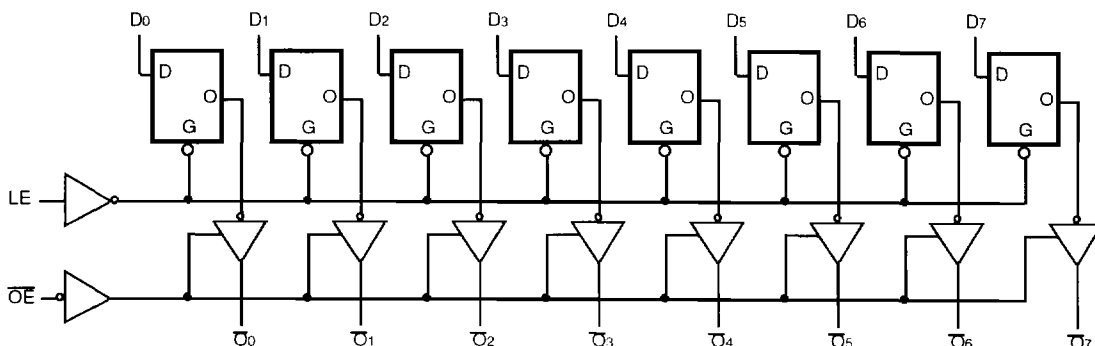
The IDT54/74FCT3373/A, IDT54/74FCT3533/A and IDT54/74FCT3573/A are octal transparent latches built using an advanced dual metal CMOS technology.

These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAM FCT3373 AND FCT3573



FUNCTIONAL BLOCK DIAGRAM FCT3533

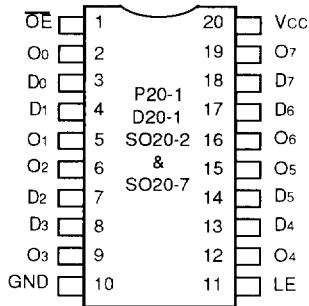


3093 drw 01

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PIN CONFIGURATIONS

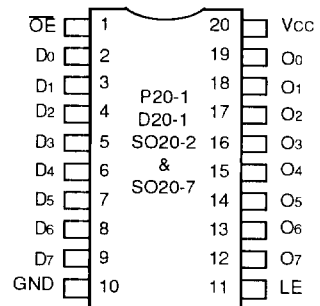
FCT3373



DIP/SOIC/SSOP
TOP VIEW

3093 drw 02

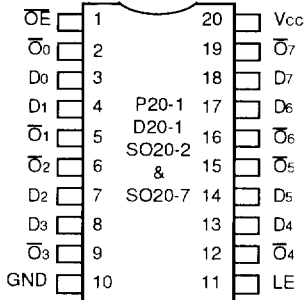
FCT3573



DIP/SOIC/SSOP
TOP VIEW

3093 drw 03

FCT3533



DIP/SOIC/SSOP
TOP VIEW

3093 drw 04

FUNCTION TABLE (3533)⁽¹⁾

Inputs			Outputs
DN	LE	OE	ON
H	H	L	L
L	H	L	H
X	X	H	Z

3093 tbl 01

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
DN	Data Inputs
LE	Latch Enable Input (Active HIGH)
OE	Output Enable Input (Active LOW)
ON	3-State Outputs
ON	Complementary 3-State Outputs

3093 tbl 02

FUNCTION TABLE (3373 and 3573)⁽¹⁾

Inputs			Outputs
DN	LE	OE	ON
H	H	L	H
L	H	L	L
X	X	H	Z

3093 tbl 03

NOTE:

- H = HIGH Voltage Level
- X = Don't Care
- L = LOW Voltage Level
- Z = High Impedance

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	-0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V _{TERM} ⁽⁴⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} + 0.5	-0.5 to V _{CC} + 0.5	V
T _A	Operating Temperature	-40 to +85	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	-60 to +60	-60 to +60	mA

NOTES:

3093 Ink 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	4.0	8.0	pF

NOTE:

3093 Ink 05

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V ; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit				
V _{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2.0	—	5.5	V				
	Input HIGH Level (I/O pins)		2.0	—	V _{CC} +0.5					
V _{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V				
I _{IH}	Input HIGH Current (Input pins) ⁽⁶⁾	V _{CC} = Max. V _I = 5 V	—	—	±1	μA				
	Input HIGH Current (I/O pins) ⁽⁶⁾		—	—	±1					
I _{IL}	Input LOW Current (Input pins) ⁽⁶⁾		V _I = GND	—	—		±1			
	Input LOW Current (I/O pins) ⁽⁶⁾			—	—		±1			
I _{ozH}	High Impedance Output Current (3-State Output pins) ⁽⁶⁾	V _{CC} = Max. V _O = V _{CC}	—	—	±1	μA				
I _{ozL}			V _O = GND	—	—		±1			
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V				
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	-36	-60	-110	mA				
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	50	90	200	mA				
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -0.1mA	V _{CC} -0.2	—	V				
		V _{CC} = 3.0V V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3mA	2.4	3.0					
			I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.	2.4 ⁽⁵⁾	3.0		—			
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1mA	—	0.2	V				
			I _{OL} = 16mA	—	0.2		0.4			
			I _{OL} = 24mA	—	0.3		0.5			
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max., V _O = GND ⁽³⁾	-60	-135	-240	mA				
V _H	Input Hysteresis	—	—	150	—	mV				
I _{CC1}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}	COM'L.	—	0.1	10				
I _{CC2}							MIL.	—	0.1	100
I _{CC3}										

NOTES:

3093 Ink 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V_{OH} = V_{CC} - 0.6V at rated current.
- The test limits for this parameter is ± 5μA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit	
ΔI_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$				μA	
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$				$\mu A / \text{MHz}$	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $LE = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$				mA	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$					
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $LE = V_{CC}$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$					
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$					

NOTES:

3093 tbl 07

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current } (I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽³⁾

Symbol	Parameter	Conditions ⁽¹⁾	FCT3373/3573				FCT3373A/3573A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
tPLH	Propagation Delay LE to ON		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	ns
tPZH	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	ns
tPZL	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	ns

3093 tbl 08

Symbol	Parameter	Conditions ⁽¹⁾	FCT3533				FCT3533A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	ns
tPLH	Propagation Delay LE to ON		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	ns
tPZH	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	ns
tPZL	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width HIGH ⁽³⁾		6.0	—	6.0	—	5.0	—	6.0	—	ns

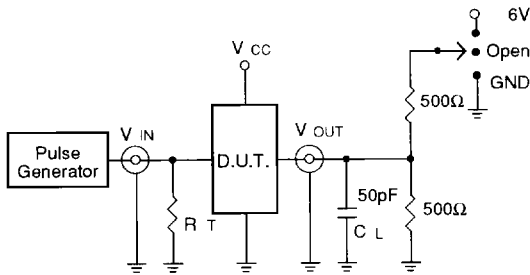
3093 tbl 09

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ± 0.3V, Normal Range. For Vcc = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3093 drw 05

SWITCH POSITION

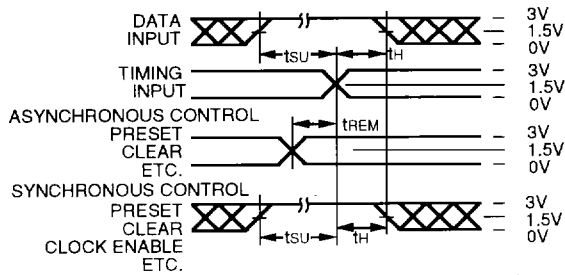
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

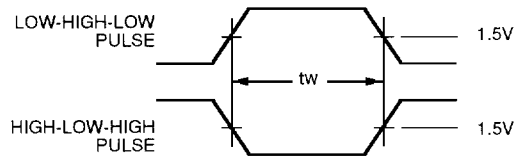
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SET-UP, HOLD AND RELEASE TIMES



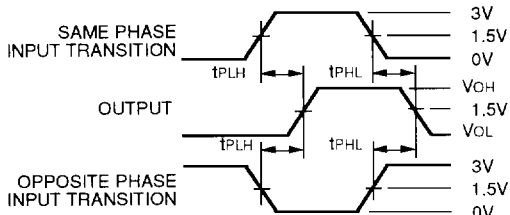
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PULSE WIDTH



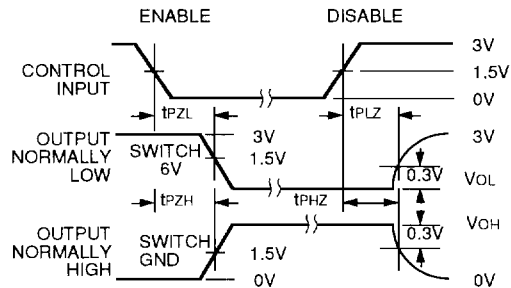
3093 drw 06

PROPAGATION DELAY



3093 drw 07

ENABLE AND DISABLE TIMES



3093 drw 08

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.
- If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

ORDERING INFORMATION

IDT	XX	FCT	X	XX	X	X	
Temp. Range		Family	Device Type	Package	Process		
						Blank	Commercial
						B	MIL-STD-883, Class B
						P	Plastic DIP (P20-1)
						D	CERDIP (D20-1)
						SO	Small Outline IC (SO20-2)
						PY	Shrink Small Outline Package (SO20-7)
						373	Non-Inverting Octal Transparent Latch
						573	Non-Inverting Octal Transparent Latch
						533	Inverting Octal Transparent Latch
						373A	
						573A	
						533A	
						3	3.3 Volt
						54	-55°C to +125°C
						74	-40°C to +85°C

3093 drw 09