



MM54HC259/MM74HC259 8-Bit Addressable Latch/3-to-8 Line Decoder

General Description

This device utilizes advanced silicon-gate CMOS technology to implement an 8-bit addressable latch, designed for general purpose storage applications in digital systems.

The MM54HC259/MM74HC259 has a single data input (D), 8 latch outputs (Q₀–Q₇), 3 address inputs (A, B, and C), a common enable input (\bar{G}), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addressed output. The data is stored when ENABLE transitions from low to high. All unaddressed latches will remain unaffected. With enable in the high state the device is deselected, and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

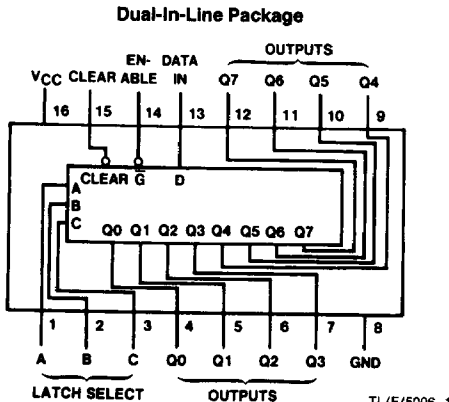
If enable is held high and CLEAR is taken low all eight latches are cleared to a low state. If enable is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide supply range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum (74HC Series)

Connection Diagram



Top View

Order Number MM54HC259* or MM74HC259*

*Please look into Section 8, Appendix D for availability of various package types.

Latch Selection Table

| Select Inputs | | | Latch Addressed |
|---------------|---|---|-----------------|
| C | B | A | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

H = high level, L = low level

D = the level at the data input

Q_{i0} the level of Q_i (i = 0, 1, ..., 7, as appropriate) before the indicated steady-state input conditions were established.

Truth Table

| Inputs | | Outputs of Addressed Latch | Each Other Output | Function |
|--------|-----------|----------------------------|-------------------|--------------------------|
| Clear | \bar{G} | | | |
| H | L | D | Q _{i0} | Addressable Latch Memory |
| H | H | Q _{i0} | Q _{i0} | |
| L | L | D | L | 8-Line Decoder Clear |
| L | H | L | L | |

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------------|
| Supply Voltage (V_{CC}) | -0.5 to +7.0V |
| DC Input Voltage (V_{IN}) | -1.5 to $V_{CC} + 1.5V$ |
| DC Output Voltage (V_{OUT}) | -0.5 to $V_{CC} + 0.5V$ |
| Clamp Diode Current (I_{IK}, I_{OK}) | ± 20 mA |
| DC Output Current, per pin (I_{OUT}) | ± 25 mA |
| DC V_{CC} or GND Current, per pin (I_{CC}) | ± 50 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering 10 seconds) | 260°C |

Operating Conditions

| | Min | Max | Units |
|--|-----|----------|-------|
| Supply Voltage (V_{CC}) | 2 | 6 | V |
| DC Input or Output Voltage (V_{IN}, V_{OUT}) | 0 | V_{CC} | V |
| Operating Temp. Range (T_A) | | | |
| MM74HC | -40 | +85 | °C |
| MM54HC | -55 | +125 | °C |
| Input Rise or Fall Times (t_r, t_f) | | | |
| $V_{CC} = 2.0V$ | | 1000 | ns |
| $V_{CC} = 4.5V$ | | 500 | ns |
| $V_{CC} = 6.0V$ | | 400 | ns |

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | 74HC $T_A = -40$ to $85^\circ C$ | | 54HC $T_A = -55$ to $125^\circ C$ | | Units | | |
|----------|-----------------------------------|---|----------|--------------------|-----------|-------------------------------------|-----------|--------------------------------------|--|-------|--|--|
| | | | | Typ | | Guaranteed Limits | | | | | | |
| | | | | | | | | | | | | |
| V_{IH} | Minimum High Level Input Voltage | | 2.0V | | 1.5 | 1.5 | 1.5 | V | | | | |
| | | | 4.5V | | 3.15 | 3.15 | 3.15 | V | | | | |
| | | | 6.0V | | 4.2 | 4.2 | 4.2 | V | | | | |
| V_{IL} | Maximum Low Level Input Voltage** | | 2.0V | | 0.5 | 0.5 | 0.5 | V | | | | |
| | | | 4.5V | | 1.35 | 1.35 | 1.35 | V | | | | |
| | | | 6.0V | | 1.8 | 1.8 | 1.8 | V | | | | |
| V_{OH} | Minimum High Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$ | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | V | | | | |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | V | | | | |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | V | | | | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V | | | | |
| | | | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V | | | | |
| | | | | | | | | | | | | |
| V_{OL} | Maximum Low Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$ | 2.0V | 0 | 0.1 | 0.1 | 0.1 | V | | | | |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | V | | | | |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V | | | | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V | | | | |
| | | | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V | | | | |
| | | | | | | | | | | | | |
| I_{IN} | Maximum Input Current | $V_{IN} = V_{CC}$ or GND | 6.0V | | ± 0.1 | ± 1.0 | ± 1.0 | μA | | | | |
| I_{CC} | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$ | 6.0V | | 8.0 | 80 | 160 | μA | | | | |

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics ($V_{CC}=5.0V$, $T_A=25^\circ C$, $t_r=t_f=6$ ns, $C_L=15$ pF unless otherwise specified.)

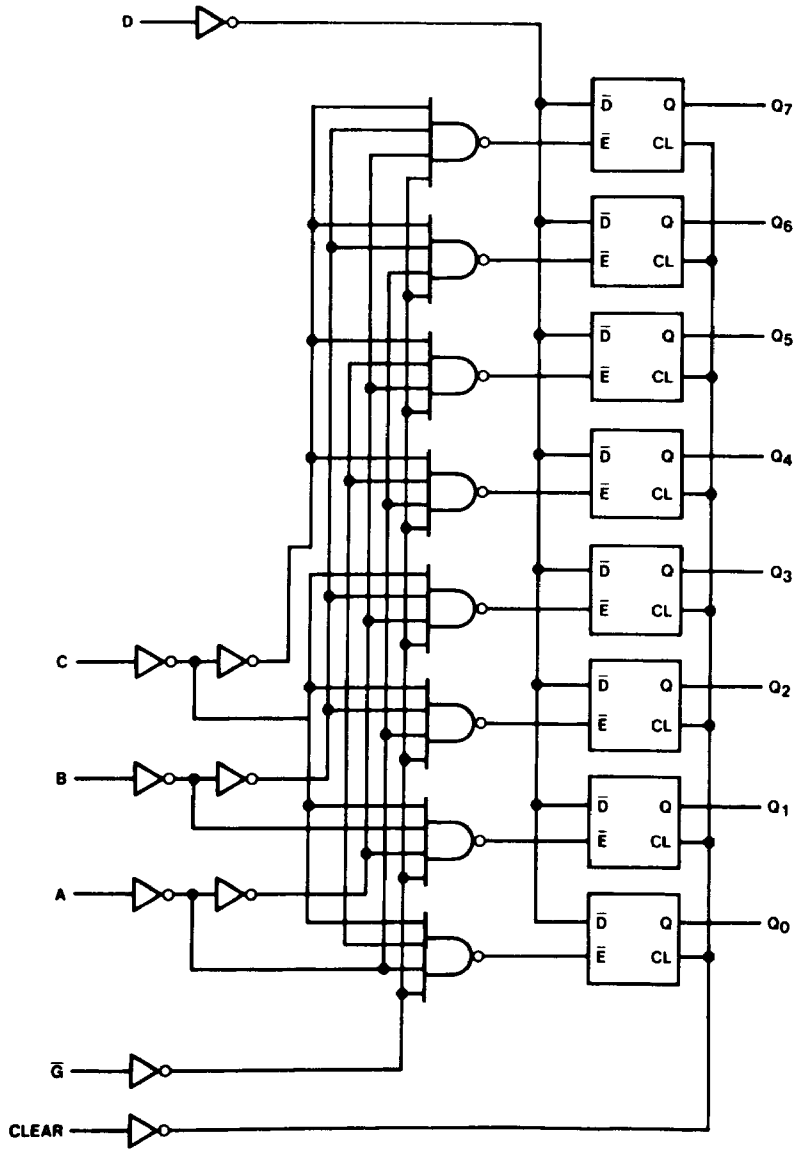
| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|-----------------------|---|------------|-----|------------------|-------|
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Data to Output | | 18 | 32 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Select to Output | | 20 | 38 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Enable to Output | | 20 | 35 | ns |
| t_{PHL} | Maximum Propagation Delay Clear to Output | | 17 | 27 | ns |
| t_W | Minimum Enable Pulse Width | | 10 | 16 | ns |
| t_W | Minimum Clear Pulse Width | | 10 | 16 | ns |
| t_r , t_f | Maximum Input Rise and Fall Time | | | 500 | ns |
| t_s | Minimum Setup Time Select or Data to Enable | | 15 | 20 | ns |
| t_H | Minimum Hold Time Data or Address to Enable | | -2 | 0 | ns |

AC Electrical Characteristics ($t_r=t_f=6$ ns, $C_L=50$ pF, $V_{CC}=2.0V-6.0V$)

| Symbol | Parameter | Conditions | V_{CC} | $T_A=25^\circ C$ | | $T_A=-40$ to $85^\circ C$ | | $T_A=-55$ to $125^\circ C$ | | Units |
|-----------------------|--|---------------|----------|------------------|-------------------|---------------------------|-----|----------------------------|--|-------|
| | | | | Typ | Guaranteed Limits | | | | | |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Data to Output | | 2.0V | 60 | 180 | 225 | 250 | ns | | |
| | | | 4.5V | 19 | 37 | 46 | 52 | ns | | |
| | | | 6.0V | 17 | 32 | 40 | 45 | ns | | |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Select to Output | | 2.0V | 72 | 220 | 275 | 310 | ns | | |
| | | | 4.5V | 21 | 43 | 54 | 60 | ns | | |
| | | | 6.0V | 18 | 37 | 46 | 52 | ns | | |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Enable to Output | | 2.0V | 65 | 200 | 250 | 280 | ns | | |
| | | | 4.5V | 27 | 40 | 50 | 58 | ns | | |
| | | | 6.0V | 23 | 35 | 44 | 50 | ns | | |
| t_{PHL} | Maximum Propagation Delay Clear to Output | | 2.0V | 50 | 150 | 190 | 210 | ns | | |
| | | | 4.5V | 18 | 31 | 39 | 44 | ns | | |
| | | | 6.0V | 16 | 26 | 32 | 37 | ns | | |
| t_W | Minimum Pulse Width Clear or Enable | | 2.0V | | 80 | 100 | 120 | ns | | |
| | | | 4.5V | | 16 | 20 | 24 | ns | | |
| | | | 6.0V | | 14 | 18 | 20 | ns | | |
| t_s | Minimum Setup Time Address or Data to Enable | | 2.0V | | 100 | 125 | 150 | ns | | |
| | | | 4.5V | | 20 | 25 | 28 | ns | | |
| | | | 6.0V | | 15 | 19 | 25 | ns | | |
| t_H | Minimum Hold Time Address or Data to Enable | | 2.0V | -10 | 0 | 0 | 0 | ns | | |
| | | | 4.5V | -2 | 0 | 0 | 0 | ns | | |
| | | | 6.0V | -2 | 0 | 0 | 0 | ns | | |
| t_{TLH} , t_{THL} | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | ns | | |
| | | | 4.5V | 8 | 15 | 19 | 22 | ns | | |
| | | | 6.0V | 7 | 13 | 16 | 19 | ns | | |
| C_{IN} | Input Capacitance | | | 5 | 10 | 10 | 10 | pF | | |
| C_{PD} | Power Dissipation Capacitance (Note 5) | (per package) | | 80 | | | | pF | | |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} s f + I_{CC}$.

Logic Diagram



TL/F/5006-2