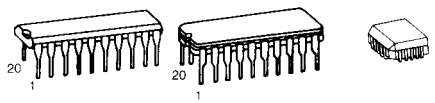
HS-C²MOS™ INTEGRATED CIRCUITS

M54HC373/563/533/573
M74HC373/563/533/573

PRELIMINARY DATA

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
HC373 NON INVERTING
HC533 INVERTING
HC563 INVERTING
HC573 NON INVERTING



B1 Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

ORDERING NUMBERS: M54HCXXX F1
M74HCXXX B1
M74HCXXX F1
M74HCXXX C1

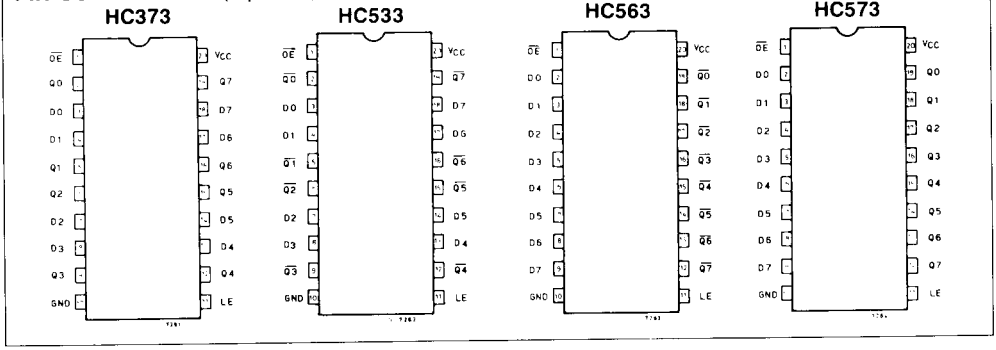
DESCRIPTION

The M54/74HC373, M54/74HC533, M54/74HC563 and M54/74HC573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.
These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). While the LE input is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data.
While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The application designer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighboring input/output pin layout. The HC373 and the HC573, the HC533 and the HC563 have the same function and the same characteristics respectively, but have different pin layouts. The three-state output configuration and the wide choice of outline make bus-organized systems simple.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

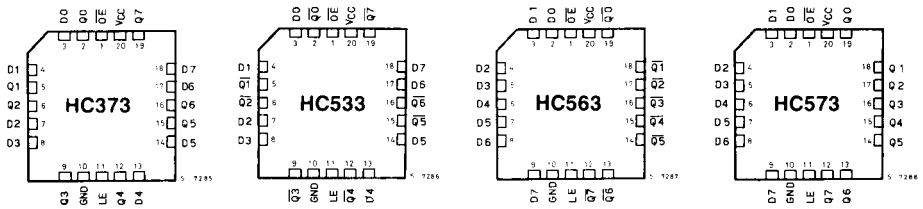
FEATURES

- High Speed
  t_{PD} = 15 ns (Typ) at V_{CC} = 5V
- Low Power Dissipation
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability
  15 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 6 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible with 74LS373/533/563/573

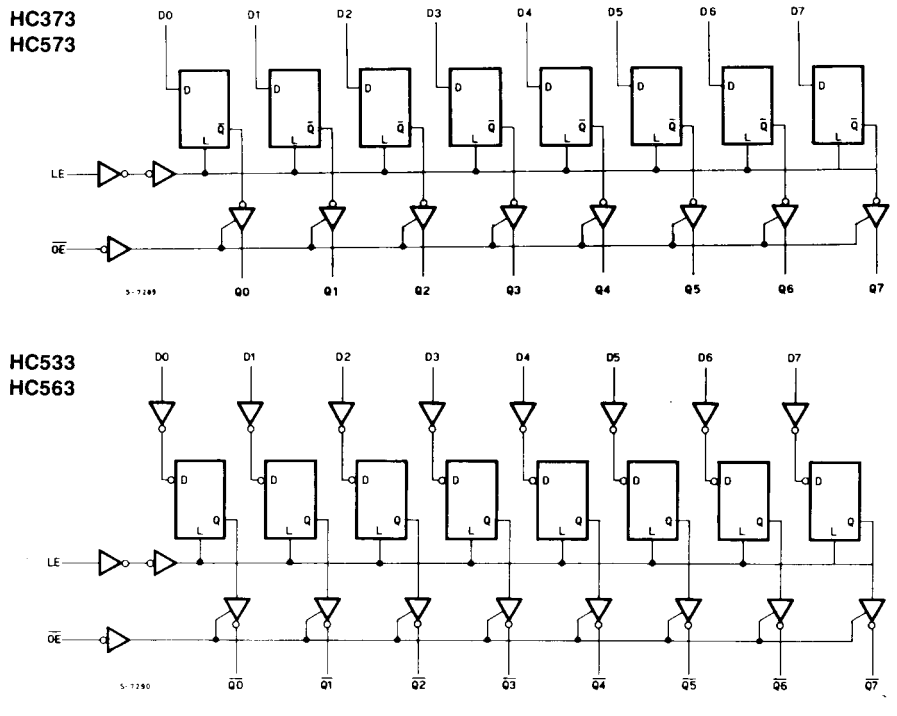
PIN CONNECTIONS (top view)



CHIP CARRIER



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HC373) (HC573)	$\overline{Q}$ (HC533) (HC563)
H	X	X	Z	Z
L	L	X	No change*	No change*
L	H	L	L	H
L	H	H	H	L

X: Don't Care Z: High impedance

*: Q/$\overline{Q}$ outputs are latched at the time when the LE input is taken low logic level.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
Tstg	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{OZ}	3-State Output Off-State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND		—	—	±0.5	—	±5		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND I_O = 0		—	—	4	—	40		80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	CL (pF)	54HC and 74HC			Unit
			MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time	50		7	11	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LE-Q, $\overline{Q}$)	50		20	32	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D-Q, $\overline{Q}$)	50		17	27	ns
$t_{W(H)}$	Minimum Pulse Width (LE)	50		8	15	ns
t_s	Minimum Set-up Time	50		2	15	ns
t_h	Minimum Hold Time	50		—	10	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	50		17	27	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	5		16	26	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	24	60	—	75			ns
		4.5		—	8	12	—	15			
		6.0		—	6	10	—	13			
t_{PLH} t_{PHL}	Propagation Delay Time (LE - Q, $\overline{Q}$)	2.0		—	82	175	—	210			ns
		4.5		—	22	35	—	42			
		6.0		—	19	30	—	36			
t_{PLH} t_{PHL}	Progation Delay Time ($\overline{D}$-Q, $\overline{Q}$)	2.0		—	66	145	—	175			ns
		4.5		—	18	29	—	35			
		6.0		—	16	25	—	30			
$t_{W(H)}$	Minimum Pulse Width (LE)	2.0		—	30	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time	2.0		—	10	75	—	90			ns
		4.5		—	2	15	—	18			
		6.0		—	2	13	—	16			
t_h	Minimum Hold Time	2.0		—	—	50	—	60			ns
		4.5		—	—	10	—	12			
		6.0		—	—	9	—	11			
t_{PZL} t_{PZH}	Output Enable Time	2.0	$R_L = 1k\Omega$	—	62	145	—	175			ns
		4.5		—	18	29	—	35			
		6.0		—	16	25	—	30			
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	$R_L = 1k\Omega$	—	45	175	—	210			ns
		4.5		—	22	35	—	42			
		6.0		—	20	30	—	36			
C_{IN}	Input Capacitance			—	5	10	—	10			pF
C_{OUT}	Output Capacitance			—	10	—	—	—			
C_{PD} (*)	Power Dissipation Capacitance			—	41	—	—	—			

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Latch)