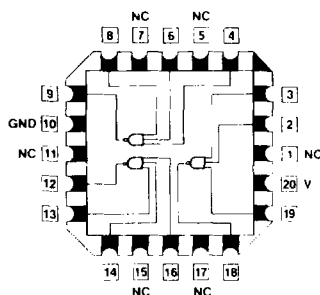
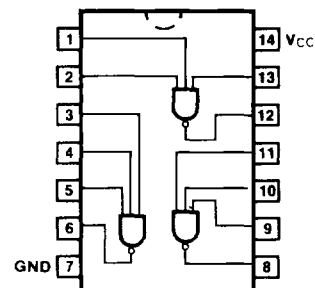


54F/74F10

Triple 3-Input NAND Gate

Connection Diagrams

Pin Assignment
for LCC and PCCPin Assignment
for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max		$V_{IN} = \text{Gnd}$	$V_{CC} = \text{Max}$
I_{CCH}	Power Supply Current		1.4	2.1	mA		
I_{CCL}			5.1	7.7		$V_{IN} = \text{Open}$	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	3-1
		1.5	3.2	4.3	1.5	6.5	1.5	5.3		3-3