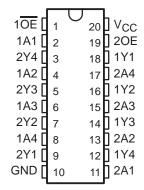
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

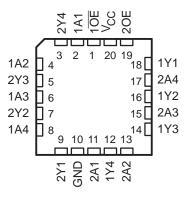
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'F240 and 'F244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{OE} (active-low output-enable) inputs, and complementary OE and \overline{OE} inputs.

The SN54F241 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74F241 is characterized for operation from 0°C to 70°C.

SN54F241 . . . J PACKAGE SN74F241 . . . DW OR N PACKAGE (TOP VIEW)



SN54F241 . . . FK PACKAGE (TOP VIEW)

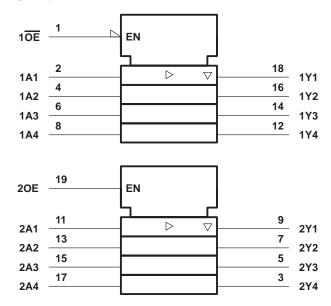


FUNCTION TABLES

INP	JTS	ОИТРИТ
10E	1A	1Y
Н	Χ	Z
L	Н	н
L	L	L

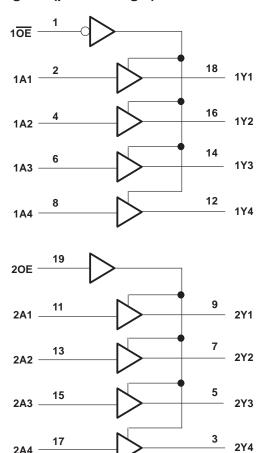
INP	JTS	OUTPUT
20E	2A	2Y
Н	Н	Н
Н	L	L
L	X	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	0.5 V to 5.5 V
Voltage range applied to any output in the high state	0.5 V to V _{CC}
Current into any output in the low state: SN54F241	96 mA
SN74F241	128 mA
Operating free-air temperature range: SN54F241	–55°C to 125°C
SN74F241	0°C to 70°C
Storage temperature range	–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.



recommended operating conditions

		S	N54F24	1	S	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
ΙΙΚ	Input clamp current			-18			-18	mA
IOH	High-level output current			- 12			- 15	mA
loL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEG	TEST CONDITIONS			1	S				
PARAMETER	TEST CONDITIONS			TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	V _{CC} = 4.5 V,	I _I = –18 mA			-1.2			-1.2	V	
		$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3			
V	V _{CC} = 4.5 V	$I_{OH} = -12 \text{ mA}$	2	3.2					V	
VOH		$I_{OH} = -15 \text{ mA}$				2	3.1		V	
	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -3 \text{ mA}$				2.7			7	
V	V45V	I _{OL} = 48 mA		0.38	0.55				V	
V _{OL}	V _{CC} = 4.5 V	$I_{OL} = 64 \text{ mA}$					0.42	0.55	V	
lozh	V _{CC} = 5.5 V,	V _O = 2.7 V			50			50	μΑ	
lozL	V _{CC} = 5.5 V,	V _O = 0.5 V			-50			-50	μA mA	
lį	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1		
lн	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ	
OE or OE	V 55V	V. 05.V			– 1			– 1	mA	
I _{IL} Any A	$V_{CC} = 5.5 \text{ V},$	V _I = 0.5 V		- 1.6		_		- 1.6	mA	
los [‡]	V _{CC} = 5.5 V,	V _O = 0	-100		-225	-100		-225	mA	
		Outputs high		40	60		40	60		
Icc	V _{CC} = 5.5 V	Outputs low		60	90		60	90	mA	
		Outputs disabled		60	90		60	90		

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN54F241, SN74F241 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SDFS090 - MARCH 1987 - REVISED OCTOBER 1993

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25^{\circ}\text{C}$			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX [†]				UNIT
			′F241			SN54	F241	SN74F241		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH	Any A	Υ	1.7	3.6	5.2	1.2	6.5	1.7	6.2	ns
t _{PHL}	Ally A		1.7	3.6	5.2	1.2	7	1.7	6.5	
^t PZH	OE or OE	Y	1.2	3.9	5.7	1.2	7	1.2	6.7	20
t _{PZL}	OE OF OE		1.2	5	7	1.2	8.5	1.2	8	ns
t _{PHZ}	OE or OE	Y	1.2	4.1	6	1.2	7	1.2	7	ns
^t PLZ	OL 01 OL	OE OF OE Y		4.1	6	1.2	7.5	1.2	7	115

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuits and waveforms are shown in Section 1.



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PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY/PKG

APPLICATION NOTES | RELATED DOCUMENTS

PRODUCT SUPPORT: TRAINING

SN74F241, Octal Buffers/Drivers With 3-State Outputs

DEVICE STATUS: ACTIVE

PARAMETER NAME	SN54F241	SN74F241		
Voltage Nodes (V)	5	5		
Vcc range (V)	4.5 to 5.5	4.5 to 5.5		
Input Level	TTL	TTL		
Output Level	TTL	TTL		
Output Drive (mA)		-15/64		
tpd max (ns)		6.5		
Static Current		75		

FEATURES ▲Back to Top

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

DESCRIPTION Back to Top

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the ´F240 and ´F244, these devices provide the choice of selected combinations of inverting and non inverting outputs, symmetrical \overline{OE} (active-low output-enable) inputs, and complementary OE and \overline{OE} inputs.

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TECHNICAL DOCUMENTS

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DATASHEET

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APPLICATION NOTES

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View Application Notes for Digital Logic

- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 Updated: 10/01/1996)
- Timing Differences of 10-pF Versus 50pF Loading (SCEA004 Updated: 11/01/1996)

RELATED DOCUMENTS

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View Related Documentation for <u>Digital Logic</u>

- Logic Reference Guide (SCYB004, 1032 KB Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

DEVICE INFOR	RMATION							INVENTORY STAT 00 PM GMT, 26 S		REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002			
ORDERABLE DEVICE	<u>STATUS</u>	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	<u>LEAD TIME</u>	DISTRIBUTOR COMPANY REGION	<u>IN STOCK</u>	PURCHASE	
SN74F241DW	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 0.27	25	<u>N/A*</u>	819 30 Sep	5 WKS				
								9614 04 Oct					
								>10k 11 Oct					
SN74F241DWR	ACTIVE	SOP 20	0 TO 70	<u>View Contents</u>	1KU 0.27	2000	<u>N/A*</u>	9614 04 Oct	5 WKS				
								>10k 11 Oct					
SN74F241N	ACTIVE	<u>PDIP</u> 20	0 TO 70	View Contents	1KU 0.27	20	<u>N/A*</u>	9614 07 Oct	5 WKS				
								>10k 14 Oct					
								7800 21 Oct					
SN74F241NSR	ACTIVE	SOP 20		View Contents	1KU 0.78	2000	<u>N/A*</u>	>10k 14 Oct	5 WKS				

Table Data Updated on: 9/26/2002