CY74FCT163374
CY74FCT163H374

16-Bit Registers

Features

- **5V tolerant Inputs and Outputs**
- **24 mA balanced drive outputs**
- **Low power, pin-compatible replacement for LCX, LPT, LVC, LVCH & LVT families**
- **FCT-C speed at 5.2 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 2.7V to 3.6V**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 3.3V, T_A= 25°C**

CY74FCT163H374 Features:

- **Bus hold on data inputs**
- **Eliminates the need for external pull-up or pull-down resistors**

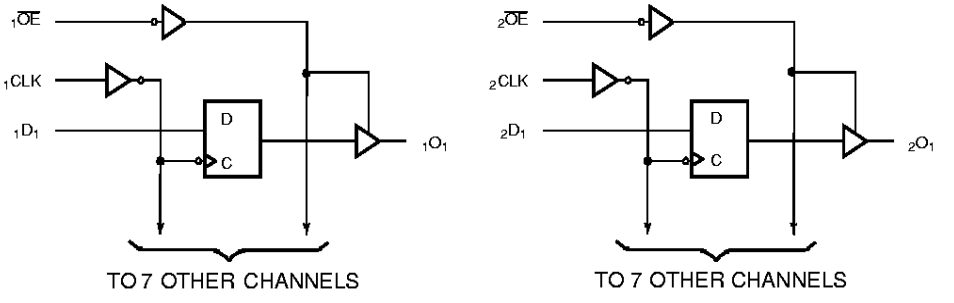
Functional Description

The CY74FCT163374 and CY74FCT163H374 are 16-bit D-type registers designed for use as buffered registers in high-speed, low power bus applications. These devices can be used as two independent 8-bit registers or as a single 16-bit register by connecting the output Enable (OE) and Clock (CLK) inputs. The outputs are 24-mA balanced output drivers with current limiting resistors to reduce the need for external terminating resistors and provide for minimal undershoot and reduced ground bounce. Flow-through pinout and small shrink packaging aid in simplifying board layout.

The CY74FCT163H374 has "bus hold" on the data inputs, which retain the input's last state whenever the source driving the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

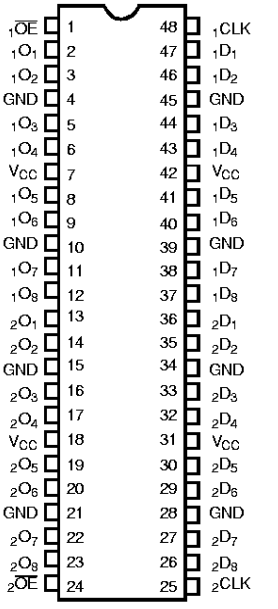
The CY74FCT163374 and the CY74FCT163H374 are designed with inputs and outputs capable of being driven by 5.0 V busses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power off disable feature enabling them to be used in applications requiring live insertion.

Logic Block Diagrams



Pin Configuration

SSOP/TSSOP
Top View



Function Table[1]

Inputs			Outputs	
D	CLK	$\overline{OE}$	O	Function
X	L	H	Z	High-Z
X	H	H	Z	
L	⌐	L	L	Load Register
H	⌐	L	H	
L	⌐	H	Z	
H	⌐	H	Z	

Pin Description

Name	Description
D	Data Inputs[2]
CLK	Clock Inputs
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
O	Three-State Outputs

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage Range..... 0.5V to +4.6V

DC Input Voltage ..... –0.5V to +7.0V

DC Output Voltage ..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... –60 to +120 mA

Power Dissipation..... 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	–40°C to +85°C	2.7V to3.6V

Electrical Characteristics Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description		Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage		All Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage						0.8	V
V_H	Input Hysteresis[6]					100		mV
V_{IK}	Input Clamp Diode Voltage		V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_{IH}	Input HIGH Current	Standard	V_{CC}=Max., V_I=V_{CC}				±1	µA
		Bus Hold					±100	
I_{IL}	Input LOW Current	Standard	V_{CC}=Max., V_I=GND				±1	µA
		Bus Hold					±100	
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[7]		V_{CC}=Min.	V_I=2.0V	–50			µA
				V_I=0.8V	+50			
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[7]		V_{CC}=Max., V_I=1.5V				±500	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	Standard	V_{CC}=Max., V_{OUT}=2.7V				±1	µA
		Bus Hold	V_{CC}=Max., V_{OUT}=V_{CC}				±1	
I_{OZL}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=GND				±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. ⌐ = LOW-to-HIGH Transition.
2. On the CY74FCT163H374, these pins have "bus hold."
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. Typical values are at V_{CC}=3.3V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Pins with bus hold are described in Pin Description.
8. V_{OH}=V_{CC}-0.6 V at rated current.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Electrical Characteristics Over the Operating Range V_{CC}=2.7V to 3.6V (continued)

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Current[9]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	50	90	200	mA
I_{ODH}	Output HIGH Current[9]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–36	–60	–110	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}= –0.1 mA	V_{CC}–0.2			V
		V_{CC}=3.0V, I_{OH}= –8 mA	2.4[8]	3.0		V
		V_{CC}=3.0V, I_{OH}= –24 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}= 0.1mA			0.2	V
		V_{CC}=Min., I_{OL}= 24 mA		0.3	0.5	
I_{OS}	Short Circuit Current[9]	V_{CC}=Max., V_{OUT}=GND	–60	–135	–240	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±100	µA

Capacitance[6] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V, V_{IN}≥V_{CC}–0.2V	0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=V_{CC}–0.6V[10]	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	50	75	µA/MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_0=10 MHz, f_1=5 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	0.5	0.8	mA
			V_{IN}=V_{CC}–0.6V or V_{IN}=GND	0.5	0.8	mA
		V_{CC}=Max., f_0=10 MHz, f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	2.5	3.8[13]	mA
			V_{IN}=V_{CC}–0.6V or V_{IN}=GND	2.5	4.0[13]	mA

Notes:

10. Per TTL driven input; all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = I_{CC}+$\Delta I_{CC} D_H N_T$+$I_{CCD}(f_0 N_C/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    N_C = Number of clock inputs changing at f_1
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range V_{CC}=3.0V to 3.6V[14,15]

Parameter	Description	CY74FCT163374A CY74FCT163H374A		CY74FCT163374C CY74FCT163H374C		Unit	Fig. No.[16]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay CLK to O	2.0	6.5	2.0	5.2	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.5	1.5	5.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.5	1.5	5.0	ns	1, 7, 8
t_{SU}	Set-Up Time HIGH or LOW, D to CLK	2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW, D to CLK	1.5		1.5		ns	4
t_W	CLK Pulse Width HIGH or LOW	5.0		3.3		ns	5
$t_{SK(O)}$	Output Skew[17]		0.5		0.5	ns	

14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. For V_{CC} =2.7, propagation delay, output enable and output disable times should be degraded by 20%
16. See "Parameter Measurement Information" in the General Information section.
17. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Ordering Information CY74FCT163374

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT163374CPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163374CPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT163374APAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163374APVC	O48	48-Lead (300-Mil) SSOP	

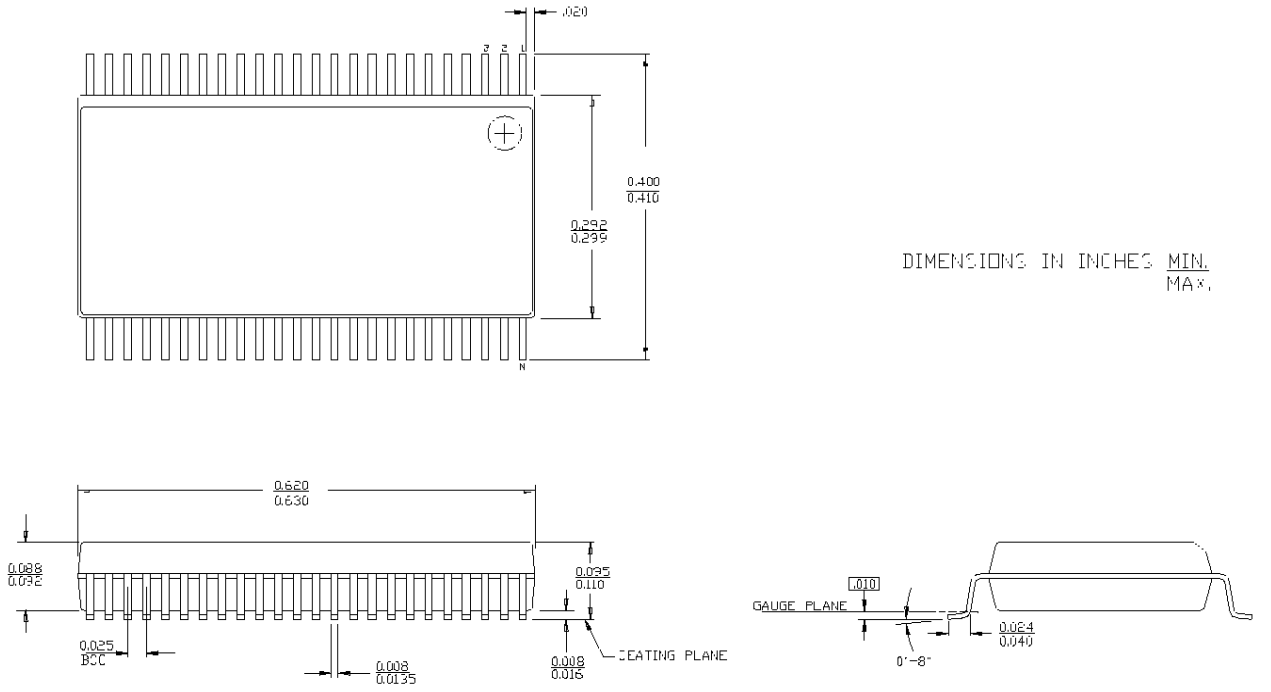
Ordering Information CY74FCT163H374

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT163H374CPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163H374CPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT163H374APAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163H374APVC	O48	48-Lead (300-Mil) SSOP	

Document #: 38-00577

Package Diagrams

48-Lead Shrunk Small Outline Package O48



48-Lead Thin Shrunk Small Outline Package Z48