Octal transceiver/register with dual enable; 3-state; inverting

74HL33651

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33651 consist of 8 inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropiate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE_n inputs this operating mode permits. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input.

The '651' is functionally identical to the '652', but has inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.4	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33651D	28	SO	plastic	SOT136-1
74HL33651DB	28	SSOP	plastic	SOT341-1
74HL33651PW	28	TSSOP	plastic	SOT361-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	output enable A to B input
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ to $\overline{A}_7$	'A' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	$\overline{OE}_{BA}$	output enable B to A input (active LOW)
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ to $\overline{B}_7$	'B' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

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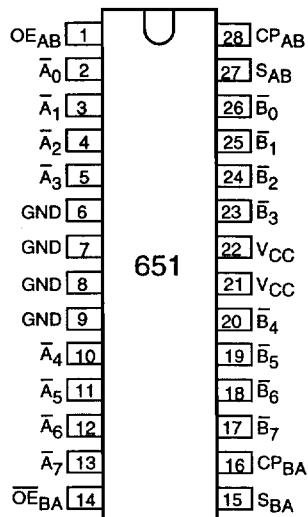
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Fig.1 Pin configuration.
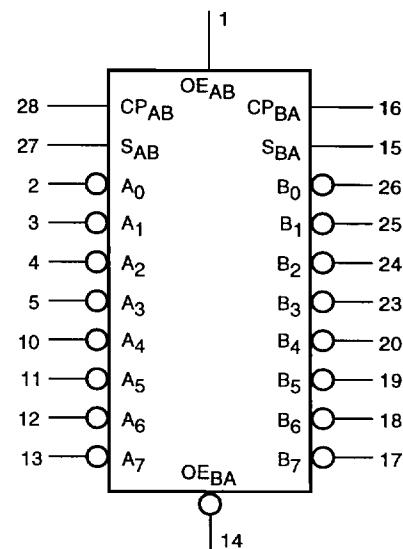
Fig.2 Logic symbol.
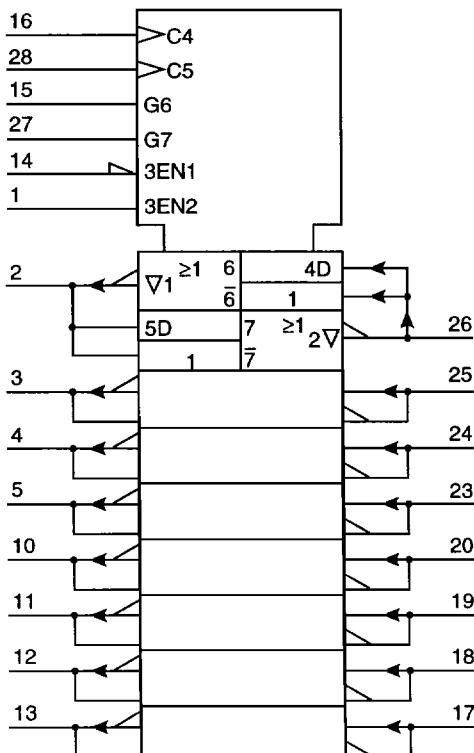
Fig3. IEC logic symbol.
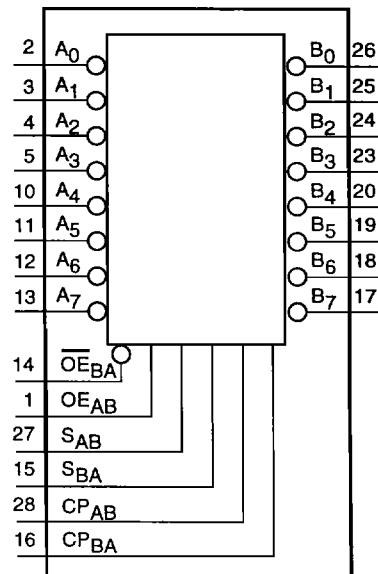
Fig.4 Functional diagram.

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Fig.5 Logic diagram.
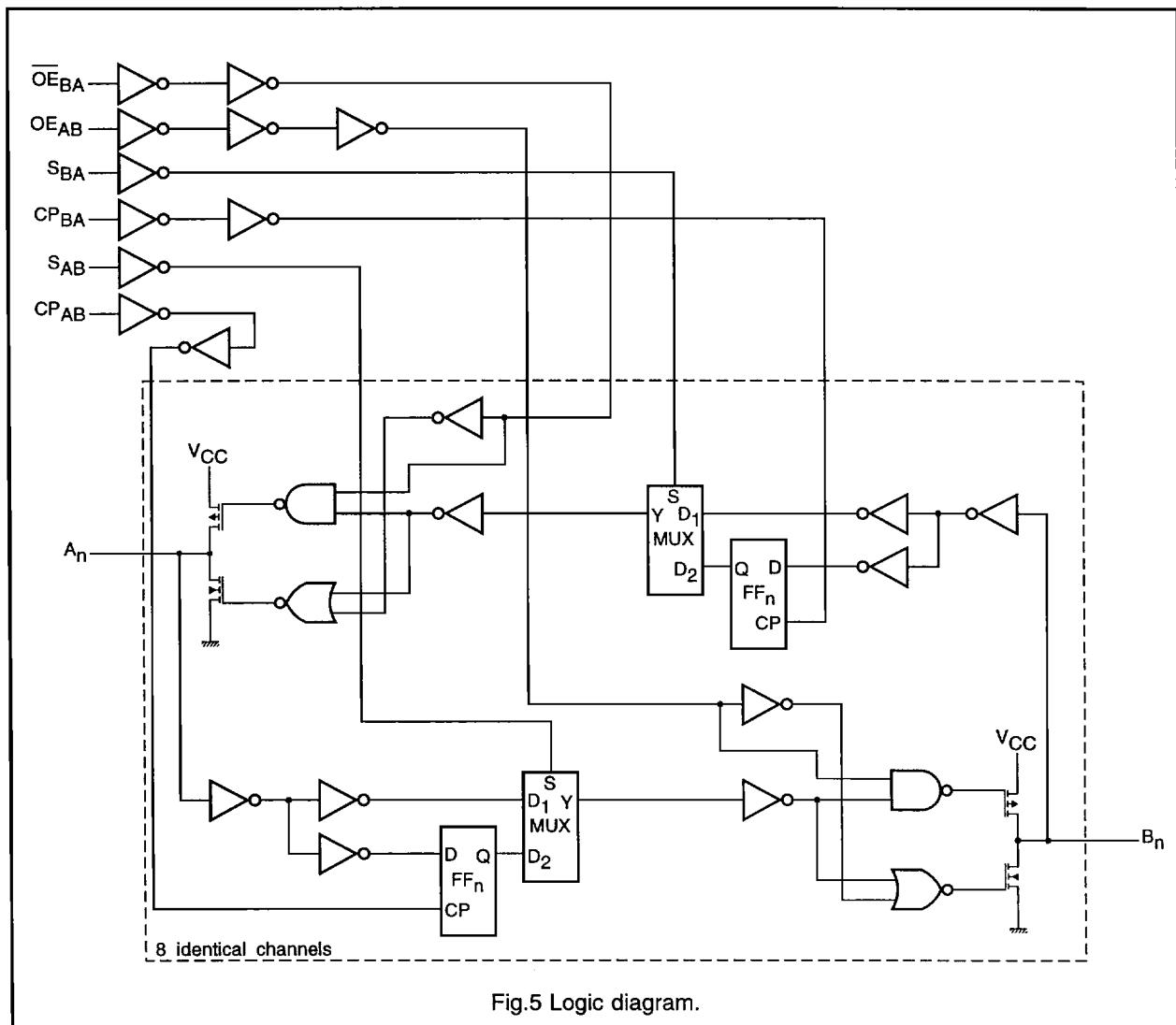
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FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ to $\overline{A}_7$	$\overline{B}_0$ to $\overline{B}_7$	
L	H	H or L	H or L	X	X	input	input	isolation
L	H	↑	↑	X	X			store $\overline{A}$ and $\overline{B}$ data
X	H	↑	H or L	X	X	input	un*	store A, hold B
H	H	↑	↑	L	X	input	output	store A in both registers
L	X	H or L	↑	X	X	un*	input	hold A, store B
L	L	↑	↑	X	L	output	input	store B in both registers
L	L	X	X	X	L	output	input	real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			stored $\overline{B}$ data to A bus
H	H	X	X	L	X	input	output	real-time $\overline{A}$ data to B bus
H	H	H or L	X	H	X			stored $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	output	output	stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

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DC CHARACTERISTICS FOR 74HL33651

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

I_{cc} category: MSI

AC CHARACTERISTICS FOR 74HL33651

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{cc} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$, $\overline{B}_n$ to $\overline{B}_n$, $\overline{A}_n$	−	19.5	−	22.4	ns	1.2	Fig.6
		−	7.3	−	8.4		2.0	
		−	4.9	−	5.6		3.0	
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to $\overline{B}_n$, $\overline{A}_n$	−	23.2	−	26.8	ns	1.2	Fig.7
		−	8.7	−	10.1		2.0	
		−	5.8	−	6.7		3.0	
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to $\overline{B}_n$, $\overline{A}_n$	−	24.4	−	28.0	ns	1.2	Fig.8
		−	9.2	−	10.5		2.0	
		−	6.1	−	7.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to $\overline{B}_n$	−	22.0	−	25.2	ns	1.2	Fig.9
		−	8.3	−	7.8		2.0	
		−	5.5	−	6.3		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to $\overline{B}_n$	−	17.5	−	20.2	ns	1.2	Fig.9
		−	7.3	−	8.4		2.0	
		−	5.3	−	6.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$	−	22.0	−	25.2	ns	1.2	Fig.9
		−	8.3	−	9.5		2.0	
		−	5.5	−	6.3		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$	−	17.5	−	20.3	ns	1.2	Fig.9
		−	7.4	−	8.4		2.0	
		−	5.3	−	6.0		3.0	
t_w	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0	−	3.7	−	ns	2.0	Figs 6 and 8
		2.0	−	2.5	−		3.0	
t_{su}	set-up time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	−	−	−	−	ns	1.2	Fig.7
		−	−	−	−		2.0	
		1.0	−	1.0	−		3.0	
t_h	hold time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	−	−	−	−	ns	1.2	Fig.7
		−	−	−	−		2.0	
		1.0	−	1.0	−		3.0	
f_{max}	maximum clock pulse frequency	150	−	100	−	MHz	2.0	Fig.7
		200	−	150	−		3.0	

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AC WAVEFORMS
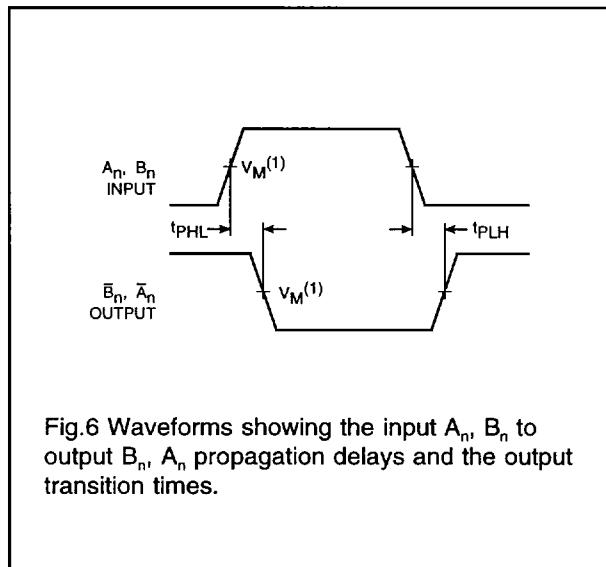
Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.
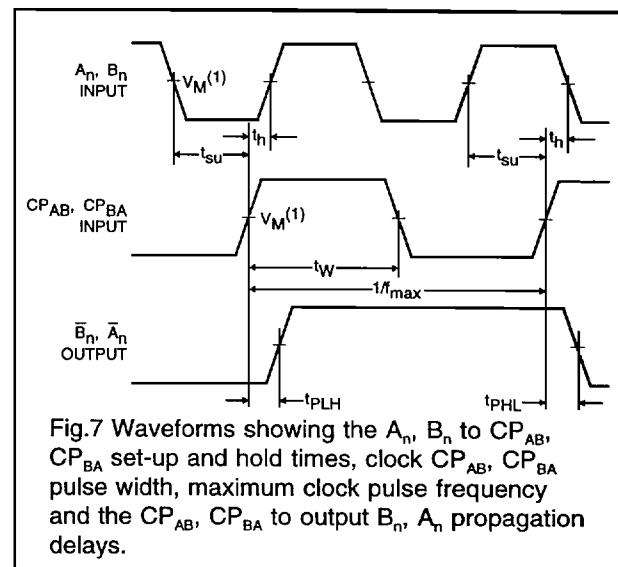

Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.
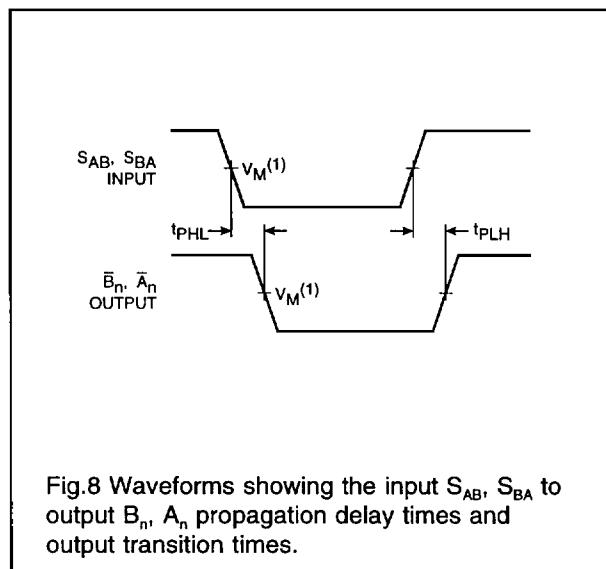

Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and output transition times.
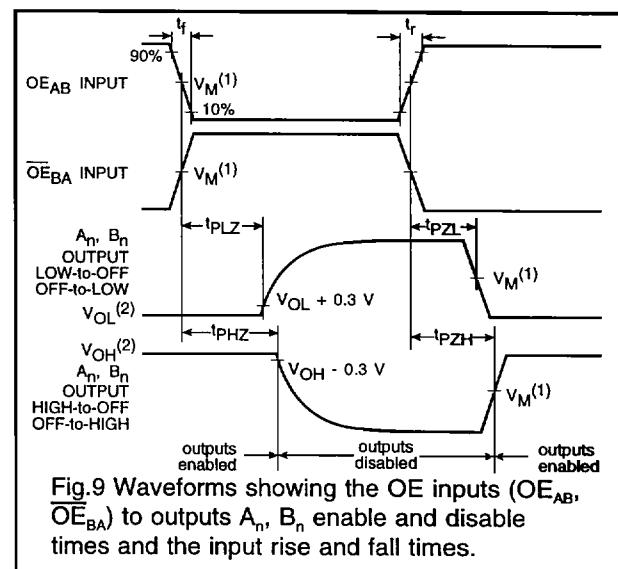

Fig.9 Waveforms showing the OE inputs (OE$_{AB}$, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times and the input rise and fall times.

Notes:
   (1) $V_M = 0.6$ V at $V_{CC} = 1.2$ V.
              $V_M = 1.0$ V at $V_{CC} = 2.0$ V.
              $V_M = 1.5$ V at $V_{CC} = 3.0$ V.
   (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

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### APPLICATION INFORMATION

Real-time transfer; bus B to bus A

OE_AB	OE̅_BA	CP_AB	CP_BA	S_AB	S_BA
L	L	X	X	X	L
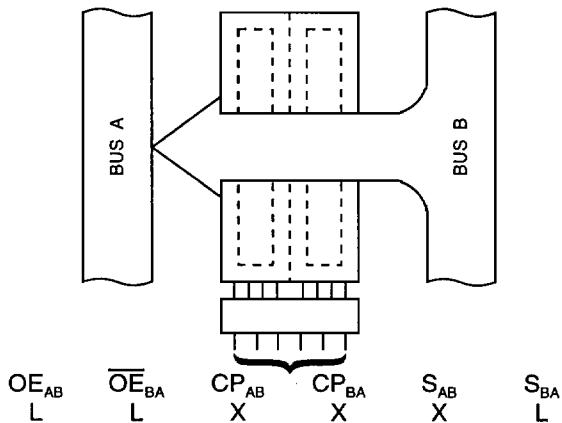
Real-time transfer; bus A to bus B

OE_AB	OE̅_BA	CP_AB	CP_BA	S_AB	S_BA
H	H	X	X	L	X
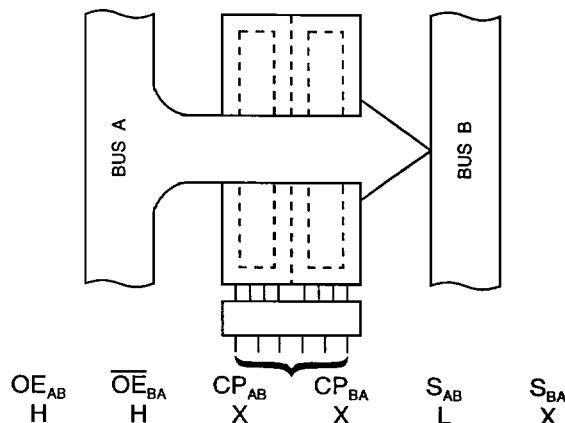
Store A, B or A and B in one register

OE_AB	OE̅_BA	CP_AB	CP_BA	S_AB	S_BA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X
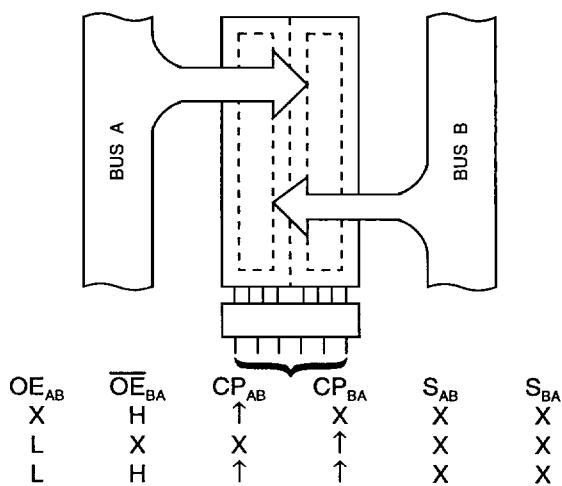
Transfer A stored data to B bus or B stored data to A bus or both at the same time

OE_AB	OE̅_BA	CP_AB	CP_BA	S_AB	S_BA
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H
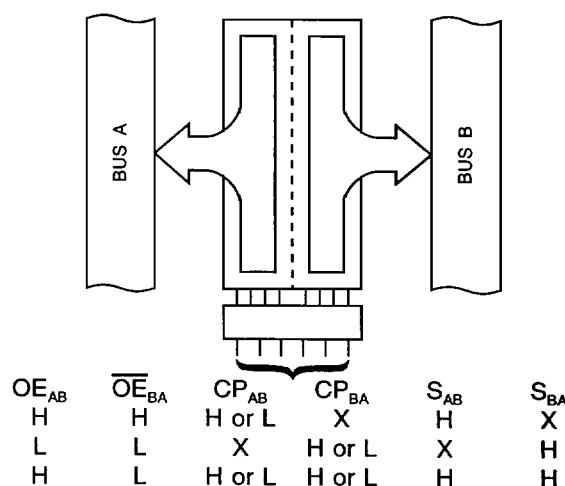
Store bus A in both registers or store bus B in both registers

OE_AB	OE̅_BA	CP_AB	CP_BA	S_AB	S_BA
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation

OE_AB	OE̅_BA	CP_AB	CP_BA	S_AB	S_BA
L	H	H or L	H or L	X	X