



# 3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

**IDT74ALVCH16601**

## FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$ , Normal Range
- $V_{cc} = 2.7V$  to  $3.6V$ , Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels ( $0.4\mu W$  typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP and TSSOP packages

## DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Suitable for heavy loads

## APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

## DESCRIPTION:

This 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. The ALVCH16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

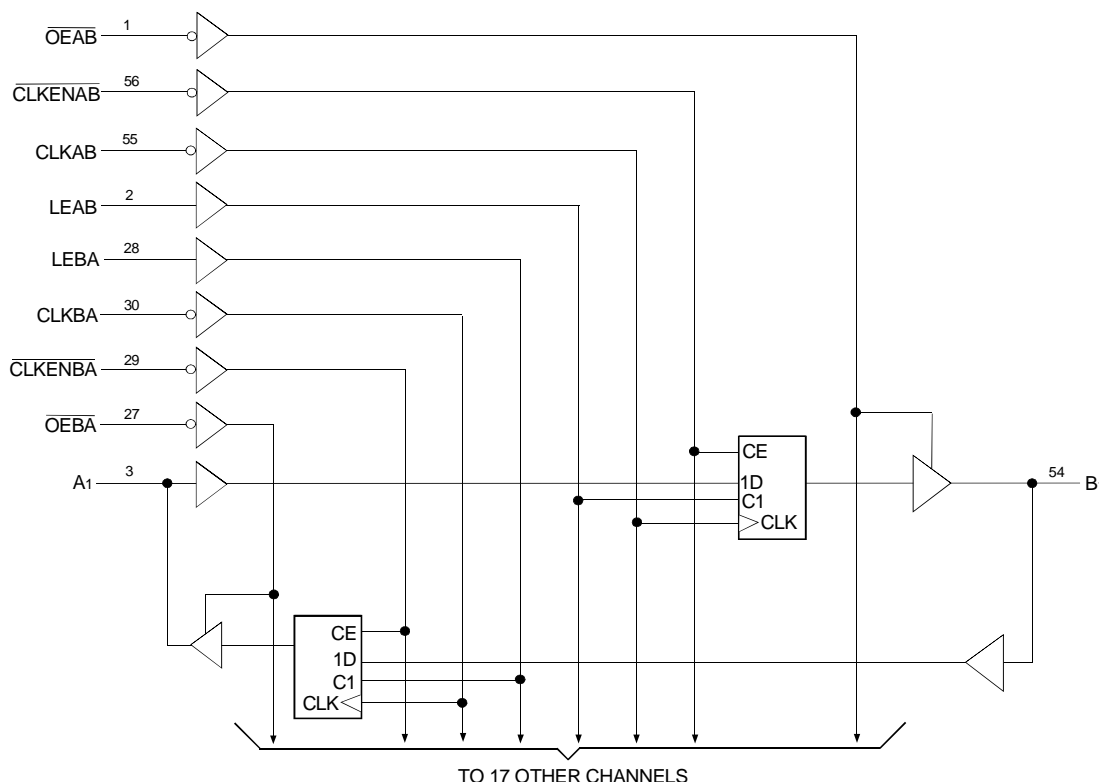
Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ( $\overline{CLKENAB}$  and  $\overline{CLKENBA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable  $\overline{OEAB}$  is active low. When  $\overline{OEAB}$  is low, the outputs are active. When  $\overline{OEAB}$  is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses  $\overline{OEBA}$ , LEBA, CLKBA and  $\overline{CLKENBA}$ .

The ALVCH16601 has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16601 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM

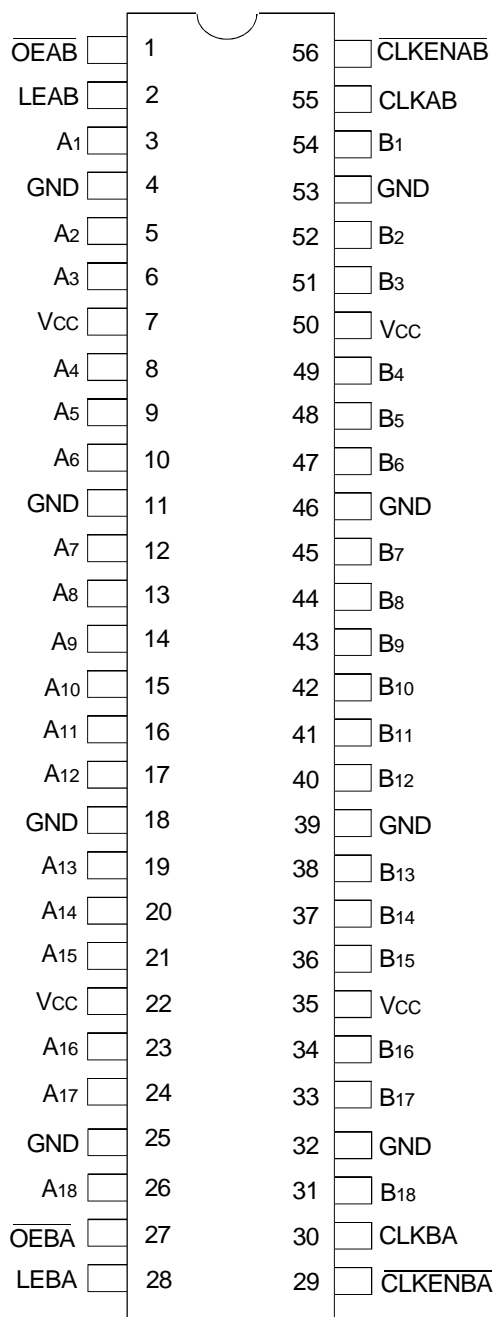


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INDUSTRIAL TEMPERATURE RANGE

JANUARY 2004

## PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	±50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A <sub>x</sub>	A-to-B Data Inputs or B-to-A 3-State Outputs <sup>(1)</sup>
B <sub>x</sub>	B-to-A Data Inputs or A-to-B 3-State Outputs <sup>(1)</sup>
$\overline{CLKENAB}$	A-to-B Clock Enable Input (Active LOW)
$\overline{CLKENBA}$	B-to-A Clock Enable Input (Active LOW)

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE<sup>(1,2)</sup>

Inputs					Output
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	Ax	Bx
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B <sup>(3)</sup>
H	L	L	X	X	B <sup>(3)</sup>
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L or H	X	B <sup>(3)</sup>

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses  $\overline{\text{OEBA}}$ , LEBA, and CLKBA, and CLKENBA.
2. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
↑ = LOW-to-HIGH transition
3. Level of B before the indicated steady-state inputs were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	Vi = VCC	—	—	±5	µA
IiL	Input LOW Current	VCC = 3.6V	Vi = GND	—	—	±5	µA
IoZH IoZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V		—	—	±10	µA
		Vo = GND		—	—	±10	
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = 3.6V VIN = GND or VCC		—	0.1	40	µA
ΔICC	Quiescent Power Supply Current Variation	One input at VCC - 0.6V, other inputs at VCC or GND		—	—	750	µA

NOTE:

1. Typical values are at VCC = 3.3V, +25°C ambient.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3V	V <sub>I</sub> = 2V	-75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	-45	—	—	μA
			V <sub>I</sub> = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	±500	μA

**NOTES:**

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3V		2.4	—	
			V <sub>CC</sub> = 3V	I <sub>OH</sub> = -24mA	2	
VOL	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3V	I <sub>OL</sub> = 24mA	—	0.55	

**NOTE:**

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = -40°C to +85°C.

## OPERATING CHARACTERISTICS, T<sub>A</sub> = 25°C

Symbol	Parameter	Test Conditions	V <sub>CC</sub> = 2.5V ± 0.2V	V <sub>CC</sub> = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C <sub>L</sub> = 0pF, f = 10Mhz	41	52	pF
CPD	Power Dissipation Capacitance Outputs disabled		6	6	

SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>MAX</sub>		150	—	150	—	150	—	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ax to Bx or Bx to Ax	1	4	—	4.6	—	4.1	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEAB to Bx or LEBA to Ax	1	4.6	—	5.3	—	4.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLKAB to Bx or CLKBA to Ax	1.2	5.2	—	5.8	—	5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OEAB}$ to Bx or $\overline{OEBA}$ to Ax	1.1	5.3	—	6.1	—	5.2	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OEAB}$ to Bx or $\overline{OEBA}$ to Ax	1.4	4.9	—	4.8	—	4.4	ns
t <sub>SU</sub>	Set-up Time, data before CLK↑	2.3	—	2.4	—	2.1	—	ns
t <sub>SU</sub>	Set-up Time, data before LE↓, CLK HIGH	2	—	1.6	—	1.6	—	ns
t <sub>SU</sub>	Set-up Time, data before LE↓, CLK LOW	1.3	—	1.2	—	1.1	—	ns
t <sub>SU</sub>	Set-up Time, $\overline{CLKEN}$ before CLK↑	2	—	2	—	1.7	—	ns
t <sub>H</sub>	Hold Time, data after CLK↑	0.7	—	0.7	—	0.8	—	ns
t <sub>H</sub>	Hold Time, data after LE↓, CLK HIGH	1.3	—	1.6	—	1.4	—	ns
t <sub>H</sub>	Hold Time, data after LE↓, CLK LOW	1.7	—	2	—	1.7	—	ns
t <sub>H</sub>	Hold Time, $\overline{CLKEN}$ after CLK↑	0.3	—	0.5	—	0.6	—	ns
t <sub>w</sub>	Pulse Width, LE HIGH	3.3	—	3.3	—	3.3	—	ns
t <sub>w</sub>	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t <sub>sk(0)</sub>	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

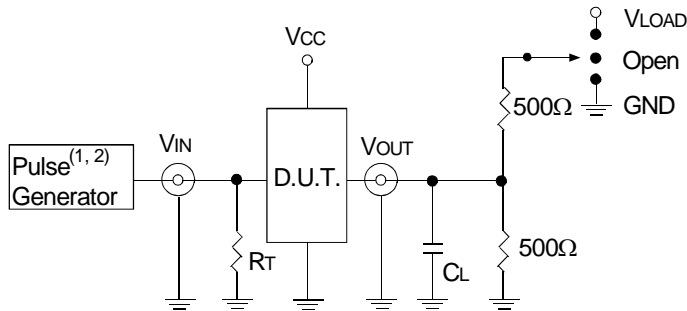
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. T<sub>A</sub> = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> = 3.3V ± 0.3V	V <sub>CC</sub> <sup>(1)</sup> = 2.7V	V <sub>CC</sub> <sup>(2)</sup> = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

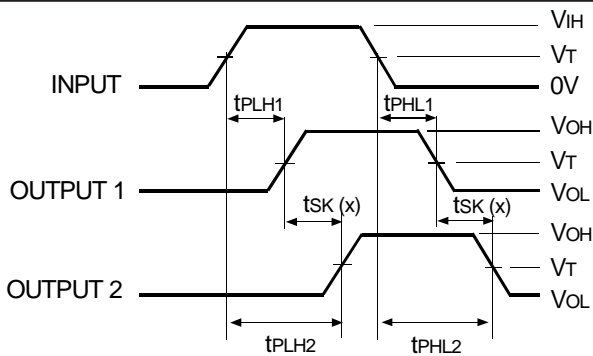
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open

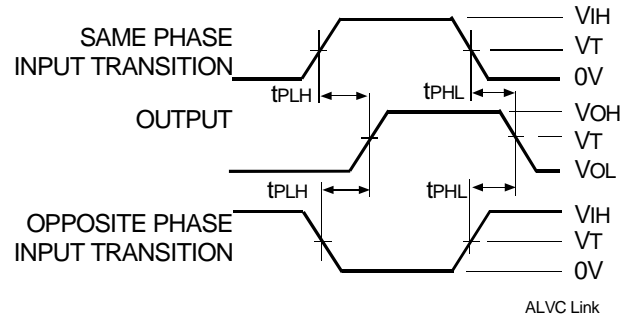


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

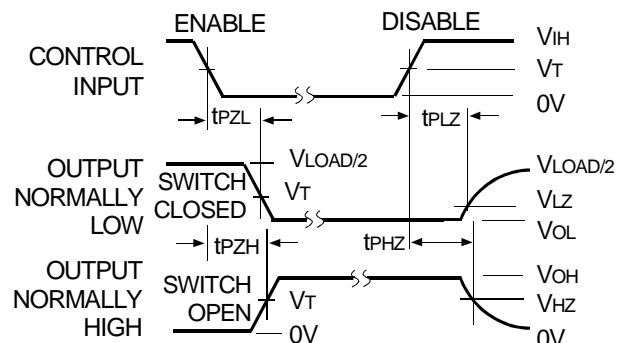
Output Skew - t<sub>SK</sub>(x)

#### NOTES:

1. For t<sub>SK</sub>(a) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.



Propagation Delay

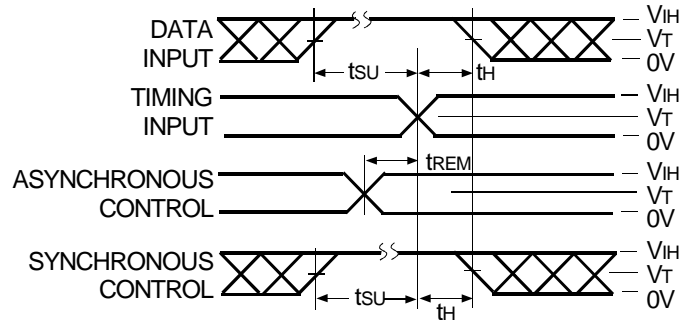


ALVC Link

#### Enable and Disable Times

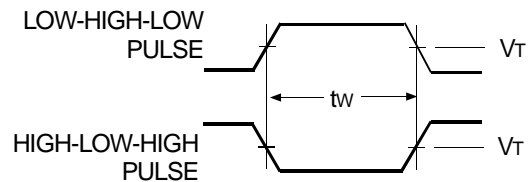
#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



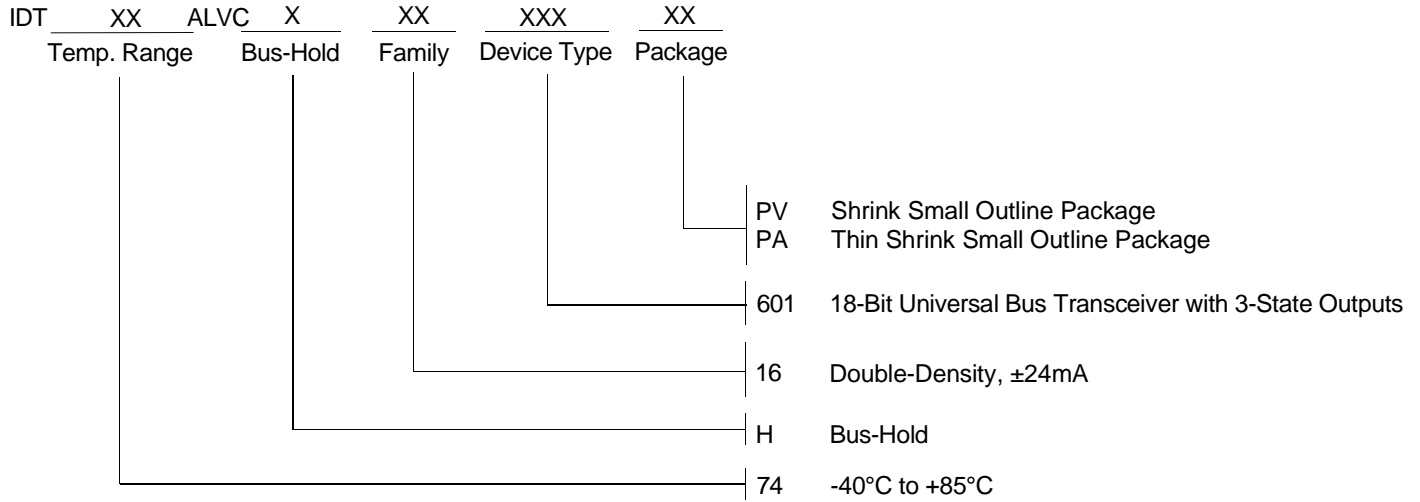
ALVC Link

#### Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION



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