



# CY74FCT16374T CY74FCT162374T

## 16-Bit Registers

### Features

- Low power, pin-compatible replacement for ABT functions
- FCT-C speed at 5.2 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000 V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 5V \pm 10\%$

### CY74FCT16374T Features:

- 64 mA sink current (Com'1), 32 mA source current (Com'1)
- Typical  $V_{OLP}$  (ground bounce) < 1.0V at  $V_{CC} = 5V, T_A = 25^\circ C$

### CY74FCT162374T Features:

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) < 0.6V at  $V_{CC} = 5V, T_A = 25^\circ C$

### Functional Description

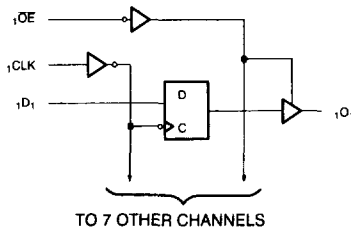
CY74FCT16374T and CY74FCT162374T are 16-bit D-type registers designed for use as buffered registers in high-speed, low power bus applications. These devices can be used as two independent

8-bit registers or as a single 16-bit register by connecting the output Enable (OE) and Clock (CLK) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout. The output buffers are designed with power-off disable feature that allows live insertion of boards.

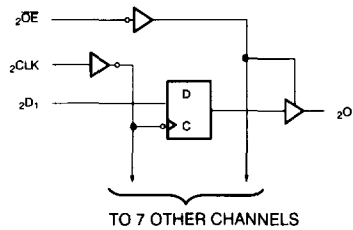
The CY74FCT16374T is ideally suited for driving high capacitance loads and low-impedance backplanes.

The CY74FCT162374T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162374T is ideal for driving transmission lines.

### Logic Block Diagrams

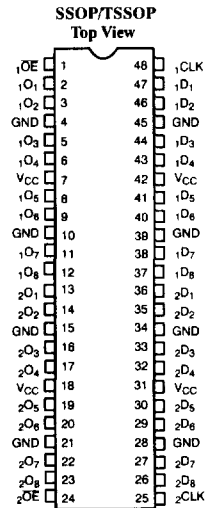


FCT162374-1



FCT162374-2

### Pin Configuration



FCT162374-3



**Function Table<sup>[1]</sup>**

Inputs			Outputs	Function
D	CLK	OE	O	
X	L	H	Z	High-Z
X	H	H	Z	
L	↕	L	L	Load Register
H	↕	L	H	
L	↕	H	Z	
H	↕	H	Z	

**Maximum Ratings<sup>[2, 3]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	Com'l	-55°C to +125°C
Ambient Temperature with Power Applied	Com'l	-55°C to +125°C
DC Input Voltage		-0.5V to +7.0V
DC Output Voltage		-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)		-60 to +120 mA

**Pin Description**

Name	Description
D	Data Inputs
CLK	Clock Inputs
OE	Three-State Output Enable Inputs (Active LOW)
O	Three-State Outputs

Power Dissipation	1.0W
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[5]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>			±1	µA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>I</sub> =GND			±1	µA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	µA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	µA
I <sub>OS</sub>	Short Circuit Current <sup>[6]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[6]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>ON</sub>	Power Off Input Current	V <sub>IN</sub> =0V, V <sub>CC</sub> =5.5V			±1	µA

**Notes:**

- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = HIGH Impedance, ↕ = LOW-to-HIGH Transition.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Output Drive Characteristics for CY74FCT16374T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

**Output Drive Characteristics for CY74FCT162374T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[6]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[6]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA		0.3	0.55	V

**Capacitance<sup>[5]</sup> (T<sub>A</sub> = +25°C, f = 1.0 MHz)**

Parameter	Description	Test Conditions	Typ. <sup>[4]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[4]</sup>	Max.	Unit	
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max. V <sub>IN</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V	5	500	μA	
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max. V <sub>IN</sub> =3.4V <sup>[7]</sup>	0.5	1.5	mA	
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[8]</sup>	V <sub>CC</sub> =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND	60	100	μA/MHz	
I <sub>C</sub>	Total Power Supply Current <sup>[9]</sup>	V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, f <sub>1</sub> =5 MHz 50% Duty Cycle, Outputs Open, One Bit Toggling, OE=GND	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	0.6	1.5	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, f <sub>1</sub> =2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, OE=GND	V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	1.1	3.0	mA
			V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	3.0	5.5 <sup>[10]</sup>	mA
			V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	7.5	19.0 <sup>[10]</sup>	mA

**Notes:**

- Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub> · D<sub>IH</sub> · N<sub>T</sub> + I<sub>CCD</sub> · (f<sub>0</sub> · 2 + f<sub>1</sub> · N<sub>I</sub>)  
I<sub>CC</sub> = Quiescent Current with CMOS input levels  
ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
D<sub>IH</sub> = Duty Cycle for TTL inputs HIGH

- N<sub>T</sub> = Number of TTL inputs at D<sub>IH</sub>  
I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)  
f<sub>0</sub> = Clock frequency for registered devices, otherwise zero  
f<sub>1</sub> = Input signal frequency  
N<sub>I</sub> = Number of inputs changing at f<sub>1</sub>  
All currents are in milliamps and all frequencies are in megahertz.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.



**Switching Characteristics Over the Operating Range**

Parameter	Description	CY74FCT16374T CY74FCT162374T		CY74FCT16374AT CY74FCT162374AT		CY74FCT16374CT CY74FCT162374CT		Unit	Fig. No. <sup>[12]</sup>
		Min. <sup>[11]</sup>	Max.	Min. <sup>[11]</sup>	Max.	Min. <sup>[11]</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLK to O	2.0	10.0	2.0	6.5	2.0	5.2	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	12.5	1.5	6.5	1.5	5.5	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	8.0	1.5	5.5	1.5	5.0	ns	1, 7, 8
t <sub>SU</sub>	Set-Up Time HIGH or LOW, D to CLK	2.0		2.0		2.0		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW, D to CLK	1.5		1.5		1.5		ns	4
t <sub>w</sub>	CLK Pulse Width HIGH or LOW	5.0		5.0		3.3		ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[13]</sup>		0.5		0.5		0.5	ns	

**Ordering Information CY74FCT16374**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT16374CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16374CTPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16374ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16374ATPVC	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT16374TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16374TPVC	O48	48-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT162374**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT162374CTPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162374CTPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT162374ATPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162374ATPVC	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT162374TPAC	Z48	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162374TPVC	O48	48-Lead (300-Mil) SSOP	

**Notes:**

11. Minimum limits are guaranteed but not tested on Propagation Delays.  
 12. See "Parameter Measurement Information" in the General Information Section.

13. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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