National Semiconductor

74FR74•74FR1074
Dual D-Type Flip-Flop

General Description

The 'FR74 and 'FR1074 are dual D-type flip-flops with true and complement ($Q/\overline{Q}$) outputs. On the 'FR74, data at the D inputs is transferred to the outputs on the rising edge of the clock input (CPn). The 'FR1074 is the negative edge triggered version of this device. Both parts feature asynchronous clear (CDn) and set (SDn) inputs which are low level enabled.

Features

- 'FR74 is pin-for-pin compatible with the 'F74
- True 150 MHz f_{max} capability on 'FR74
- Outputs sink 24 mA and source 24 mA
- Guaranteed pin-to-pin skew specifications

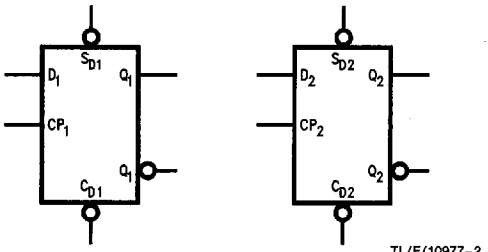
Ordering Code: See Section 11

Commercial	Package Number	Package Description
74FR74PC	N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
74FR74SC (Note 1)	M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74FR1074PC	N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
74FR1074SC (Note 1)	M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

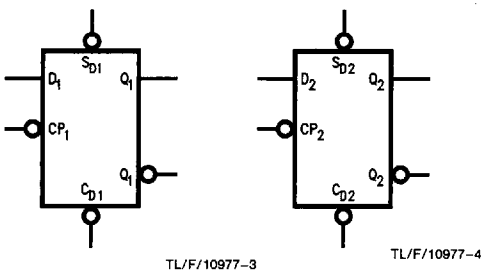
Logic Symbols

'FR74



TL/F/10977–1 TL/F/10977–2

'FR1074



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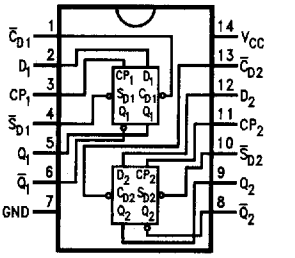
Connection Diagrams

Pin Assignment for SOIC and DIP 'FR74



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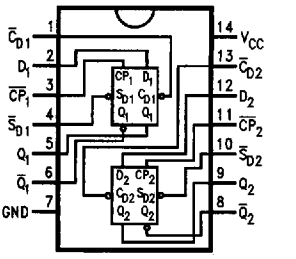
'FR1074



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Truth Tables

'FR74

Inputs				Outputs	
$\overline{SD}$	$\overline{CD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance
X = Immaterial
↗ = Rising Edge
Q_0 = Previous Q($\overline{Q}$) before LOW-to-HIGH Clock Transition

'FR1074

Inputs				Outputs	
$\overline{SD}$	$\overline{CD}$	$\overline{CP}$	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↘	H	H	L
H	H	↘	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance
X = Immaterial
↘ = Falling Edge
Q_0 = Previous Q($\overline{Q}$) before HIGH-to-LOW Clock Transition

Pin Descriptions

Pin Names	Description
Dn	Data Inputs
CPn	Clock Inputs
SDn	Asynchronous Set Inputs
CDn	Asynchronous Clear Inputs
Qn	True Output
$\overline{Q}$n	Complementary Output

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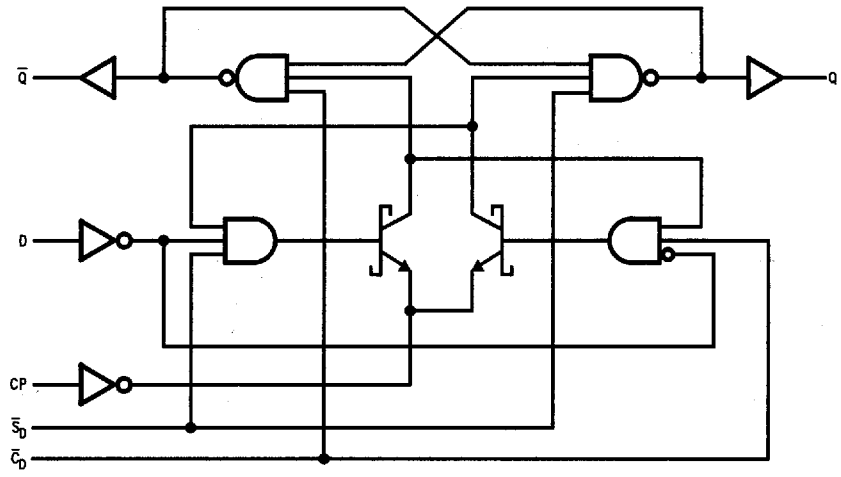
Logic Diagrams

'FR74



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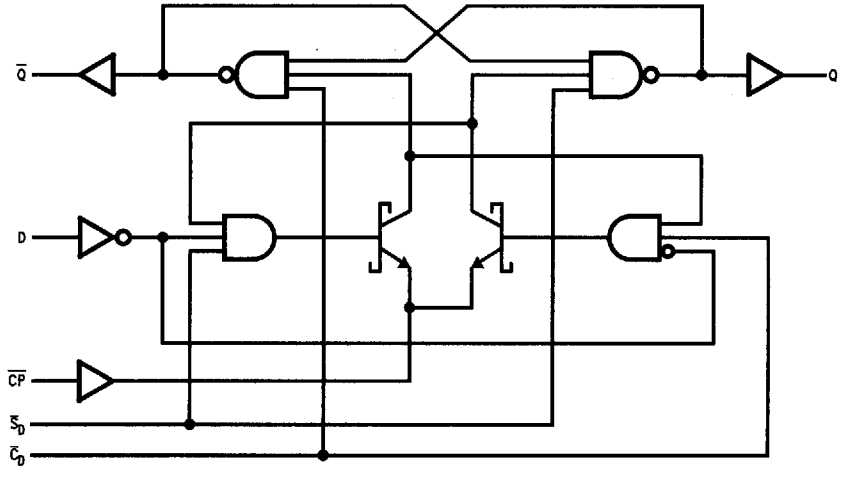
'FR1074



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Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V) Standard Output	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74FR74/74FR1074			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.5			V	Min	I_{OH} = −1 mA
		2.4			V	Min	I_{OH} = −3 mA
		2.0			V	Min	I_{OH} = −24 mA
V_{OL}	Output LOW Voltage			0.5	V	Min	I_{OL} = 24 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−150	μA	Max	V_{IN} = 0.5V (Dn, CPn)
				−1.8	mA	Max	V_{IN} = 0.5V (CDn, SDn)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, All Other Pins Grounded
I_{OD}	Output Circuit Leakage Test			3.75	V	0.0	V_{IOD} = 150 mV, All Other Pins Grounded
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
I_{CC}	Power Supply Current			24	mA	Max	

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74FR74 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74FR74 $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	150	190		150		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q_n}$	2.5 2.5	3.5 4.5	5.0 6.0	2.5 2.5	5.0 6.0	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{CD}n$ or $\overline{SD}n$ to Qn or $\overline{Qn}$	1.5 2.0	3.5 5.5	5.5 7.0	1.5 2.0	5.5 7.0	ns	2–3
t_{OSHL} (Note 1)	Pin to Pin Skew for HL Transitions					1.0	ns	2–3
t_{OSLH} (Note 1)	Pin to Pin Skew for LH Transitions					1.0	ns	2–3
t_{OST} (Note 1)	Pin to Pin Skew for HL/LH Transitions					3.0	ns	2–3
$t_{Q/\overline{Q}}$ (Note 1)	True/Complement Output Skew					1.8	ns	2–3
t_{PS} (Note 1)	Pin (Signal) Transition Variation					1.8	ns	2–3

Note 1: Pin to Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). t_{OST} is guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74FR74 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		74FR74 $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF		Units	Fig. No.
		Min	Max	Min	Max		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW Dn to CPn	2.5 2.5		2.5 2.5		ns	2–6
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW Dn to CPn	0 0		0 0		ns	2–6
$t_W(H)$ $t_W(L)$ (Note 2)	CPn Pulse Width HIGH or LOW	3.3 3.3		3.3 3.3		ns	2–4
$t_W(L)$	$\overline{SD}n$ or $\overline{CD}n$ Pulse Width	4.0		4.0		ns	2–4
t_{rec}	Recovery Time $\overline{SD}n$ or $\overline{CD}n$ to CPn	2.0		2.0		ns	2–4

Note 2: This specification is guaranteed by design.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74FR1074 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74FR1074 $T_A =$ Comm $V_{CC} =$ Comm $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	120	160		120		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Qn}$	2.5 3.0	4.0 5.0	5.5 6.5	2.5 3.0	5.5 6.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{CD}n$ or $\overline{SD}n$ to Qn or $\overline{Qn}$	1.5 2.0	3.5 5.5	5.5 7.0	1.5 2.0	5.5 7.0	ns	2–3
t_{OSHL} (Note 1)	Pin to Pin Skew for HL Transitions					1.5	ns	2–3
t_{OSLH} (Note 1)	Pin to Pin Skew for LH Transitions					1.5	ns	2–3
t_{OST} (Note 1)	Pin to Pin Skew for HL/LH Transitions					3.5	ns	2–3
$t_{Q/\overline{Q}}$ (Note 1)	True/Complement Output Skew					2.0	ns	2–3
t_{PS} (Note 1)	Pin (Signal) Transition Variation					2.0	ns	2–3

Note 1: Pin to Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). t_{OST} is guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74FR1074 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		74FR1074 $T_A =$ Comm $V_{CC} =$ Comm $C_L = 50$ pF		Units	Fig. No.
		Min	Max	Min	Max		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW Dn to CPn	2.0 2.0		2.0 2.0		ns	2–6
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW Dn to CPn	0 0		0 0		ns	2–6
$t_W(H)$ $t_W(L)$ (Note 2)	$\overline{CP}n$ Pulse Width HIGH or LOW	3.3 3.3		3.3 3.3		ns	2–4
$t_W(L)$	$\overline{SD}n$ or $\overline{CD}n$ Pulse Width	4.0		4.0		ns	2–4
t_{rec}	Recovery Time $\overline{SD}n$ or $\overline{CD}n$ to CPn	2.0		2.0		ns	2–4

Note 2: This specification is guaranteed by design.