DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT137

3-to-8 line decoder/demultiplexer with address latches; inverting

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

3-to-8 line decoder/demultiplexer with address latches; inverting

74HC/HCT137

FEATURES

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT137 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT137 are 3-to-8 line decoder/demultiplexers with latches at the three address inputs (A_n). The “137” essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the “137” acts as a 3-to-8 active LOW decoder. When the latch enable ($\overline{LE}$) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH.

The output enable input ($\overline{E}_1$ and E_2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless $\overline{E}_1$ is LOW and E_2 is HIGH.

The “137” is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

QUICK REFERENCE DATA

GND = 0 V; T_{amb}= 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	A_n to $\overline{Y}_n$		18	19	ns
	$\overline{LE}$ to $\overline{Y}_n$		17	21	ns
	$\overline{E}_1$ to $\overline{Y}_n$		15	17	ns
	E_2 to $\overline{Y}_n$		15	15	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	57	59	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	data inputs
4	$\overline{LE}$	latch enable input (active LOW)
5	$\overline{E}_1$	data enable input (active LOW)
6	E_2	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	multiplexer outputs
16	V_{CC}	positive supply voltage

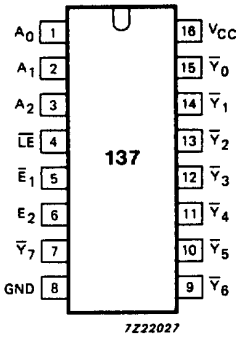


Fig.1 Pin configuration.

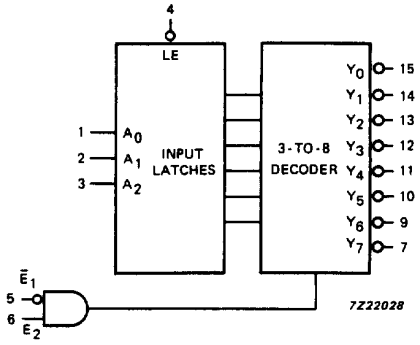


Fig.2 Logic symbol.

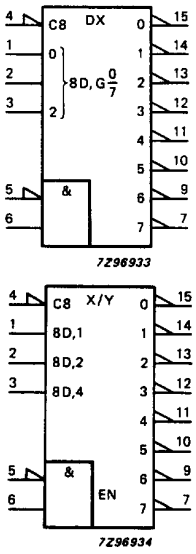


Fig.3 IEC logic symbol.

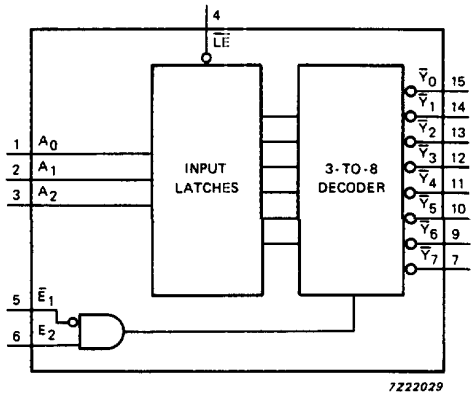


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E_2	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	L	H	X	X	X	stable							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

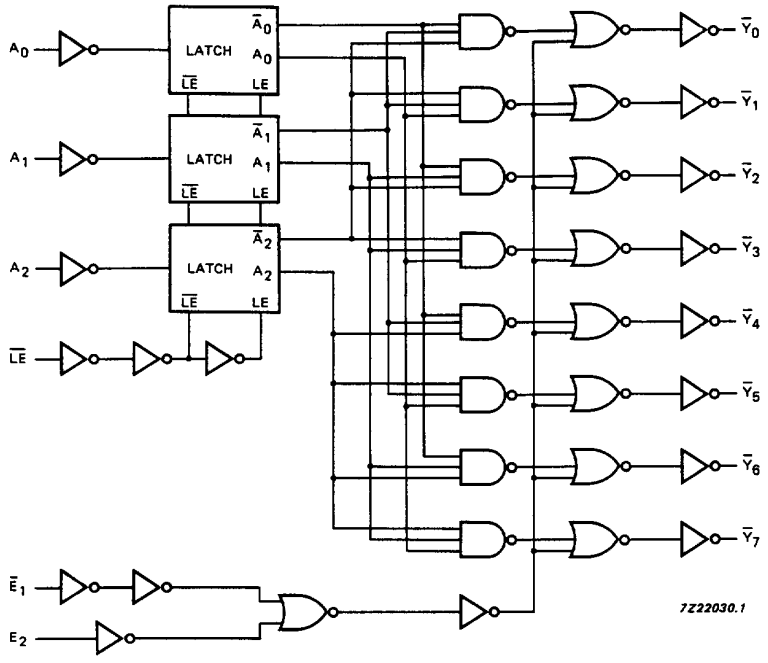


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}n$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to $\overline{Y}_n$		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}_1$ to $\overline{Y}_n$		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay E_2 to $\overline{Y}_n$		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	$\overline{LE}$ pulse width HIGH	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time A_n to $\overline{LE}$	50 10 9	3 1 1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.8
t_h	hold time A_n to $\overline{LE}$	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

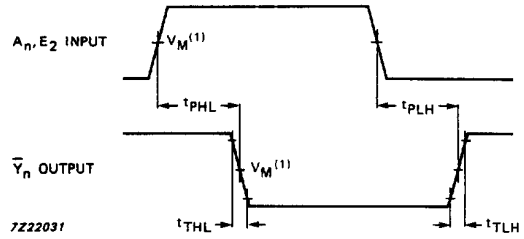
INPUT	UNIT LOAD COEFFICIENT
A_n	1.50
$\overline{E}_1$	1.50
E_2	1.50
$\overline{LE}$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

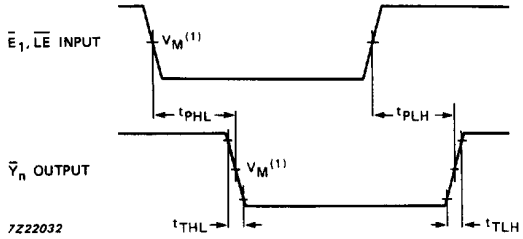
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		22	38		48		57	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to $\overline{Y}_n$		25	44		55		66	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}_1$ to $\overline{Y}_n$		20	37		46		56	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay E_2 to $\overline{Y}_n$		18	35		44		53	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t_W	$\overline{LE}$ pulse width HIGH	10	5		13		15		ns	4.5	Fig.8
t_{su}	set-up time A_n to $\overline{LE}$	10	2		13		15		ns	4.5	Fig.8
t_h	hold time A_n to $\overline{LE}$	7	2		9		11		ns	4.5	Fig.8

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the address input (A_n) and enable inputs (E_2) to output ($\overline{Y}_n$) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the enable input ($\overline{E}_1$, $\overline{LE}$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

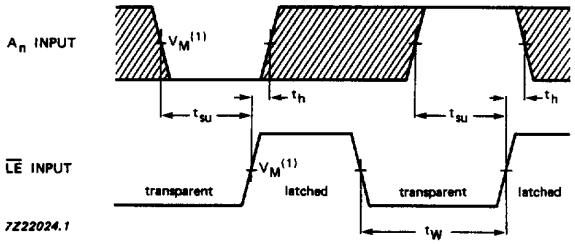


Fig.8 Waveforms showing the data set-up, hold times for A_n input to $\overline{LE}$ input and the latch enable pulse width.

APPLICATION INFORMATION

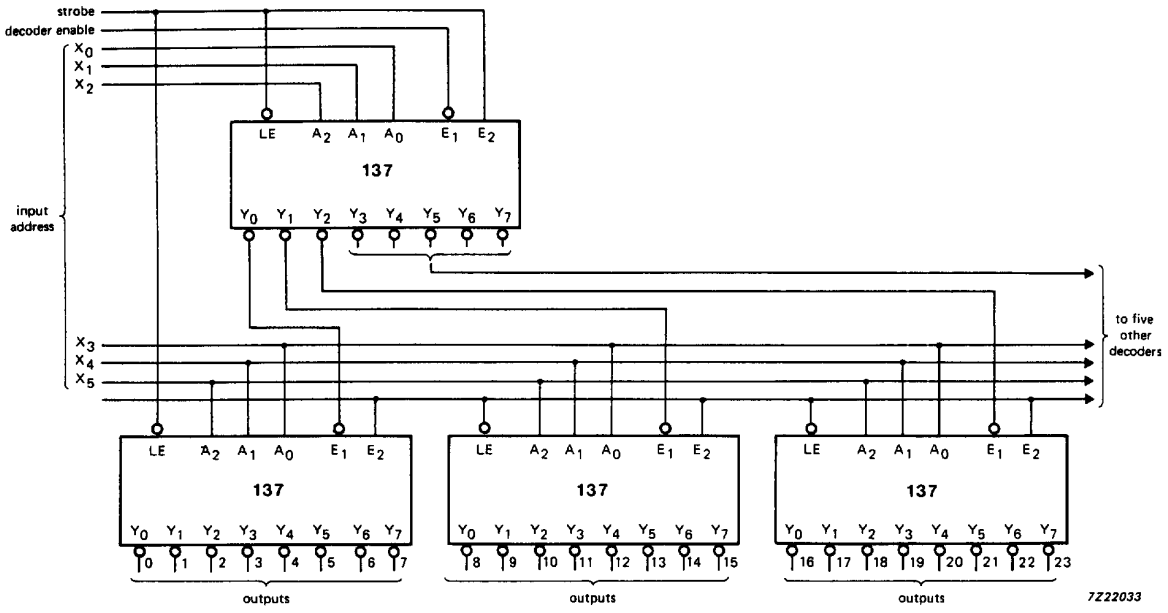


Fig.9 6-to-64 line decoder with input address storage.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

74HC/HCT137; 3-to-8 line decoder/demultiplexer with address latches; inverting

Information as of 2003-04-22

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General description

The 74HC/HCT137 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT137 are 3-to-8 line decoder/demultiplexers with latches at the three address inputs (A_n). The '137' essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled (LE = LOW), the '137' acts as a 3-to-8 active LOW decoder. When the latch enable (LE) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as LE remains HIGH.

The output enable input (E_1 and E_2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless E_1 is LOW and E_2 is HIGH.

The '137' is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

Features

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74HC/HCT137	3-to-8 line decoder/demultiplexer with address latches; inverting	12/1/1990	Product specification	8	66	Download

Additional datasheet info

To complete the device datasheet with package and family information, also download the following PDF files. The "Logic Package Information" document is required to determine in which package(s) this device is available.

	Document	Description
1	HCT_FAMILY_SPECIFICATIONS	HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications
2	HCT_PACKAGE_INFO	HC/T Package Info, The IC06 74HC/HCT/HCMOS Logic Package Information
3	HCT_PACKAGE_OUTLINES	HC/T Package Outlines, The IC06 74HC/HCT/HCMOS Logic Package Outlines

Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74HC137D	SOT109 (SO16)	3-to-8 Line Decoder/Demultiplexer with Address Latches; Inverting	15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low
74HC137DB	SOT338-1 (SSOP16)	3-to-8 Line Decoder/Demultiplexer with Address Latches; Inverting	15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low
74HC137N	SOT38-1 (DIP16)	3-to-8 Line Decoder/Demultiplexer with Address Latches; Inverting	15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low
74HCT137D	SOT109-1 (SO16)	3-to-8 Line Decoder/Demultiplexer with Address Latches; Inverting; TTL Enabled	15	5 Volts +	16	Low Power or Battery Applications	TTL	Low
74HCT137N	SOT38-1 (DIP16)	3-to-8 Line Decoder/Demultiplexer with Address Latches; Inverting; TTL Enabled	15	5 Volts +	16	Low Power or Battery Applications	TTL	Low

Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing Discretes packing info	Package	Device status	Buy online
74HC137D	74HC137D	9337 570 70652	Standard Marking * Bulk Pack, CECC	SOT109 (SO16)	Full production	order this
	74HC137D-T	9337 570 70653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT109 (SO16)	Full production	order this
74HC137DB	74HC137DB	9351 896 60112	Standard Marking * Bulk Pack	SOT338-1 (SSOP16)	Full production	order this
	74HC137DB-T	9351 896 60118	Standard Marking * Reel Pack, SMD, 13"	SOT338-1 (SSOP16)	Full production	order this
74HC137N	74HC137N	9337 570 60652	Standard Marking * Bulk Pack, CECC	SOT38-1 (DIP16)	Full production	order this
74HCT137D	74HCT137D	9337 570 90652	Standard Marking * Bulk Pack, CECC	SOT109-1 (SO16)	Full production	order this
	74HCT137D-T	9337 570 90653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT109-1 (SO16)	Full production	order this
74HCT137N	74HCT137N	9337 570 80652	Standard Marking * Bulk Pack, CECC	SOT38-1 (DIP16)	Full production	order this

Products in the above table are all in production. Some variants are discontinued; click here for information on these variants.

Similar products

74HC/HCT137 links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

Support & tools

HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications(date 01-Mar-98)
HC/T User Guide(date 01-Nov-97)

Email/translate this product information

- Email this product information.
- Translate this product information page from English to:

French Translate

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