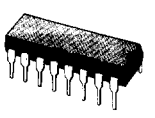
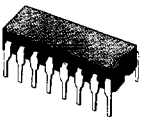
QUAD D-TYPE REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 73 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS 173



B1R
(Plastic Package)



F1R
(Ceramic Package)

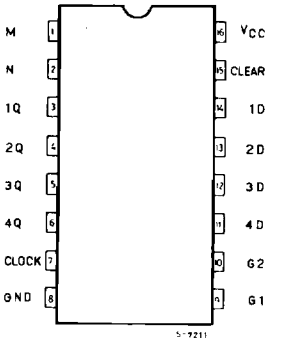
M1R
(Micro Package)

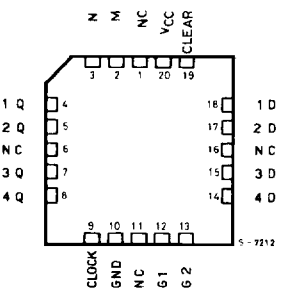
C1R
(Chip Carrier)

ORDER CODES :

M54HC173F1R M74HC173M1R
M74HC173B1R M74HC173C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC173 is a high speed CMOS QUAD D-TYPE REGISTER (3-STATE) fabricated in silicon gate C^2MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is composed of a four-bit register including D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common reset input (CLEAR). Signals applied to the data inputs (D_1-D_4) are stored at the respective flip-flops on the positive going transition of the clock input, only when both clock control inputs (G_1 and G_2) are held low.

The reset feature is asynchronous and active high. The stored data are provided on each output only when both output control inputs (M and N) are held low, otherwise the outputs go to the high-impedance state.

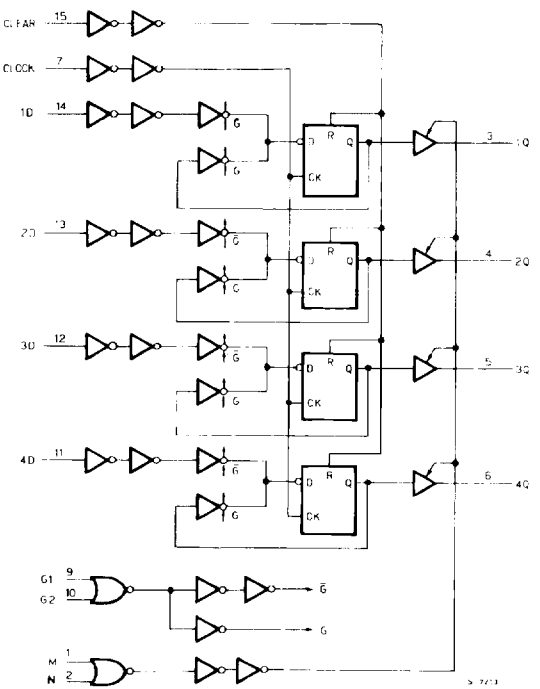
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

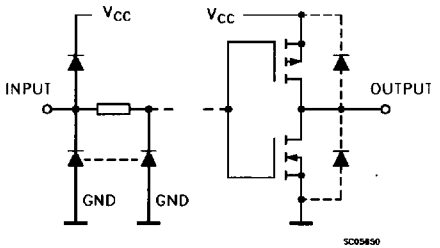
CLEAR	CLOCK	DATA ENABLE		Dn	OUTPUT CONTROL		Qn
		G1	G2		M	N	
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L	┐	X	X	X	L	L	Q0
L	┌	H	X	X	L	L	Q0
L	┌	X	H	X	L	L	Q0
L	┌	L	L	H	L	L	H
L	┌	L	L	L	L	L	L

X: Don't Care Z: High Impedance

LOGIC DIAGRAM



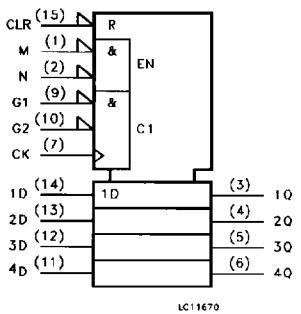
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2	M, N	Output Enable Input (Active LOW)
3, 4, 5, 6	1Q to 4Q	3-State Flip-flop Outputs
7	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
9, 10	G1, G2	Data Enable Inputs (Active LOW)
14, 13, 12, 11	1D to 4D	Data Inputs
15	CLEAR	Asynchronous Master Reset (Active HIGH)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

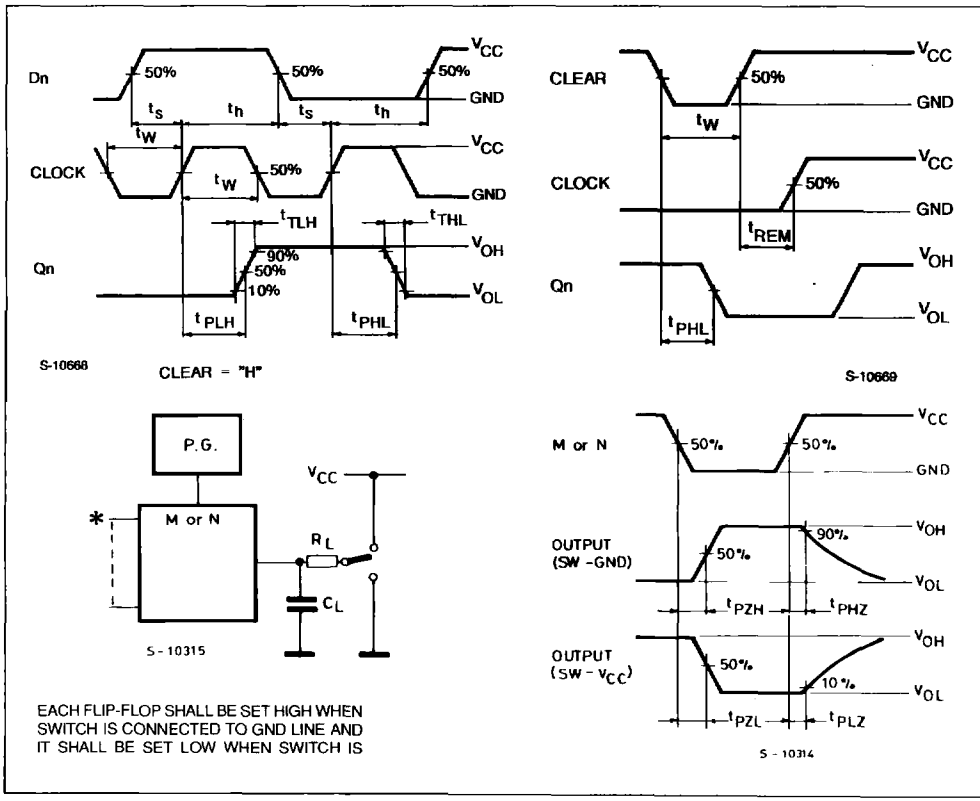
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0	50			50	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
		2.0	150			65	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q)	2.0	50			50	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
		2.0	150			65	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
f_{MAX}	Maximum Clock Frequency	2.0	50		8.6	20		6.8		5.8		MHz
		4.5			43	67		34		29		
		6.0			51	84		40		34		
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1KΩ		50	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
		2.0	150	R_L = 1KΩ		65	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1KΩ		36	105		130		160	ns
		4.5				15	21		26		32	
		6.0				13	18		22		27	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0	50			16	75		95		110	ns
		4.5				4	15		19		22	
		6.0				3	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0	50			16	75		95		110	ns
		4.5				4	15		19		22	
		6.0				3	13		16		19	
t_s	Minimum Set-up Time (G1, G2)	2.0	50			40	100		125		150	ns
		4.5				10	20		25		30	
		6.0				9	17		21		26	
t_s	Minimum Set-up Time (D)	2.0	50			24	75		95		110	ns
		4.5				6	15		19		22	
		6.0				5	13		16		19	
t_h	Minimum Hold Time (G1, G2, D)	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{REM}	Minimum Removal Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					50						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)