MOTOROLA

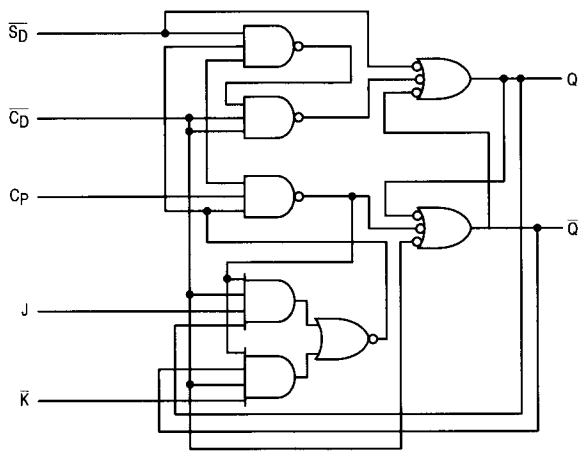
Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop

ELECTRICALLY TESTED PER:
MIL-M-38510/34102

The 54F109 consists of two high-speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of the rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:
LOW Input to $\overline{S_D}$ sets Q to HIGH level
LOW Input to $\overline{C_D}$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C_D}$ and $\overline{S_D}$ makes both Q and $\overline{Q}$ HIGH

LOGIC DIAGRAM
(one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Military 54F109

AVAILABLE AS:

1) JAN: JM38510/34102BXA
2) SMD: N/A
3) 883: 54F109/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{C_{D1}}$	1	1	2	GND
J1	2	2	3	V_{CC}
$\overline{K1}$	3	3	4	V_{CC}
CP1	4	4	5	V_{CC}
$\overline{S_{D1}}$	5	5	7	V_{CC}
Q1	6	6	8	OPEN
$\overline{Q1}$	7	7	9	OPEN
GND	8	8	10	GND
$\overline{Q2}$	9	9	12	OPEN
Q2	10	10	13	OPEN
$\overline{S_{D2}}$	11	11	14	V_{CC}
CP2	12	12	15	V_{CC}
$\overline{K2}$	13	13	17	V_{CC}
J2	14	14	18	V_{CC}
$\overline{C_{D3}}$	15	15	19	GND
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

4

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs				Outputs	
	$\overline{S_D}$	$\overline{C_D}$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H

*Both outputs will be HIGH while both $\overline{S_D}$ and $\overline{C_D}$ are LOW, but the output states are unpredictable if $\overline{S_D}$ and $\overline{C_D}$ go HIGH simultaneously.

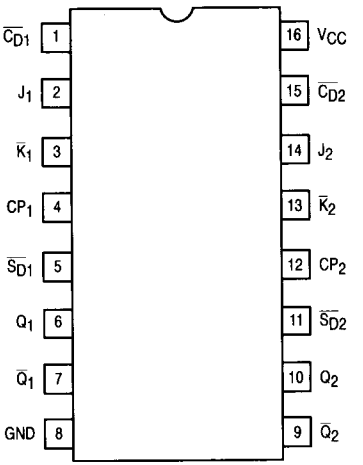
H, h = HIGH Voltage Level

L, l = LOW Voltage Level

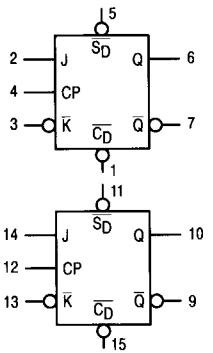
X = Don't Care

l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

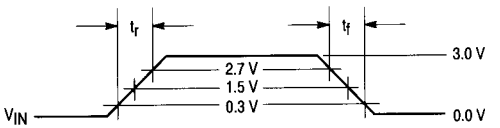
CONNECTION DIAGRAM



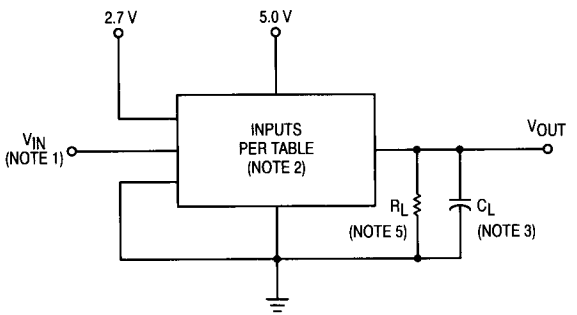
LOGIC SYMBOLS



WAVEFORM



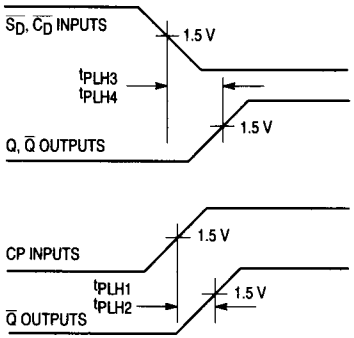
AC TEST CIRCUIT

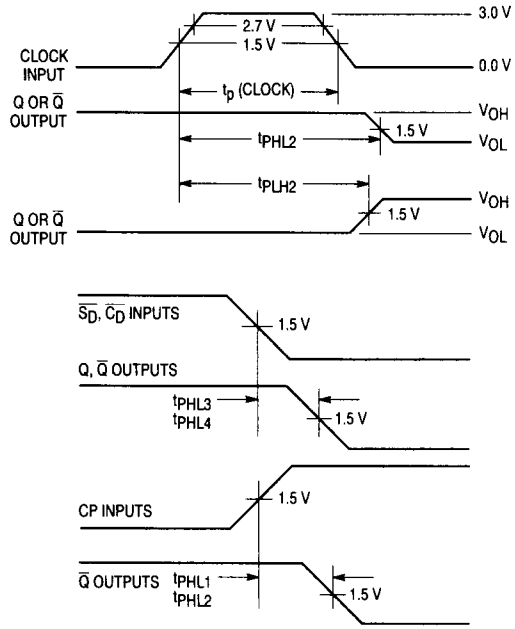


NOTES:

1. V_{IN} = Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, or as specified in table, Duty cycle = 50 ± 15%, $t_D = 5.0$ ns (min).
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. R_L = 499 Ω ± 5.0%.
6. When testing f_{MAX}, the output frequency shall be 1/2 the input frequency.
7. Clock, Clear and Set inputs need to be in the proper configuration for specified output conditions.

WAVEFORMS


$\overline{S_D}$, $\overline{C_D}$ INPUTS
1.5 V
t_{PLH3}
t_{PLH4}
1.5 V
Q, $\overline{Q}$ OUTPUTS
1.5 V
CP INPUTS
t_{PLH1}
t_{PLH2}
1.5 V
$\overline{Q}$ OUTPUTS


3.0 V
2.7 V
1.5 V
CLOCK INPUT
0.0 V
t_p (CLOCK)
Q OR $\overline{Q}$ OUTPUT
V_{OH}
1.5 V
t_{PHL2}
V_{OL}
t_{PLH2}
V_{OH}
1.5 V
Q OR $\overline{Q}$ OUTPUT
V_{OL}
$\overline{S_D}$, $\overline{C_D}$ INPUTS
1.5 V
Q, $\overline{Q}$ OUTPUTS
t_{PHL3}
t_{PHL4}
1.5 V
CP INPUTS
1.5 V
$\overline{Q}$ OUTPUTS
t_{PHL1}
t_{PHL2}
1.5 V

4

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IN} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V, V_{IN} = 4.5 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = 0 V.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs = 0 V.
I_{IL}	Logical "0" Input Current-J, K, & $\overline{CP}$	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{ILL} = 0.5 V, CP = 0 V, other inputs are open.
I_{ILL}	Logical "0" Input Current-$\overline{CD}$ & $\overline{SD}$	−0.09	−1.8	−0.09	−1.8	−0.09	−1.8	mA	V_{CC} = 5.5 V, CD = 0.5 V, SD = 0 V, other inputs = 4.5 V.
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 4.5 V, SD = 5.5 V, CD = 0 V, other inputs are open, V_{OUT} = 2.5 V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} (SD) = 0 V, other inputs are open, V_{OUT} = 0 V.
I_{CC}	Power Supply Current		17		17		17	mA	V_{CC} = 5.5 V, V_{IN} (K, CP, SD) = 0 V, other inputs are open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, **(Repeat at)**, V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output CP to Q	4.4	8.0	3.8	10.5	3.8	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω ±5.0%.
t_{PLH1}	Propagation Delay /Data-Output CP to Q	3.8	7.0	3.8	9.0	3.8	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω ±5.0%.
t_{PHL2}	Propagation Delay /Data-Output CP to $\overline{Q}$	4.4	8.0	3.8	10.5	3.8	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω ±5.0%.
t_{PLH2}	Propagation Delay /Data-Output CP to $\overline{Q}$	3.8	7.0	3.8	9.0	3.8	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω ±5.0%.
t_{PHL3}	Propagation Delay /Data-Output $\overline{CD}$ or $\overline{SD}$ to Q or $\overline{Q}$	3.5	9.0	3.2	11.5	3.2	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω ±5.0%.
t_{PLH3}	Propagation Delay /Data-Output $\overline{CD}$ or $\overline{SD}$ to Q or $\overline{Q}$	3.2	7.0	3.2	9.0	3.2	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω ±5.0%.
t_{PHL4}	Propagation Delay /Data-Output $\overline{CD}$ or $\overline{SD}$ to Q or $\overline{Q}$	3.5	9.0	3.5	11.5	3.5	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω ±5.0%.
t_{PLH4}	Propagation Delay /Data-Output $\overline{CD}$ or $\overline{SD}$ to Q or $\overline{Q}$	3.2	9.0	3.2	9.0	3.2	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω ±5.0%.
f_{MAX}	Maximum Clock Frequency	90		70		70		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω ±5.0%.
t_s (H) t_s (L)	Set Up Time J, K, or D High or Low to CP	3.0		3.0		3.0		ns	V_{CC} = 5.0 V, C_L = 50 pF, (Information only, No Testing Required).
t_h (H) t_h (L)	Hold Time J, K, or D High or Low to CP	1.0		1.0		1.0		ns	V_{CC} = 5.0 V, C_L = 50 pF, (Information only, No Testing Required).
t_{rec}	Recovery Time SD, CD, to CP	2.0		2.0		2.0		ns	V_{CC} = 5.0 V, C_L = 50 pF, (Information only, No Testing Required).