



FAST CMOS 18-BIT REGISTERED TRANSCEIVER

IDT54/74FCT162501AT/CT

FEATURES:

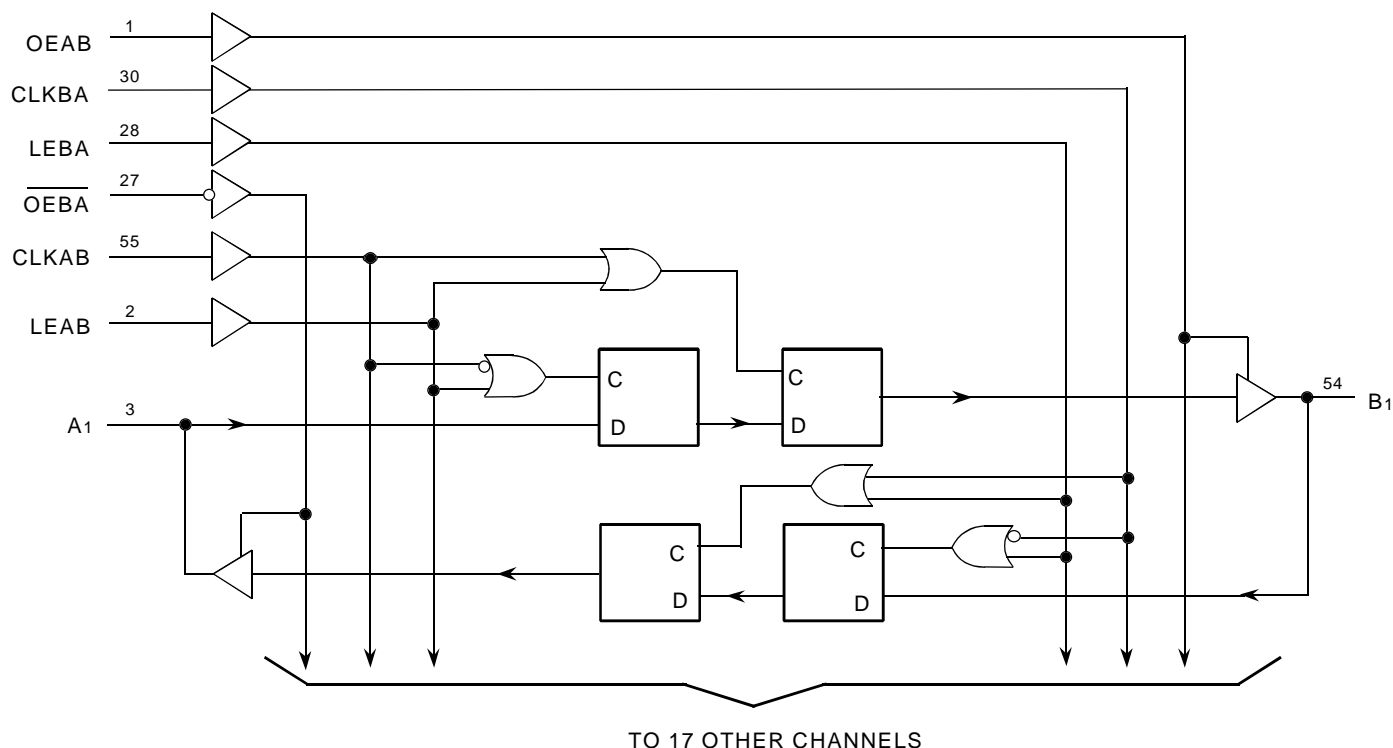
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu A$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Balanced Output Drivers:
 - $\pm 24mA$ (industrial)
 - $\pm 16mA$ (military)
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) < 0.6V at $V_{CC} = 5V$, $T_A = 25^\circ C$
- Available in the following packages:
 - Industrial: SSOP, TSSOP, TVSOP
 - Military: CERPACK

DESCRIPTION:

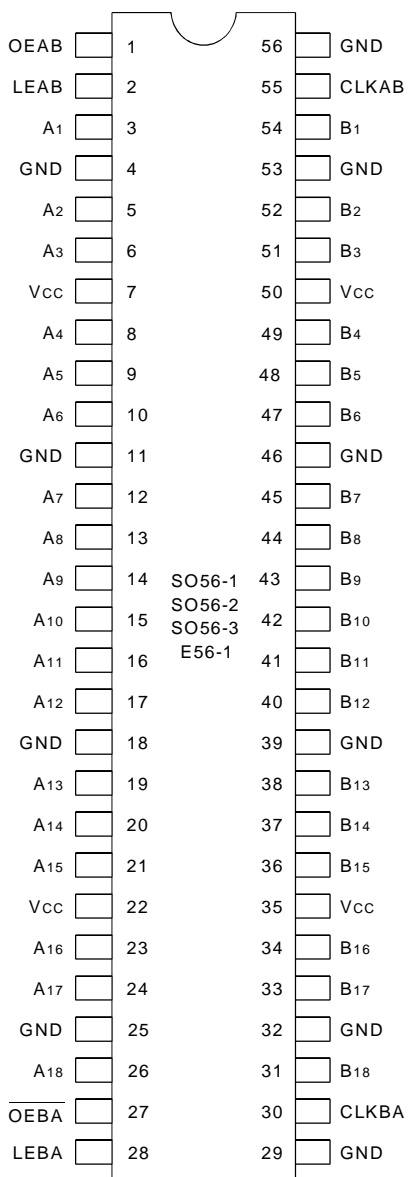
The FCT162501T 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. OEAB is the output enable for the B port. Data flow from the B port to the A port is similar but requires using \overline{OEBA} , LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162501T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162501T is a plug-in replacement for the FCT16501T and ABT16501 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP/ CERPACK
TOP VIEW

PIN DESCRIPTION

| Pin Names | Description |
|--------------------------|--|
| OEAB | A-to-B Output Enable Input |
| $\overline{\text{OEBA}}$ | B-to-A Output Enable Input (Active LOW) |
| LEAB | A-to-B Latch Enable Input |
| LEBA | B-to-A Latch Enable Input |
| CLKAB | A-to-B Clock Input |
| CLKBA | B-to-A Clock Input |
| A _x | A-to-B Data Inputs or B-to-A 3-State Outputs |
| B _x | B-to-A Data Inputs or A-to-B 3-State Outputs |

ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max | Unit |
|----------------------------------|--------------------------------------|------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7 | V |
| V _{TERM} ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to V _{CC} +0.5 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | -60 to +120 | mA |

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 3.5 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 3.5 | 8 | pF |

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NOTE:

- This parameter is measured at characterization but not tested.

FUNCTION TABLE^(1,4)

| Inputs | | | | Outputs |
|--------|------|-------|----------------|------------------|
| OEAB | LEAB | CLKAB | A _x | B _x |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↑ | L | L |
| H | L | ↑ | H | H |
| H | L | L | X | B ⁽²⁾ |
| H | L | H | X | B ⁽³⁾ |

NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|---|--|---------------------|------|---------------------|---------|---------------|
| V_{IH} | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| V_{IL} | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| I_{IH} | Input HIGH Current (Input pins) ⁽⁵⁾ | $V_{CC} = \text{Max.}$ | $V_I = V_{CC}$ | — | — | ± 1 | μA |
| | Input HIGH Current (I/O pins) ⁽⁵⁾ | | | — | — | ± 1 | |
| I_{IL} | Input LOW Current (Input pins) ⁽⁵⁾ | | $V_I = \text{GND}$ | — | — | ± 1 | |
| | Input LOW Current (I/O pins) ⁽⁵⁾ | | | — | — | ± 1 | |
| I_{OZH} | High Impedance Output Current (3-State Output pins) ⁽⁵⁾ | $V_{CC} = \text{Max.}$ | $V_O = 2.7\text{V}$ | — | — | ± 1 | μA |
| I_{OZL} | | | $V_O = 0.5\text{V}$ | — | — | ± 1 | |
| V_{IK} | Clamp Diode Voltage | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$ | | — | -0.7 | -1.2 | V |
| I_{OS} | Short Circuit Current | $V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$ | | -80 | -140 | -250 | mA |
| V_H | Input Hysteresis | — | | — | 100 | — | mV |
| I_{CCL} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}$ | | — | 5 | 500 | μA |
| I_{CCH} | | $V_{IN} = \text{GND or } V_{CC}$ | | | | | |
| I_{CCZ} | | | | | | | |

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OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|---------------------|---|---|------|---------------------|------|------|
| I_{ODL} | Output LOW Current | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$ | | 60 | 115 | 200 | mA |
| I_{ODH} | Output HIGH Current | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$ | | -60 | -115 | -200 | mA |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}$ | $I_{OH} = -16\text{mA MIL}$ $I_{OH} = -24\text{mA IND.}$ | 2.4 | 3.3 | — | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}$ | $I_{OL} = 16\text{mA MIL}$ | — | 0.3 | 0.55 | V |
| | | | $I_{OL} = 24\text{mA IND.}$ | | | | |

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.

POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------------|--|---|--|------|---------------------|---------------------|--------------------------|
| ΔI_{CC} | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$ | | — | 0.5 | 1.5 | mA |
| I_{CCD} | Dynamic Power Supply Current ⁽⁴⁾ | $V_{CC} = \text{Max.}, \text{Outputs Open}$ $OEAB = \overline{OEBA} = V_{CC} \text{ or GND}$ One Input Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 75 | 120 | $\mu\text{A}/\text{MHz}$ |
| I_C | Total Power Supply Current ⁽⁶⁾ | $V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz (CLKAB)}$ 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 0.8 | 1.7 | mA |
| | | | $V_{IN} = 3.4V$ $V_{IN} = \text{GND}$ | — | 1.3 | 3.2 | |
| | | $V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz (CLKAB)}$ 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ Eighteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 3.8 | 6.5 ⁽⁵⁾ | |
| | | | $V_{IN} = 3.4V$ $V_{IN} = \text{GND}$ | — | 8.5 | 20.8 ⁽⁵⁾ | |

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (ICCL, ICCH and ICCZ)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (VIN = 3.4V)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

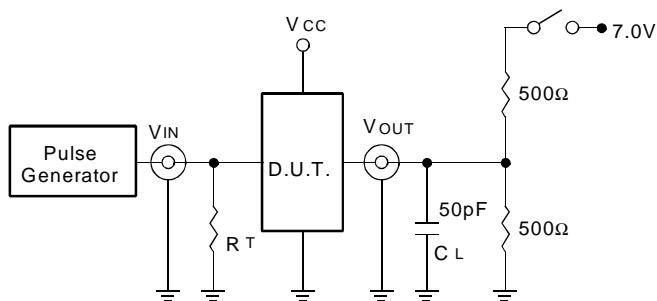
| Symbol | Parameter | Condition ⁽¹⁾ | 54/74FCT162501AT | | | | 54/74FCT162501CT | | | | Unit |
|--------------------------------------|---|--------------------------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|------|
| | | | Ind. | | Mil. | | Ind. | | Mil. | | |
| | | | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | |
| f _{MAX} | CLKAB or CLKBA frequency ⁽⁴⁾ | CL = 50pF | — | 150 | — | 150 | — | 150 | — | 150 | MHz |
| t _{PLH} t _{PHL} | Propagation Delay Ax to Bx or Bx to Ax | RL = 500Ω | 1.5 | 5.1 | 1.5 | 5.6 | 1.5 | 4.3 | 1.5 | 4.6 | ns |
| t _{PLH} t _{PHL} | Propagation Delay LEBA to Ax, LEAB to Bx | | 1.5 | 5.6 | 1.5 | 6 | 1.5 | 4.4 | 1.5 | 5.6 | ns |
| t _{PLH} t _{PHL} | Propagation Delay CLKBA to Ax, CLKAB to Bx | | 1.5 | 5.6 | 1.5 | 6 | 1.5 | 4.4 | 1.5 | 5.4 | ns |
| t _{PZH} t _{PZL} | Output Enable Time OEBA to Ax, OEAB to Bx | | 1.5 | 6 | 1.5 | 6.4 | 1.5 | 4.8 | 1.5 | 6 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time OEBA to Ax, OEAB to Bx | | 1.5 | 5.6 | 1.5 | 6 | 1.5 | 5.2 | 1.5 | 5.6 | ns |
| t _{SU} | Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA | | 3 | — | 3 | — | 2.4 | — | 3 | — | ns |
| t _H | Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA | | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{SU} | Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA | Clock LOW | 3 | — | 3 | — | 2 | — | 3 | — | ns |
| | | Clock HIGH | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _H | Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA | | 1.5 | — | 1.5 | — | 0.5 | — | 1.5 | — | ns |
| t _w | LEAB or LEBA Pulse Width HIGH ⁽⁴⁾ | | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| t _w | CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾ | | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| t _{SK(o)} | Output Skew ⁽³⁾ | | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

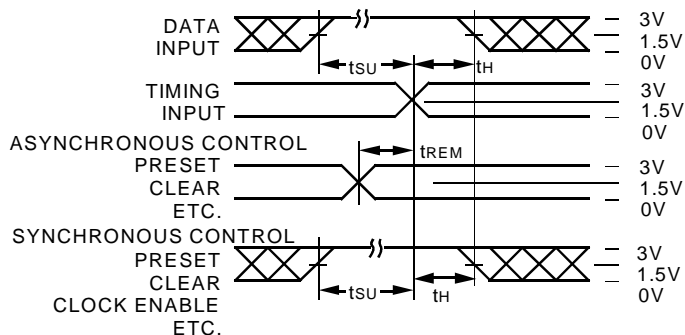
| Test | Switch |
|-----------------|--------|
| Open Drain | Closed |
| Disable Low | |
| Enable Low | |
| All Other Tests | Open |

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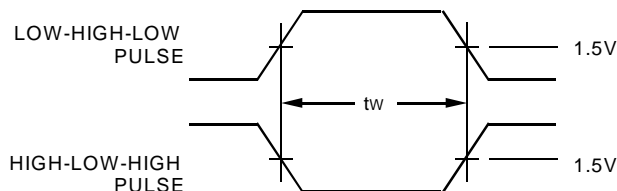
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

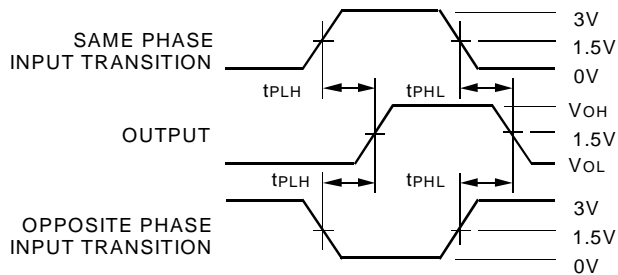
SET-UP, HOLD, AND RELEASE TIMES



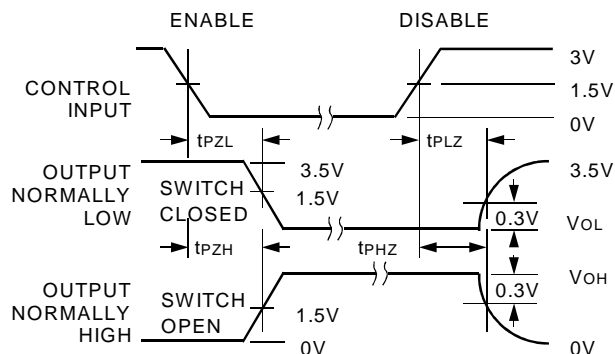
PULSE WIDTH



PROPAGATION DELAY



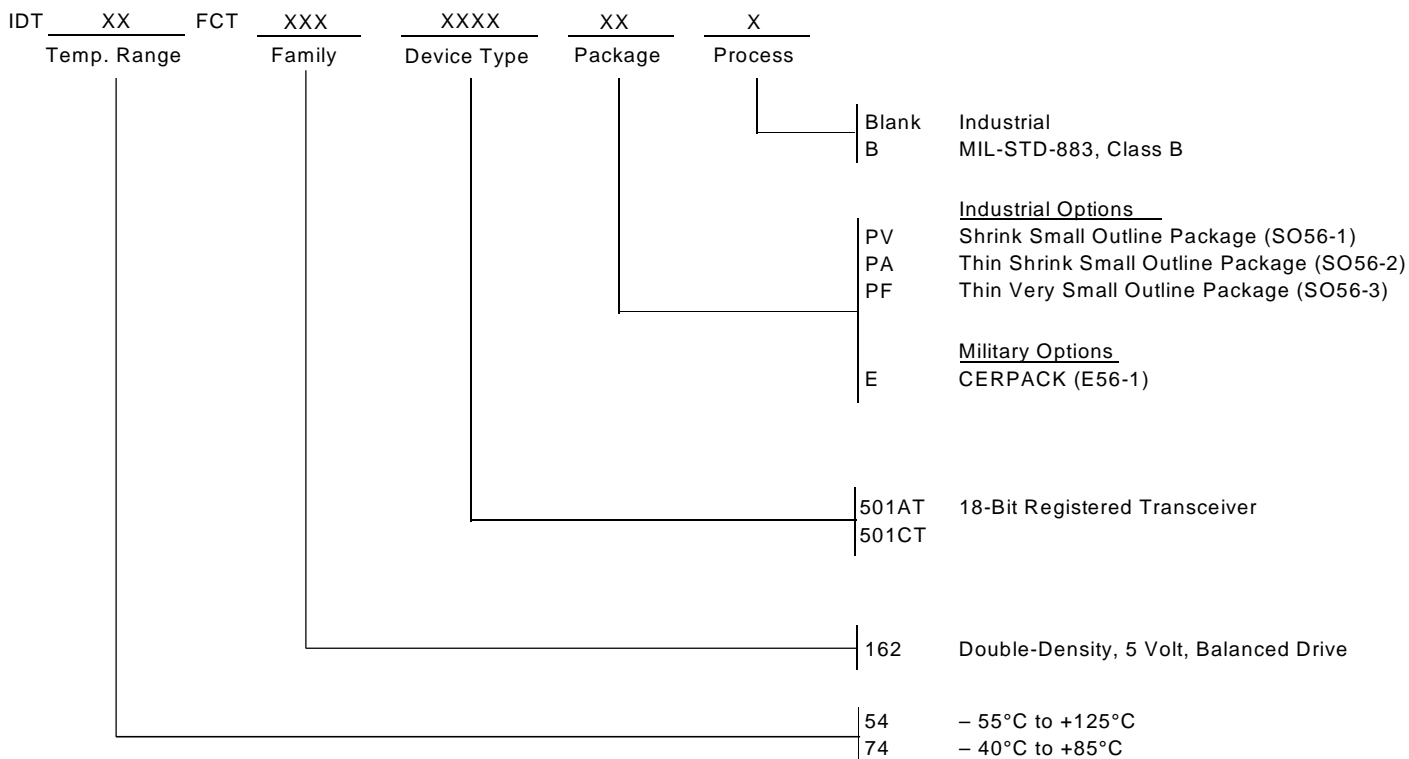
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION



NOTE:

New, tighter specs listed in the table below were changed effective with date code "0101" (parts shipped after January 1, 2001).

| Device | Parameter | Description | Condition | Old (ns) | New (ns) |
|---------------------|-------------------------------------|--------------------------------------|------------|----------|----------|
| 74FCT162501C | t _{PLH} , t _{PHL} | Prop Delay Ax to Bx, or Bx to Ax | 50pF/500 Ω | 4.6 | 4.3 |
| | t _{PLH} , t _{PHL} | Prop Delay LEBA to Ax, LEAB to Bx | 50pF/500 Ω | 5.3 | 4.4 |
| | t _{PLH} , t _{PHL} | Prop Delay CLKBA to Ax, CLKAB to Bx | 50pF/500 Ω | 5.3 | 4.4 |
| | t _{PZH} , t _{PZL} | Output Enable OEBA to Ax, OEAB to Bx | 50pF/500 Ω | 5.6 | 4.8 |



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