QUALITY SEMICONDUCTOR, INC.

Low Skew CMOS PLL Clock Driver With Integrated Loop Filter

QS5931

ADVANCE INFORMATION

FEATURES/BENEFITS

- Six low noise CMOS level outputs
- Q outputs, Q/2 output
- < 500ps output skew, Q0-Q4
- Outputs 3-state and reset while OE/$\overline{RST}$ low
- PLL disable feature for low frequency testing
- Internal loop filter RC network
- Internal VCO/2 option
- Balanced drive outputs ± 36mA
- 80MHz maximum frequency
- Industrial temperature range
- Available in space saving QSOP package

DESCRIPTION

The QS5931 Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to a reference clock input. Six outputs are available: Q0-Q4, Q/2. Careful layout and design ensure < 500ps skew between the Q0-Q4, and Q/2 outputs. The QS5931 includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. Various combinations of feedback and a divide-by-2 in the VCO path allow applications to be customized for linear VCO operation over a wide range of input SYNC frequencies. The PLL can also be disabled by the PLL_EN signal to allow low frequency or DC testing. The QS5931 is designed for use in cost sensitive high-performance computing systems, workstations, multi-board computers, networking hardware, and mainframe systems. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. In the QSOP package, the QS5931 clock driver represents the best value in small form factor, high-performance clock management products.

For more information on PLL clock driver products, see Application Note AN-22A.

Figure 1. Functional Block Diagram

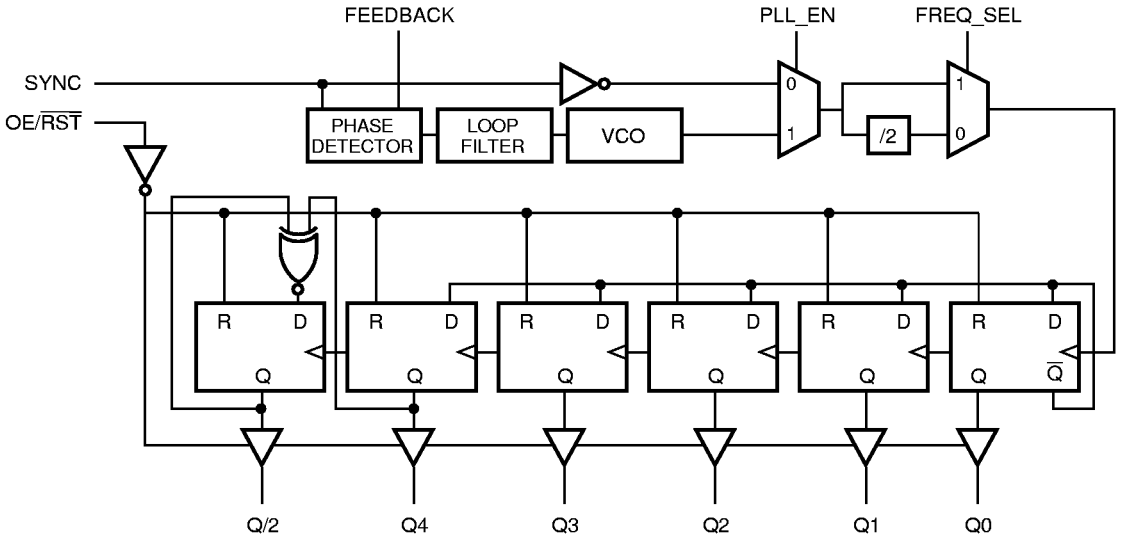
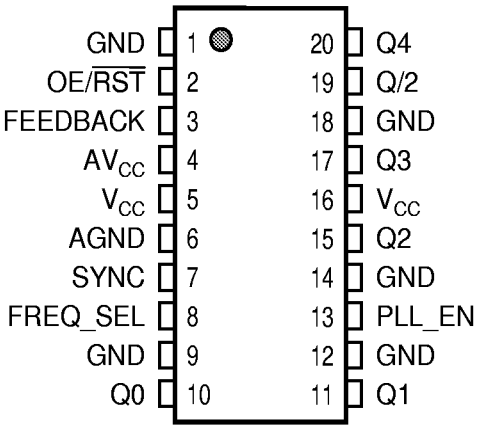


Figure 2. Pin Configuration (All Pins Top View)

QSOP



3

Table 1. Pin Description

Pin Name	I/O	Functional Description
SYNC	I	Reference clock input
FREQ_SEL	I	VCO frequency select. For choosing optimal VCO operating frequency depending on input frequency. HIGH is for higher frequencies, LOW is for lower frequencies.
FEEDBACK	I	PLL feedback input which is connected to either a Q or a Q/2 output. External feedback provides flexibility for different output frequency relationships. See the Frequency Selection Table for more information.
Q0-Q4	O	Clock outputs
Q/2	O	Clock output. Matched in phase, but frequency is half the Q frequency.
OE/$\overline{RST}$	I	Output enable/asynchronous reset. Resets all output registers. When 0, all outputs are held in a tri-stated condition. When 1, outputs are enabled.
PLL_EN	I	PLL enable. Enables and disables the PLL. Allows the SYNC input to be single-stepped for system debug.
V_{CC}	—	Power supply for output buffers.
AV_{CC}	—	Power supply for phase lock loop and other internal circuitries.
GND	—	Ground supply for output buffers.
AGND	—	Ground supply for phase lock loop and other internal circuitries.

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to V_{CC} +0.5V
Maximum Power Dissipation At T_A = 85°C	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Output Frequency Specifications

Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%

Symbol	Description	–50	–66	–80	Units
F_{MAX_Q}	Max Frequency, Q0-Q4	50	66	80	MHz
$F_{MAX\_Q/2}$	Max Frequency, Q/2	25	33	40	MHz
F_{MIN_Q}	Min Frequency, Q0-Q4	10	10	10	MHz
$F_{MIN\_Q/2}$	Min Frequency, Q/2	5	5	5	MHz

Table 4. Frequency Selection Table

FREQ_SEL	Output Used for Feedback	Allowable SYNC(1) Range (MHz) Min	Max	Output Frequency Relationships Q/2	Q0-Q4
HIGH	Q/2	$F_{MIN\_Q/2}$	$F_{MAX\_Q/2}$	SYNC	SYNC x 2
HIGH	Q0-Q4	F_{MIN_Q}	F_{MAX_Q}	SYNC/2	SYNC
LOW	Q/2	$F_{MIN\_Q/2}/2$	$F_{MAX\_Q/2}/2$	SYNC	SYNC x 2
LOW	Q0-Q4	$F_{MIN\_Q}/2$	$F_{MAX\_Q}/2$	SYNC/2	SYNC

Note:

1. Operation in the specified SYNC frequency range guarantees that the VCO will operate in its optimal range of 20MHz to F_{MAX_Q} x 2. Operation with Sync inputs outside specified frequency ranges may result in out-of-lock outputs. FREQ_SEL only affects VCO frequency and does not affect output frequencies.

Table 5. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

Pins	QSOP Typ	Max	Unit
C_{IN}	3	4	pF
C_{OUT}	4	5	pF

Note: Capacitance is characterized but not tested.

Table 6. DC Electrical Characteristics Over Operating Range

Industrial T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –36mA I_{OH} = –100µA	V_{CC} –0.75 V_{CC} –0.20			V V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 36mA V_{CC} = Min., I_{OL} = 100µA			0.45 0.2	V V
V_H	Input Hysteresis			100		mV
$\|I_{OZ}\|$	Output Leakage Current	V_{OUT} = V_{CC} or V_{OUT} = GND, V_{CC} = Max., Outputs disabled			5	µA
$\|I_{IN}\|$	Input Leakage Current	V_{CC} = Max.,V_{IN} = V_{CC} or V_{IN} = GND			5	µA

3

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., OE/$\overline{RST}$ = Low, SYNC = Low, All outputs unloaded		1	mA
ΔI_{CC}	Power Supply Current per Input HIGH	V_{CC} = Max., V_{IN} = 3.4V	0.7	1.5	mA
I_{CCD}	Dynamic Power Supply Current[1]	V_{CC} = Max., C_L = 0pF	—	0.1	mA/ MHz

Note:

1. Guaranteed by characterization but not tested.

Table 8. Switching Characteristics Over Operating Range

Industrial T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%

Symbol	Description[1]	Min	Max	Unit
t_{SKR}	Output Skew Between Rising Edges, Q0-Q4 and Q/2[2,3]	—	500	ps
t_{SKF}	Output Skew Between Falling Edges, Q0-Q4 and Q/2[2,3]	—	500	ps
t_{PW}	Pulse Width, Q0-Q4, Q/2 outputs, 80MHz[2]	T_{CY}/2 –0.4	T_{CY}/2+0.4	ns
t_J	Cycle to Cycle Jitter[2,5]	—	± 0.15	ns
t_{PD}	SYNC Input to Feedback Delay[2,6]	–500	+500	ps
t_{LOCK}	SYNC to Phase Lock	—	10	ms
t_{PZH} t_{PZL}	Output Enable Time, OE/$\overline{RST}$ LOW to HIGH[4]	0	14	ns
t_{PHZ} t_{PLZ}	Output Disable Time, OE/$\overline{RST}$ HIGH to LOW[2,4]	0	14	ns
t_R, t_F	Output Rise/Fall Times,0.2V_{CC}~0.8V_{CC}[2]	0.3	2.5	ns

Notes:

1. See Figure 3 for test load and termination. Test circuit 1 is used for output enable/disable parameters. Test circuit 2 is used for all other timing parameters.
2. This parameter is guaranteed by characterization but not tested.
3. Skew specifications apply under identical environments (loading, temperature, V_{CC}, device speed grade).
4. Measured in open loop mode PLL_EN = 0.
5. Jitter is characterized using an oscilloscope, Q output at 20MHz. Measurement is taken one cycle after jitter. See FREQUENCY SELECTION TABLE for information on proper FREQ_SEL level for specified input frequencies.
6. t_{PD} measured at device inputs at 1.5V, Q output at 80MHz.

Table 9. Input Timing Requirements

Industrial T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%

Symbol	Description	Min	Max	Unit
t_R, t_F	Maximum Input Rise and Fall Times, 0.8V to 2.0V	—	3.0	ns
F_I	Input Clock Frequency, SYNC[1]	2.5	F_{MAX_Q}	MHz
t_{PWC}	Input Clock Pulse, HIGH or LOW[2]	2	—	ns
D_H	Duty Cycle, SYNC[2]	25	75	%

Notes:

1. See Table 3 and Table 4 for more detail on allowable SYNC input frequencies for different speed grades with different FEEDBACK and FREQ_SEL combinations.
2. Input timing requirements are guaranteed by design but not tested. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

Figure 3. Test Loads and Waveforms

Test circuit 1 is used for output enable/disable parameters.
Test circuit 2 is used for all other timing parameters.

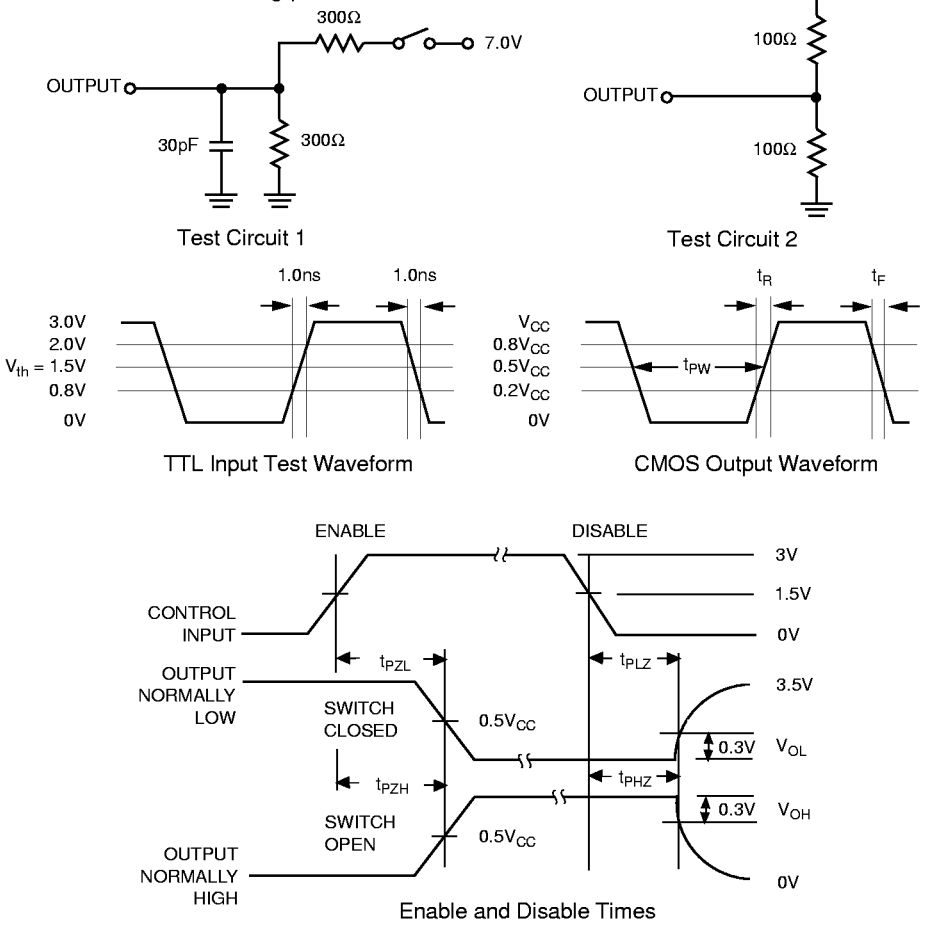
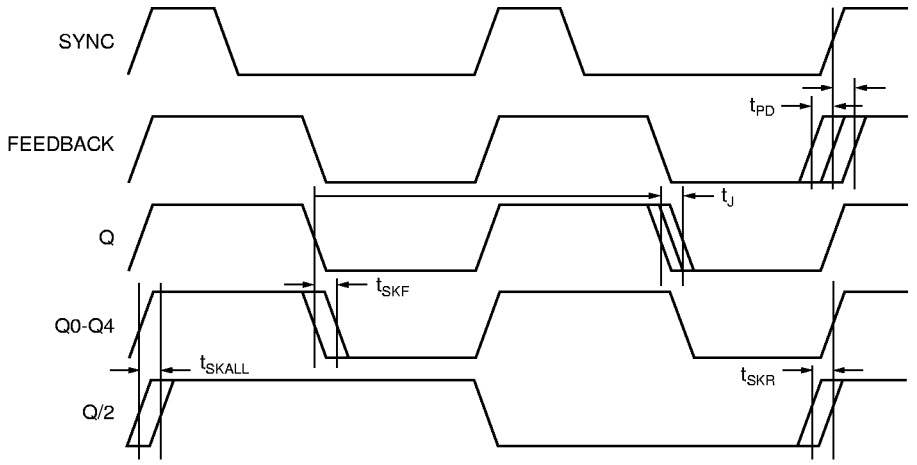


Figure 4. AC Timing Diagram



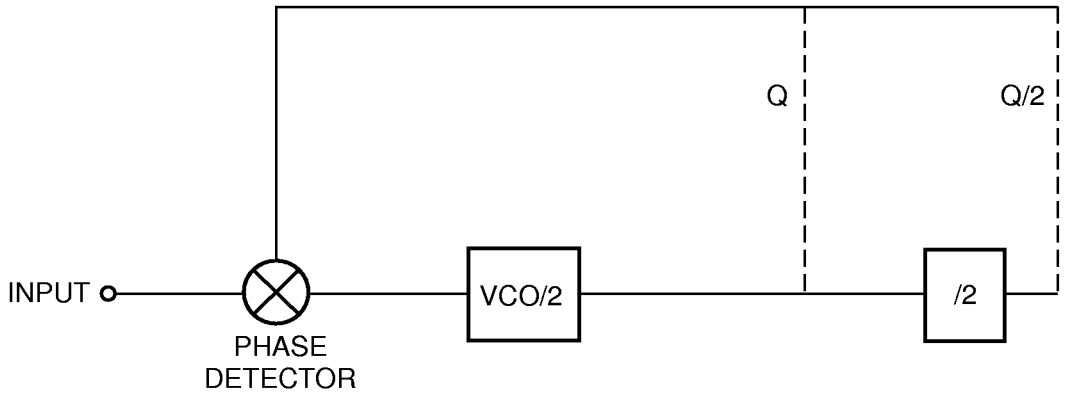
Notes:

1. Figure 4 applies to Q output connected to FEEDBACK and $\overline{PE}$ = GND. For $\overline{PE}$ = V_{CC}, the negative edge of FEEDBACK aligns with the negative edge of SYNC input, and the negative edges of the multiplied and divided outputs align with the negatve edge of SYNC.
2. All parameters are measured at $0.5V_{CC}$.

PLL OPERATION

The Phase Locked Loop (PLL) circuit included in the QS5931 provides for replication of incoming SYNC clock signals. Any manipulation of that signal, such as frequency multiplying or inversion is performed by digital logic following the PLL (see the block diagram). The key advantage of the PLL circuit is to provide an effective zero propagation delay between the output and input signals. In fact, adding delay circuits in the feedback path, 'propagation delay' can even be negative! Figure 5 shows a simplified schematic of the QS5931 PLL circuit:

Figure 5. Simplified Diagram of QS5931 Feedback



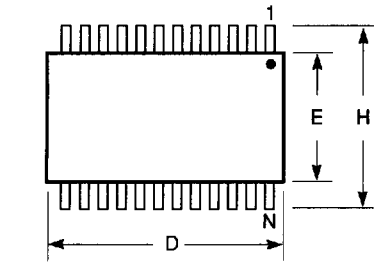
The phase difference between the output and the input frequencies feeds the VCO which drives the outputs. Whichever output is fed back, it will stabilize at the same frequency as the input. Hence, this is a true negative feedback closed loop system. In most applications, the output will optimally have zero phase shift with respect to the input. In fact, the internal loop filter on the QS5931 typically provides within 150ps of phase shift between input and output.

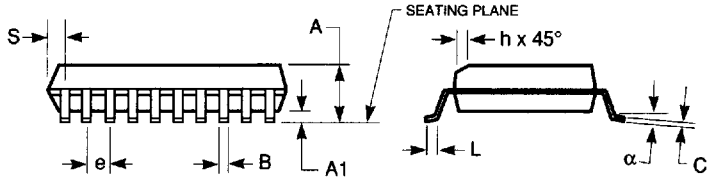
If the user wishes to vary the phase difference (typically to compensate for backplane delays), this is most easily accomplished by adding delay circuits to the feedback path. The respective output used for feedback will be advanced by the amount of delay in the feedback path. All other outputs will retain their proper relationships to that output.

150-MIL QSOP - Package Code Q

Quarter-Size Outline Package
Plastic Small Outline Gull-Wing

Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.





JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035