SN74LV4T125 Single Power Supply Quadruple Buffer Translator GATE w/3-State Output CMOS Logic Level Shifter

1 Features

- Single-Supply Voltage Translator
- Operating Range of 1.8V to 5.5V
- Up Translation Mode
  - 1.2V(1) to 1.8V at 1.8V Vcc
  - 1.5V(1) to 2.5V at 2.5V Vcc
  - 1.8V(1) to 3.3V at 3.3V Vcc
  - 3.3V to 5.0V at 5.0V Vcc
- Down Translation Mode
  - 3.3V to 1.8V at 1.8V Vcc
  - 3.3V to 2.5V at 2.5V Vcc
  - 5.0V to 3.3V at 3.3V Vcc
- Logic Output is Referring to Supply Vcc
- Unique Direction Translation-Up
- Characterized up to 50MHz at 3.3V Vcc
- TTL Compliance on Input Terminals
- Inputs are 5.5V Tolerant at Any Valid Vcc
- –40°C to 125°C Operating Temperature Range
- Pb-Free Packages Available: SC-70 (RGY)
  - 3.5 X 3.5 X 1 mm
- Latch-Up Performance Exceeds 250mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Enable the Standard Gate Function and Drop-in Replacement
- Backward Output Compatible with AUP1G, LVC1G

(1) Refer the VIH/VIL and output drive for lower Vcc condition

2 Applications

- Tablet
- Smartphone
- Personal Computer
- Industrial Automotive

3 Description

SN74LV4T125 is a Low Voltage CMOS buffer gate and operates in a wide voltage range for portable and battery back-up equipment.

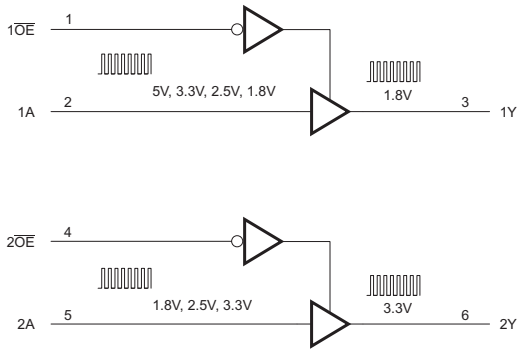
The input is designed with a lower threshold circuit to match 1.8V Input Logic at Vcc = 3.3V and can be used in 1.8V to 3.3V Level Up Translator functions. In addition, the 5V Input tolerant on input terminals enable the chip to configure Down Translation as 3.3V to 2.5V output at Vcc = 2.5V. The wide VCC range of 1.8 V to 5.5 V allows the possibility of desired switching output level to connect the controllers or processors.

The SN74LV4T125 is designed with optimized current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SN74LV4T125PW	TSSOP (14)	5mm x 4.4mm
SN74LV4T125RGY	VQFN (14)	3,5mm x 3,5mm

4 Simplified Application Diagram



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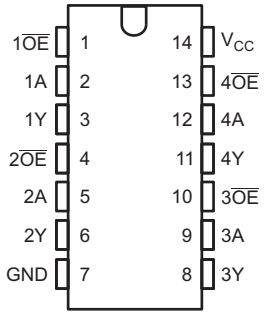
5 Revision History

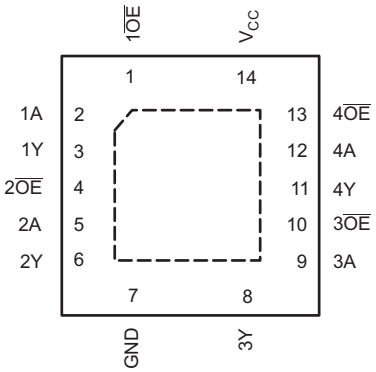
Changes from Original (February 2014) to Revision A	Page
• Updated 1 page preview document to full version.	1

6 Terminal Configuration and Functions

PW Package
(TOP VIEW)



RGY Package
(Transparent TOP VIEW)



Terminal Functions

TERMINAL		DESCRIPTION
NO.	I/O	
1	1OE	ENABLE 1
2	1A	INPUT 1
3	1Y	OUTPUT 1
4	2OE	ENABLE 2
5	2A	INPUT 2
6	2Y	OUTPUT 2
7	GND	GROUND
8	3Y	OUTPUT 3
9	3A	INPUT 3
10	3OE	ENABLE 3
11	4Y	OUTPUT 4
12	4A	INPUT 4
13	4OA	ENABLE 4
14	VCC	POWER

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7.0	V
V_I	Input voltage range (2)		–0.5	7.0	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
	Voltage range applied to any output in the high or low state(2)		–0.5	V_{CC} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > Vcc		±50	mA
I_O	Continuous output current			±35	mA
	Continuous current through V_{CC} or GND			±70	mA
θ_{JA}	Package thermal impedance (3)	PW package		113	°C/W
		RGY package		47	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C
V_{ESD}(1)	Human Body Model (HBM) ESD stress voltage(2)		2	kV
	Charged Device Model (CDM) ESD stress voltage(3)		1000	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.6	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or Low State	0	Vcc	V
		H-Z	0	Vcc	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		-3	mA
		V_{CC} = 2.5 V		-5	mA
		V_{CC} = 3.3 V		-8	
		V_{CC} = 5.0 V		-16	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		3	
		V_{CC} = 2.5 V		5	
		V_{CC} = 3.3 V		8	
		V_{CC} = 5.0 V		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.6V to 2.0V		20	ns/V
		V_{CC} = 2.3V to 2.7V		20	
		V_{CC} = 3 V or 3.6V		20	
		V_{CC} = 4.5 to 5.0 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7.4 Thermal Information

THERMAL METRIC(1)		SN74LV4T125		UNIT
		PW PACKAGE	RGY PACKAGE	
		14 TERMINALS	14 TERMINALS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.9	52.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	54.2	67.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	68.6	29.0	
ψ_{JT}	Junction-to-top characterization parameter	7.5	2.6	
ψ_{JB}	Junction-to-board characterization parameter	68.0	29.1	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	n/a	9.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{IH}	High-level input voltage		V_{CC} = 1.65 V to 1.9 V	0.95			1		V
			V_{CC} = 2.3 V to 2.7 V	1.1			1.2		
			V_{CC} = 3 V to 3.6 V	1.3			1.35		
			VCC = 4.5 V to 5.0 V	2			2		
V_{IL}	Low-level input voltage		V_{CC} = 1.65 V to 1.9 V			0.55		0.5	V
			V_{CC} = 2.3 V to 2.77 V			0.7		0.6	
			V_{CC} = 3 V to 3.6 V			0.85		0.75	
			V_{CC} = 4.5 V to 5.5 V			0.9		0.85	
V_{OH}		I_{OH} = –50 µA	V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –2 mA	V_{CC} = 1.65 V	1.4			1.35		V
		I_{OH} = –3 mA	V_{CC} = 2.3V	2.05			2.0		V
		I_{OH} = –5 mA	V_{CC} = 3.0 V	2.7			2.6		V
		I_{OH} = –8 mA		2.6			2.5		
		I_{OH} = –8 mA	V_{CC} = 4.5 V	3.7			3.6		V
		I_{OH} = –16 mA		3.8			3.7		
		I_{OH} = –16 mA	V_{CC} = 5.0 V	4.4			4.3		V
V_{OL}		I_{OL} = 50 µA	V_{CC} = 1.65 V to 5.5 V			0.1		0.1	V
		I_{OH} = 2 mA	V_{CC} = 1.65 V			0.1		0.1	V
			V_{CC} = 1.8V			0.2		0.3	
		I_{OH} = 3 mA	V_{CC} = 2.3V			0.2		0.3	V
			V_{CC} = 2.5V			0.25		0.3	
		I_{OH} = 5 mA	V_{CC} = 3.0 V			0.35		0.4	V
		I_{OH} = 8 mA				0.4		0.45	
		I_{OH} = 8mA	V_{CC} = 3.3 V			0.45		0.5	V
		I_{OH} = 8 mA	V_{CC} = 4.5 V			0.50		0.55	V
		I_{OH} = 16 mA				0.55		0.55	
		I_{OH} = 16 mA	V_{CC} = 5.0 V			0.55		0.55	V
I_I	A input	V_I =0V or V_{CC}	V_{CC} = 0V, 1.8V, 2.5V, 3.3V, 5.5 V			±0.1		±1	µA
I_{CC}		V_I = 0V or V_{CC}, I_O = 0; open on loading	V_{CC} = 5.0 V			2		20	µA
			V_{CC} = 3.3 V			2		20	
			V_{CC} = 2.5 V			2		20	
			V_{CC} = 1.8V			2		20	
ΔI_{CC}		One input at 0.3V or 3.4V Other inputs at 0 or Vcc, I_O = 0	V_{CC} = 5.5 V			1.35		1.5	µA
		One input at 0.3V or 1.1V Other inputs at 0 or Vcc, I_O = 0	V_{CC} = 1.8V						
I_{OZ}		V_O = Vcc or GND	V_{CC} = 5.5V			±0.25		±2.5	µA
I_{off}		V_O or V_I = 0 to 5.5V	V_{CC} = 0V			0.5		5	µA
C_i		V_I = V_{CC} or GND	V_{CC} = 3.3 V		1.6		1.6		pF
C_o		V_O = Vcc or GND	V_{CC} = 3.3 V		4.8		4.8		pF

7.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see **Figure 2**)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FREQUENCY (TYP)	V_{CC}	C_L	T_A = 25°C			T_A = –65°C to 125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Any In	Y	DC to 50MHz	5.0V	15pF		2.8	3.2		3	3.5	ns
					30pF		3	3.5		3	4.5	
				3.3V	15pF		4	4.5		5	5.5	
					30pF		5	5.5		5.5	6.5	
			DC to 50MHz	2.5V	15pF		5.5	6.5		7	7.5	ns
					30pF		6.5	7		7.5	8.5	
			DC to 30MHz	1.8V	15pF		10	11		11	12	ns
					30pF		11	12		12.5	13	
t_{PZH}	OE	Y	DC to 50MHz	5.0V	15pF		3.5	4		3.5	4	ns
					30pF		3.8	4.2		4	4.5	
				3.3V	15pF		5	5.8		5.8	6.1	
					30pF		5.5	6		5.7	6.5	
			DC to 50MHz	2.5V	15pF		7.5	8		8.5	9	ns
					30pF		8	8.5		9	9.5	
			DC to 30MHz	1.8V	15pF		14.5	15		15.5	16.5	ns
					30pF		15.5	16		16	17	
t_{PZL}	OE	Y	DC to 50MHz	5.0V	15pF		3	3.5		3.5	4	ns
					30pF		3.5	4		4	4.5	
				3.3V	15pF		5.3	5.6		6	6.2	
					30pF		5.8	6.2		7	7.5	
			DC to 50MHz	2.5V	15pF		8	8.5		9	9.5	ns
					30pF		9	9.5		10.5	11	
			DC to 30MHz	1.8V	15pF		17	17.5		18	18.5	ns
					30pF		18	18.5		19	20	
t_{PHZ}	OE	Y	DC to 50MHz	5.0V	15pF		3	3.5		3.5	4	ns
					30pF		3.5	4		4	4.5	
				3.3V	15pF		3.5	4		4.5	5	
					30pF		5	6		6.5	7	
			DC to 50MHz	2.5V	15pF		5.5	6		6	6.5	ns
					30pF		7.5	8		8	9	
			DC to 30MHz	1.8V	15pF		7.5	8		8	8.5	ns
					30pF		11	12		12	13	
t_{PLZ}	OE	Y	DC to 50MHz	5.0V	15pF		2	2.5		2	2.7	ns
					30pF		2	3		2	3.2	
				3.3V	15pF		2.3	2.8		2.5	3.2	
					30pF		2.8	3.2		3.3	4	
			DC to 50MHz	2.5V	15pF		3.3	3.8		3.8	4.2	ns
					30pF		4	4.3		4.2	5	
			DC to 30MHz	1.8V	15pF		5	5.5		5	5.7	ns
					30pF		6.5	7		7	8.5	
t_{sk}	Any In	Y	DC to 50MHz	5.0V to 2.5V	15pF					1		1	ns
			DC to 30MHz	1.8V	15pF							

7.7 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

7.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50pF, f = 10MHz	16	pF

7.9 Typical Characteristics

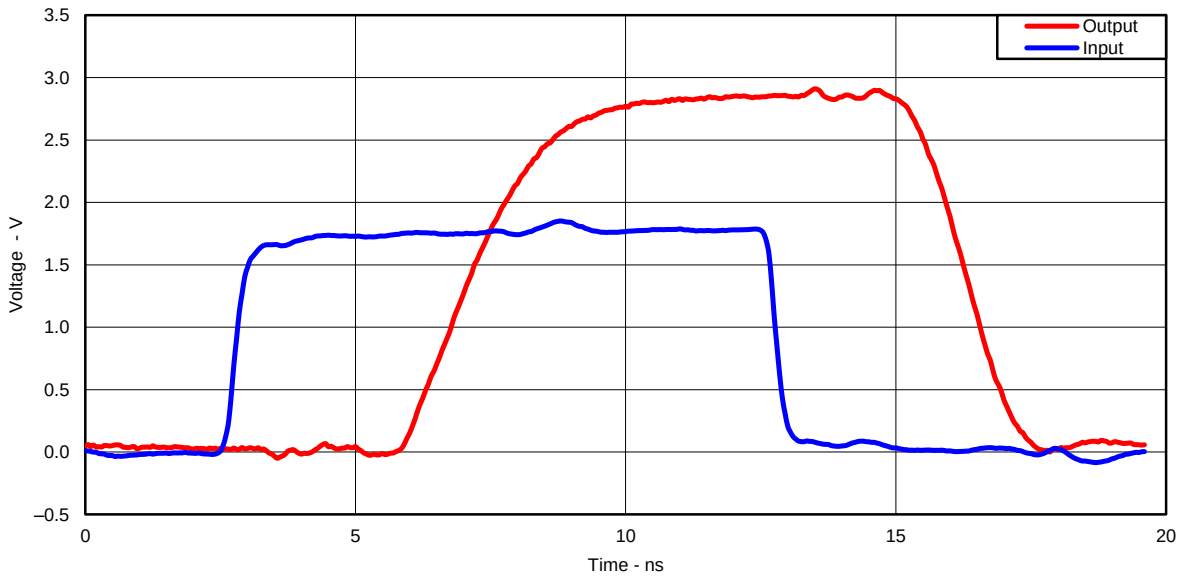
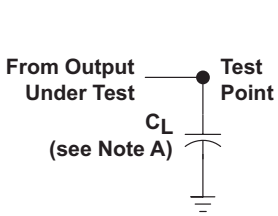
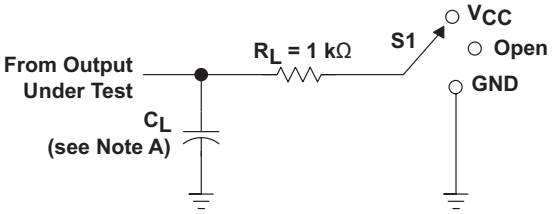


Figure 1. Switching Characteristics at 50 MHz
Excellent Signal Integrity (1.8V to 3.3V at 3.3V V_{CC})

8 Parameter Measurement Information

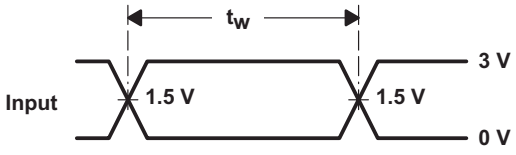


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

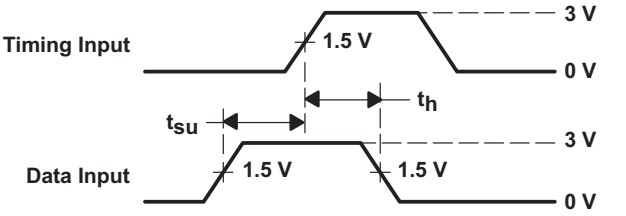


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

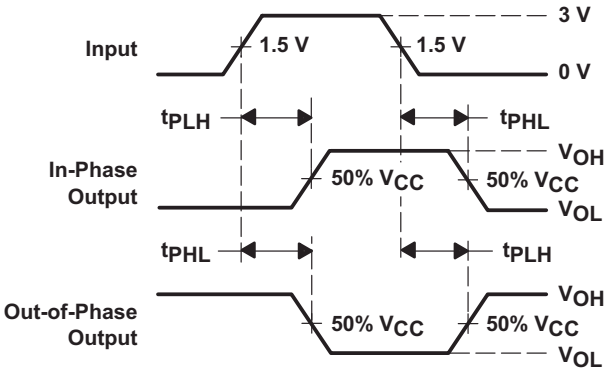
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



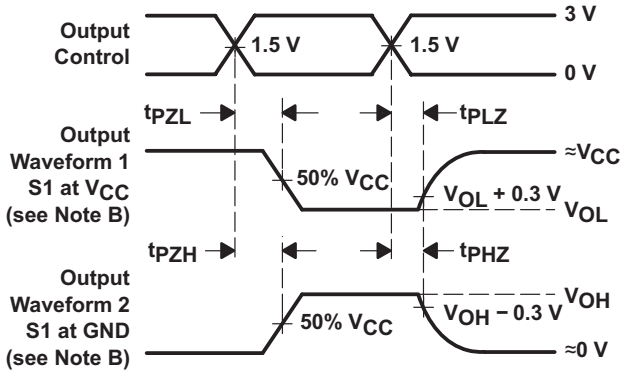
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74LVxTxx family was created to allow up or down voltage translation with only one power rail. The family has over voltage tolerant inputs that allow down translation from up to 5.5V to the Vcc level that can be as low as 1.8V. The family also has a lowered switching threshold that allows it to translate up to the Vcc level that can be as high as 5.5V.

9.1.1 Translating Down

Translating Down Using these parts to translate down is very simple. Since the inputs are tolerant to 5.5V at any valid Vcc they can be used to Down translate. The input can be any level above Vcc up to 5.5V and the output will equal the Vcc level which can be as low as 1.8V. One very good advantage to down translating using this part is that the ICC current will remain less than or equal to the specified value.

Down translation possibilities with SN74LVxTxx

With 1.8V Vcc from 2.5V, 3.3V, or 5V down to 1.8V.

With 2.5V Vcc from 3.3V or 5V down to 2.5V.

With 3.3V Vcc from 5V down to 3.3V.

9.1.2 Translating Up

Once again using the SN74LVxTxx family to translate up is very simple. The input switching threshold is lowered so the high level of the input voltage can be much lower than a typical CMOS VIH. For instance, If the Vcc is 3.3V then the typical CMOS switching threshold would be VCC/2 or 1.65V. This means the input high level must be at least Vcc × 0.7 or 2.31V. On the LV1T devices the input threshold for 3.3V Vcc is approximately 1V. This allows a signal with a 1.8V VIH to be translated up to the Vcc level of 3.3V.

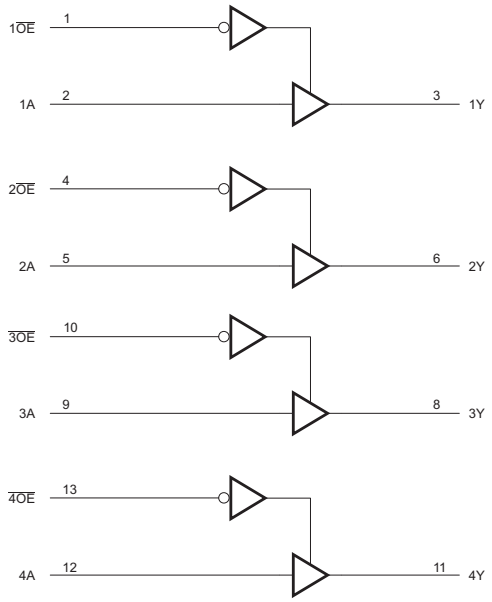
Up translation possibilities with SN74LVxTxx

With 2.5V Vcc from 1.8V to 2.5V.

With 3.3V Vcc from 1.8V or 2.5V to 3.3V.

With 5V Vcc From 2.5V or 3.3V to 5V.

9.2 Functional Block Diagram



9.3 Feature Description

This part is a single supply buffer that is capable up or down translation. The output will equal Vcc while the input can vary from 1.2V to 5.5V.

Up Translation Mode

- 1.2V to 1.8V at 1.8V Vcc
- 1.5V to 2.5V at 2.5V Vcc
- 1.8V to 3.3V at 3.3V Vcc
- 3.3V to 5.0V at 5.0V Vcc

Down Translation Mode

- 3.3V to 1.8V at 1.8V Vcc
- 3.3V to 2.5V at 2.5V Vcc
- 5.0V to 3.3V at 3.3V Vcc

9.4 Device Functional Modes

This device performs the function of a buffer where input logic level equals the output logic level while providing buffering and drive to the output. It will also translate voltages up or down while performing this function.

Function Table (Each Buffer)

INPUTS		OUTPUT Y
OE	A	
L	H	H
L	L	L
H	X	Z

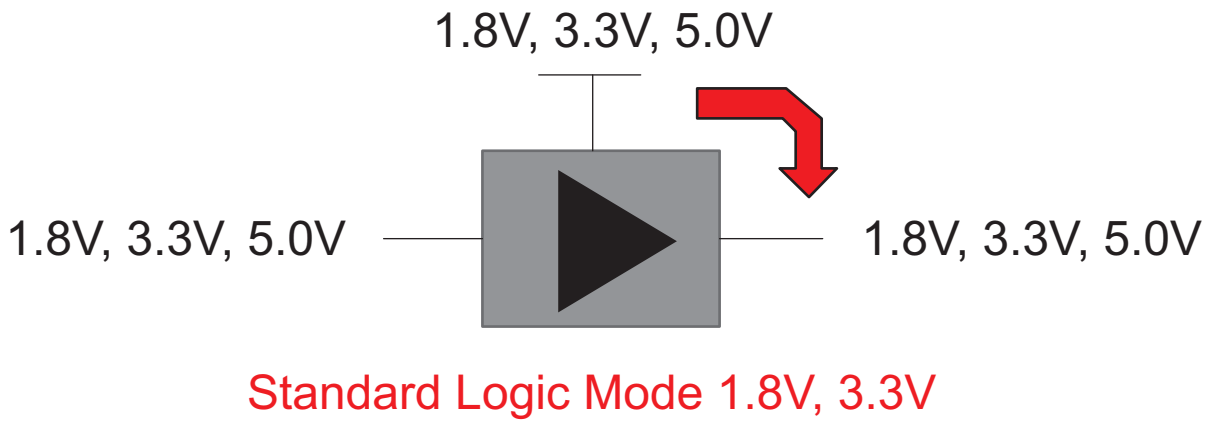
Supply Vcc = 3.3V

INPUT b (Lower Level Input)		OUTPUT (Vcc CMOS)
A	B	Y
VIH(min) = 1.35V		VOH(min) = 2.9V
VIL(max) = 0.8V		VOL(max)= 0.2V

10 Applications and Implementation

10.1 Application Information

Based upon the lower threshold circuit design of LVxT family, the LVxT family also supports level translation. For level translation up and down, the LVxT family only requires a single power supply.



10.2 Typical Application

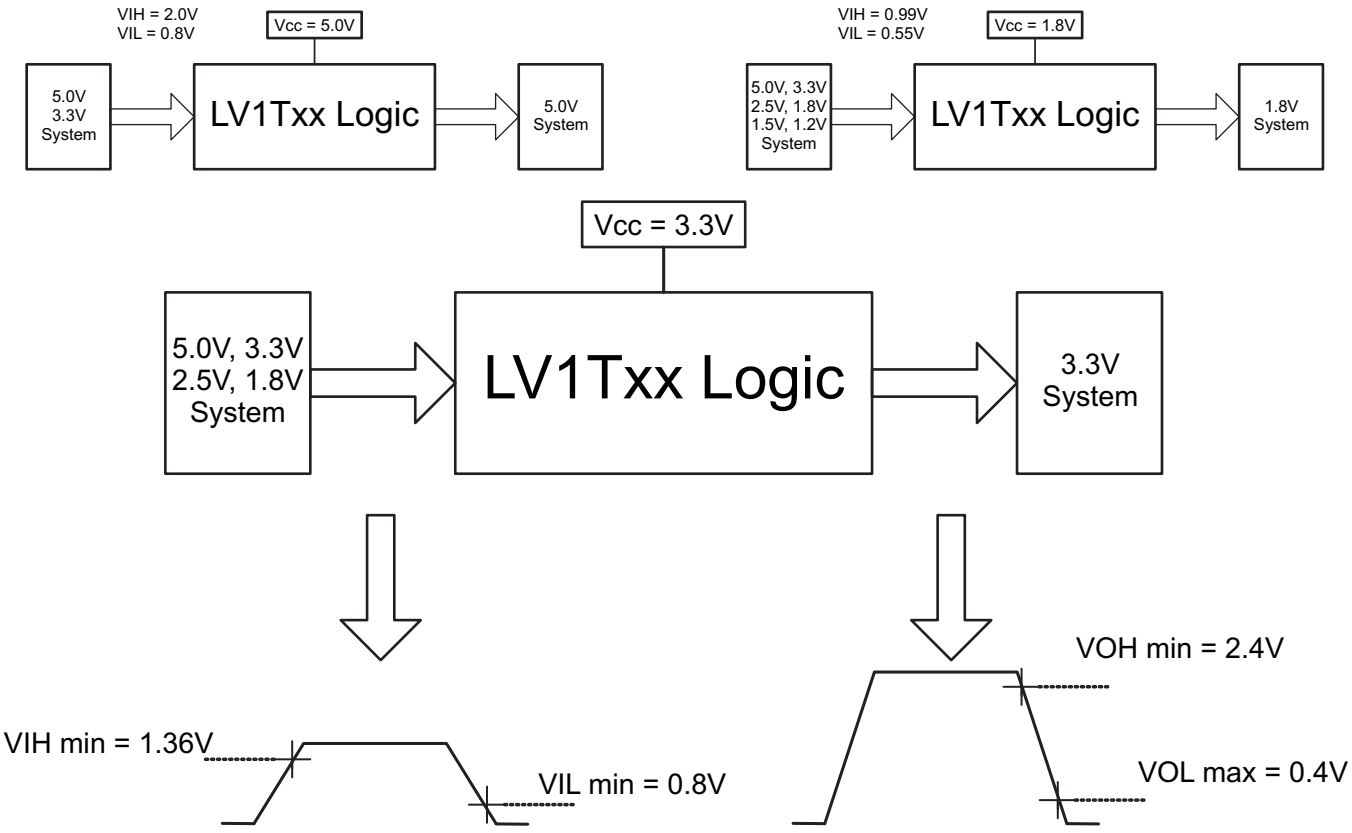


Figure 3. Switching Thresholds for 1.8-V to 3.3-V Translation

Typical Application (continued)

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. The input threshold levels are lowered to allow for up translation. At 5V the device has equivalent TTL input levels.

10.2.2 Detailed Design Procedure

1. Recommended Input conditions
   - Rise time and fall time specs see (Δt/ΔV) in Recommended Operating Conditions table.
   - Specified High and low levels. See (V_{IH} and V_{IL}) in Recommended Operating Conditions table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid Vcc
2. Recommend output conditions
   - Load currents should not exceed 25mA per output and 50mA total for the part
   - Outputs should not be pulled above Vcc

10.2.3 Application Curves

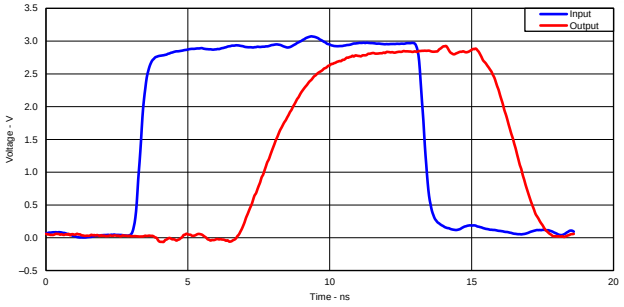


Figure 4. Switching Characteristics at 50 MHz Excellent Signal Integrity (3.3V to 3.3V at 3.3V V_{CC})

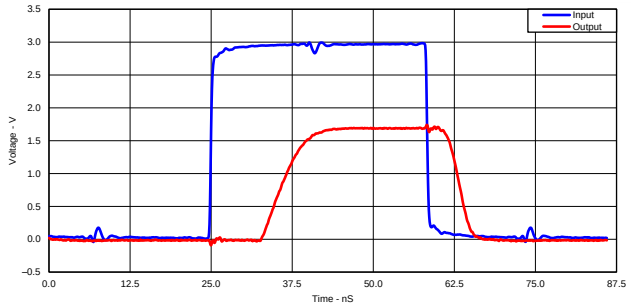


Figure 5. Switching Characteristics at 15 MHz Excellent Signal Integrity (3.3V to 1.8V at 1.8V V_{CC})

11 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the Recommended Operating Conditions.

Each Vcc terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1µf is recommended and if there are multiple Vcc terminals then .01µf or .022µf is recommended for each power terminal. It is ok to parallel multiple bypass caps to reject different frequencies of noise. A 0.1µf and 1µf are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

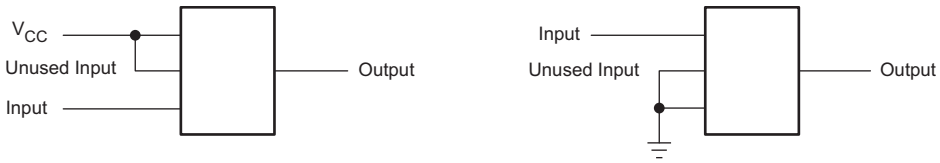
When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or Vcc whichever make more sense or is more convenient.

It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

12.2 Layout Example



13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Additional Product Selection

DEVICE	PACKAGE	DESCRIPTION
SN74LV1T00	DCK, DBV	2-Input Positive-NAND Gate
SN74LV1T02	DCK, DBV	2-Input Positive-NOR Gate
SN74LV1T04	DCK, DBV	Inverter Gate
SN74LV1T08	DCK, DBV	2-Input Positive-AND Gate
SN74LV1T34	DCK, DBV, DRL	Single Buffer Gate
SN74LV1T14	DCK, DBV	Single Schmitt-Trigger Inverter Gate
SN74LV1T32	DCK, DBV	2-Input Positive-OR Gate
SN74LV1T86	DCK, DBV	Single 2-Input Exclusive-Or Gate
SN74LV1T125	DCK, DBV, DRL	Single Buffer Gate with 3-state Output
SN74LV1T126	DCK, DBV, DRL	Single Buffer Gate with 3-state Output
SN74LV4T125	RGY, PW	Quadruple Bus Buffer Gate With 3-State Outputs

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4T125PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		Samples
SN74LV4T125RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

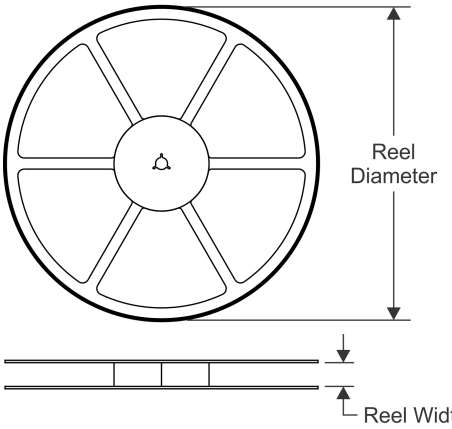
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

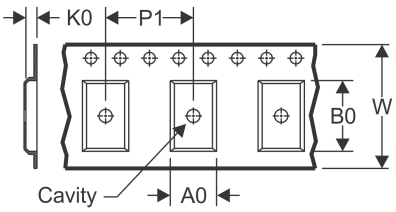
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

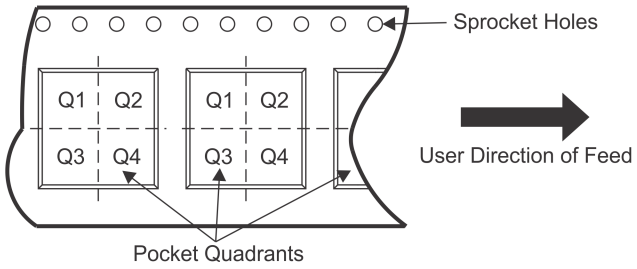


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

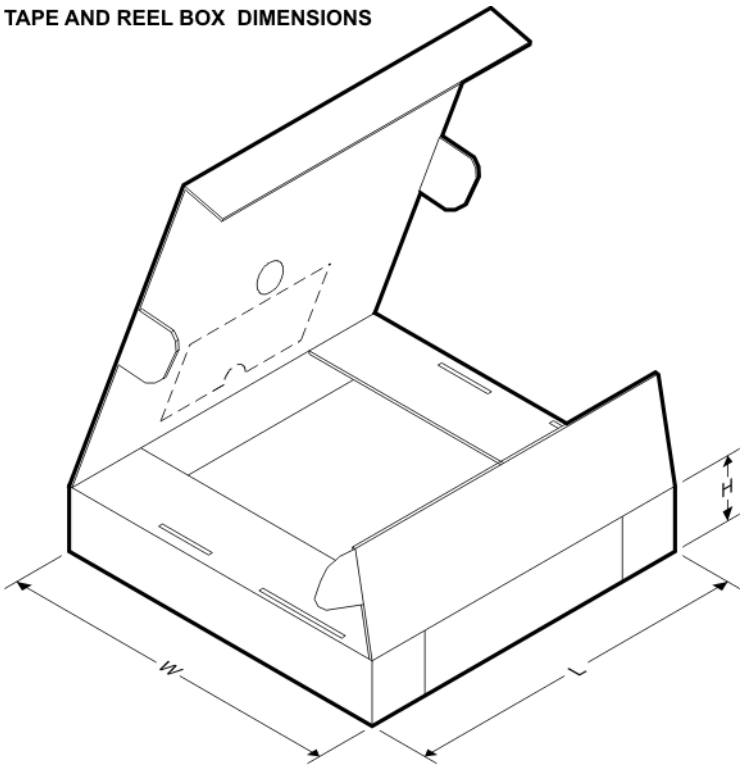
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4T125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4T125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

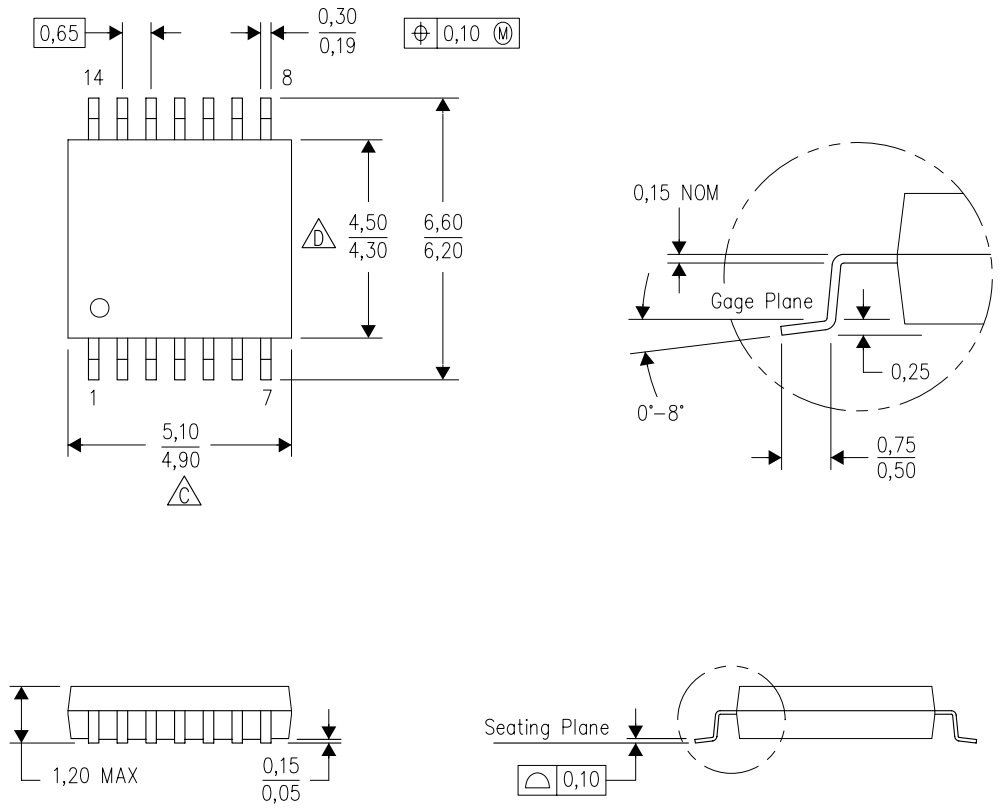
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4T125PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LV4T125RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

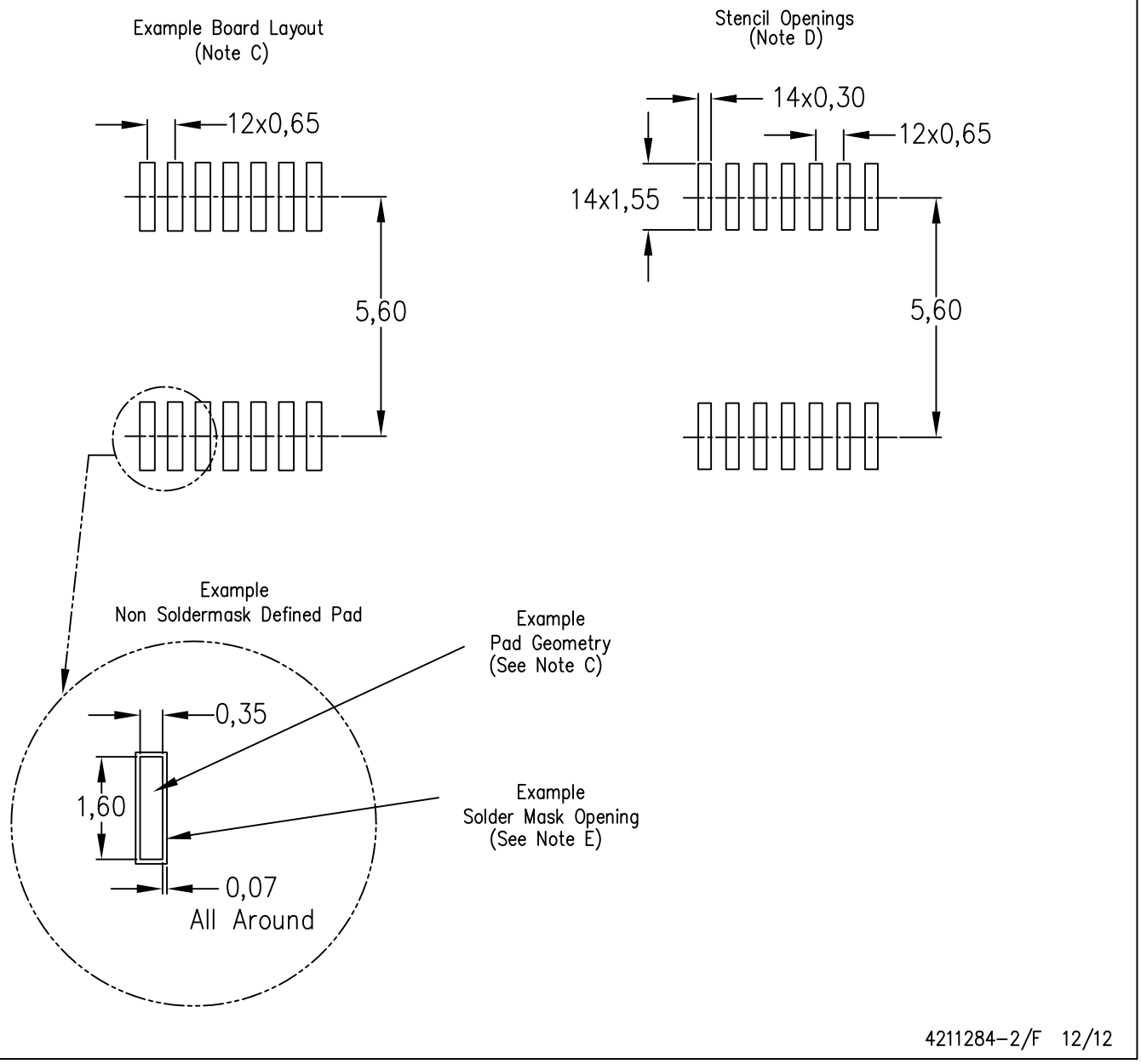
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

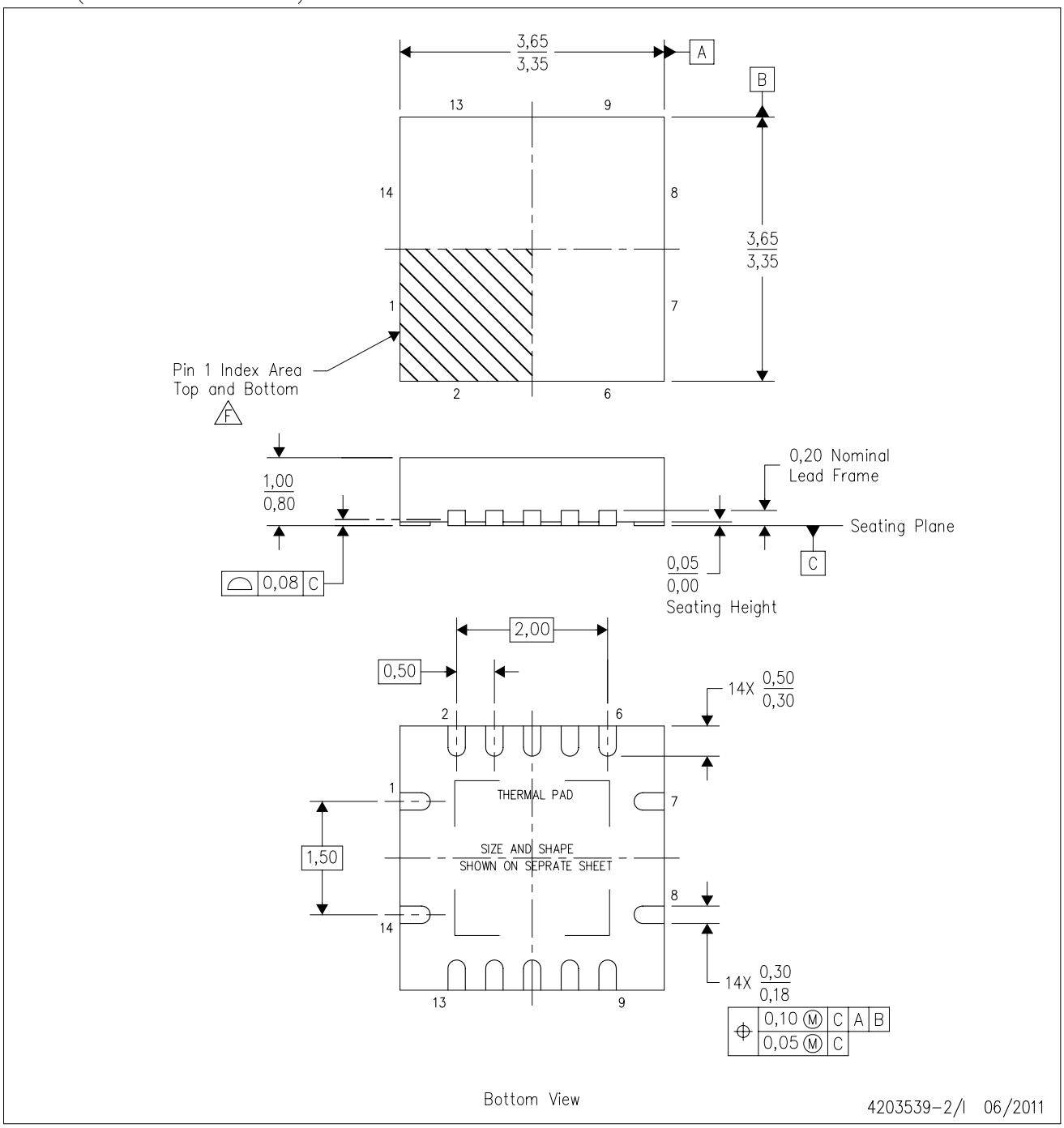
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

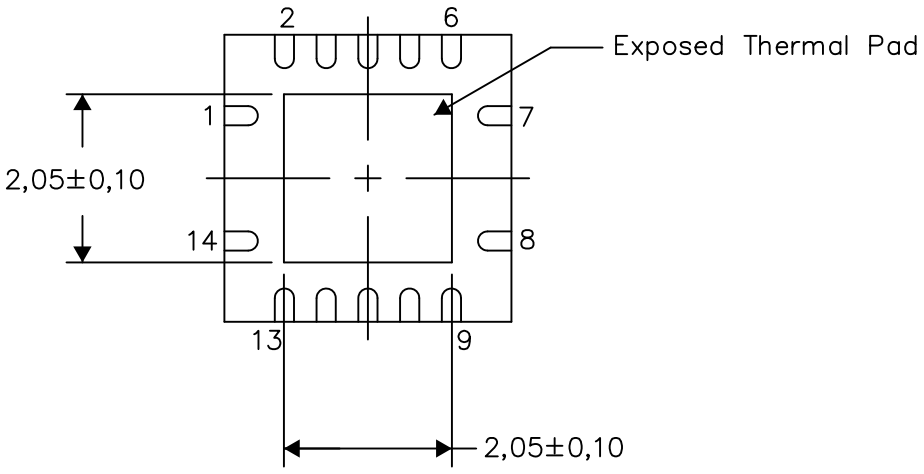
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



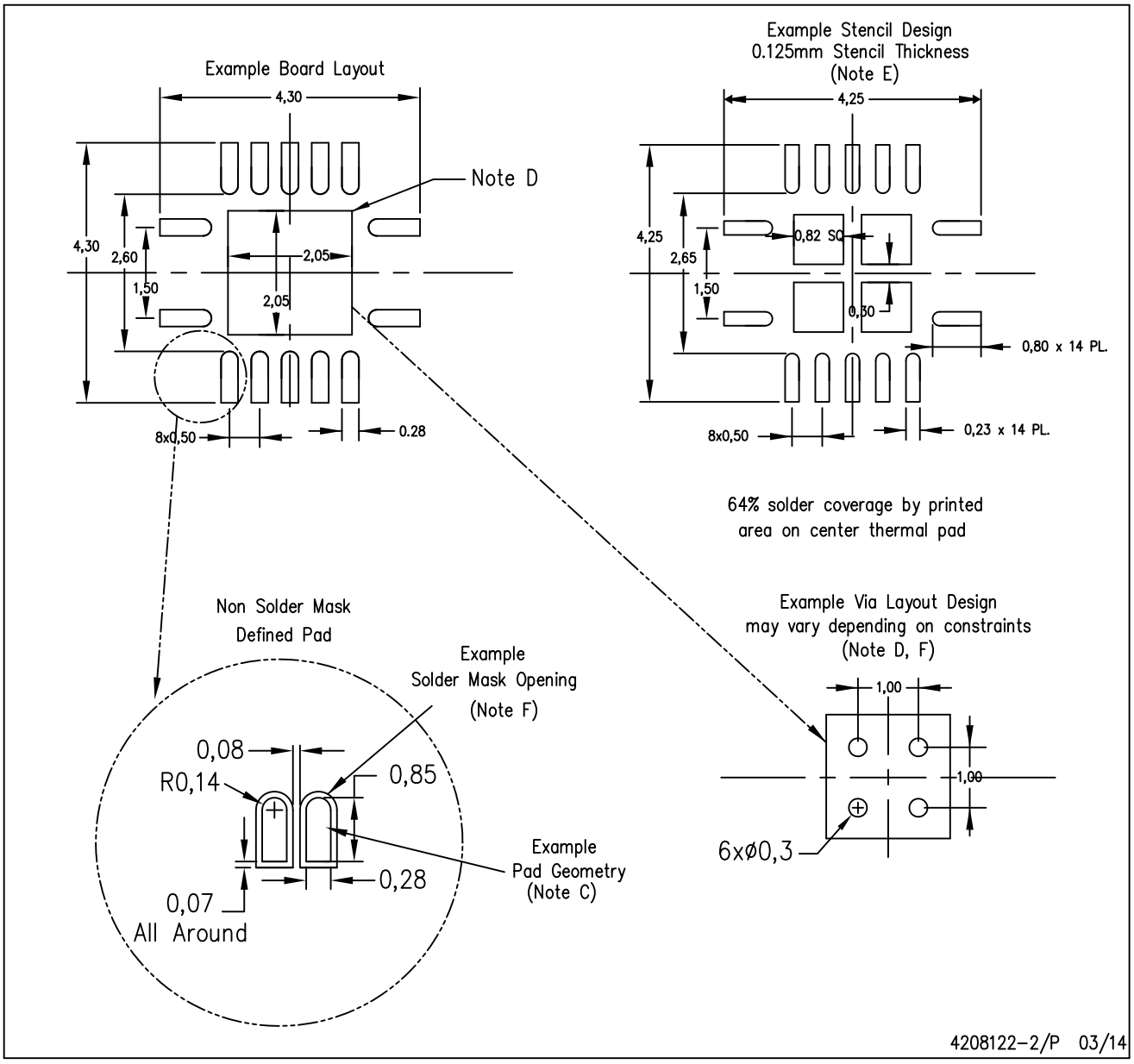
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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