Integrated Circuit Systems, Inc.

ICS9112-26

Low Skew Output Buffer

General Description

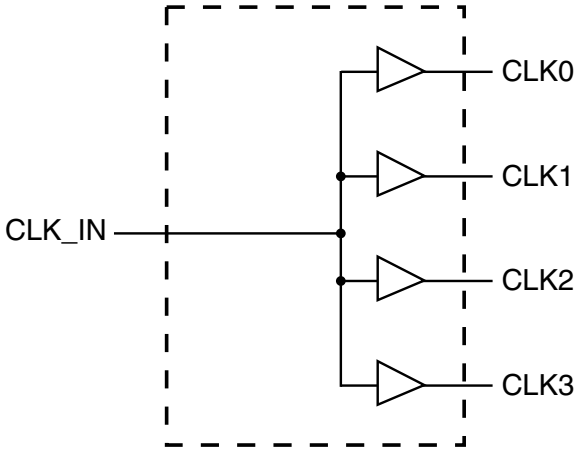
The **ICS9112-26** is a high performance, low skew, low jitter clock driver. It is designed to distribute high speed clocks in PC systems operating at speeds from 0 to 133 MHz.

The **ICS9112-26** comes in an eight pin 150 mil SOIC package. It has four output clocks.

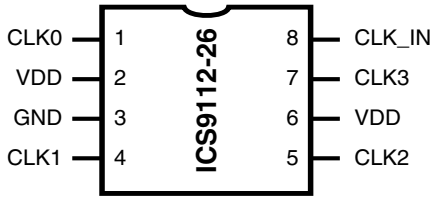
Features

- Frequency range 0 - 133 MHz (3.3V)
- Less than 200 ps Jitter between outputs
- Skew controlled outputs
- Skew less than 250 ps between outputs
- Available in 8 pin 150 mil SOIC & 173 mil TSSOP packages.
- 3.3V ±10% operation

Block Diagram



Pin Configuration



8 pin SOIC & TSSOP

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	CLK0[1]	OUT	Buffered clock output
2,6	VDD	PWR	Power Supply (3.3V)
3	GND	PWR	Ground
4	CLK1[1]	OUT	Buffered clock output
5	CLK2[1]	OUT	Buffered clock output
7	CLK3[1]	OUT	Buffered clock output
8	CLK_IN	IN	Input reference frequency.

Notes:
1. Weak pull-down on all outputs

ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-level Output Voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1 mA	V_{DD} - 0.2	3.3		V
		V_{DD} = 3V, I_{OH} = -24 mA	2	2.9		V
		V_{DD} = 3V, I_{OH} = 12 mA	2.4	3.1		V
Low-level Output Voltage	V_{OL}	V_{DD} = min to max, I_{OH} = 1 mA		0.0055	0.2	V
		V_{DD} = 3V, I_{OH} = 24 mA		0.28	0.8	V
		V_{DD} = 3V, I_{OH} = 12 mA		0.14	0.55	V
High-level Input Current	I_{OH}	V_{DD} = 3V, V_O = 1V		-61	-50	
		V_{DD} = 3.3V, V_O = 1.65V		-77		
Low-level Input Current	I_{OL}	V_{DD} = 3V, V_O = 2V	60	103		
		V_{DD} = 3.3V, V_O = 1.65V		111		
Input Current	I_I	V = V_O or V_{DD}	-5		5	µA
Input Capacitance[1]	C_I	V_{DD} = 3.3V, V_I = 0V or 3.3V		3		pF
Output Capacitance[1]	CO	V_{DD} = 3.3V, V_I = 0V or 3.3V		3.2		pF
Supply current	I_{DD}	REF = 0 MHz		22	50	µA
		Unloaded outputs at 66.67 MHz		25	40	mA

1. Guaranteed by design, not 100% tested in production.

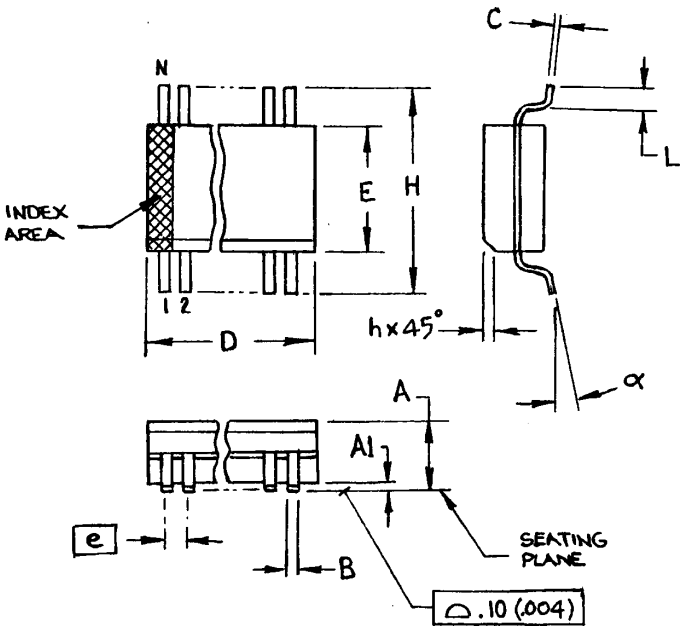
Switching Characteristics at 3.3V

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-to-high Propagation Delay[1]	t_{PLH}	V_O = V_{DD}/2	4	5.6	7	ns
High-to-low Propagation Delay[1]	t_{PHL}	V_O = V_{DD}/2	4	5.2	7	ns
Output Skew Window[1]	T_{sk}(O)	V_O = V_{DD}/2		50	100	ps
Process Skew[1]	T_{sk}(PR)	V_O = V_{DD}/2			0.5	ps
CLKIN High Time[1]	T_{high}	66 MHz	6			ns
		133 MHz	3			
CLKIN Low Time[1]	T_{low}	66 MHz	6			ns
		133 MHz	3			
Output Rise Slew Rate[1]	T_r	0.3 to 0.6 V_{DD}	2	3.6	5	V/ns
Output Rise Slew Rate[1]	T_f	0.3 to 0.6 V_{DD}	2	3.2	5	V/ns

1. Guaranteed by design, not 100% tested in production.

Notes:
1. Guaranteed by design and characterization. Not subject to 100% test.
2. CLK_IN input has a threshold voltage of 1.4V
3. All parameters expected with loaded outputs



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	SEE VARIATIONS		SEE VARIATIONS	
E	3.80	4.0	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	4.80	5.00	.1890	.1968

150 mil (Narrow Body) SOIC

Ordering Information

ICS9112yM-26-T

Example:

ICS XXXX y M - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

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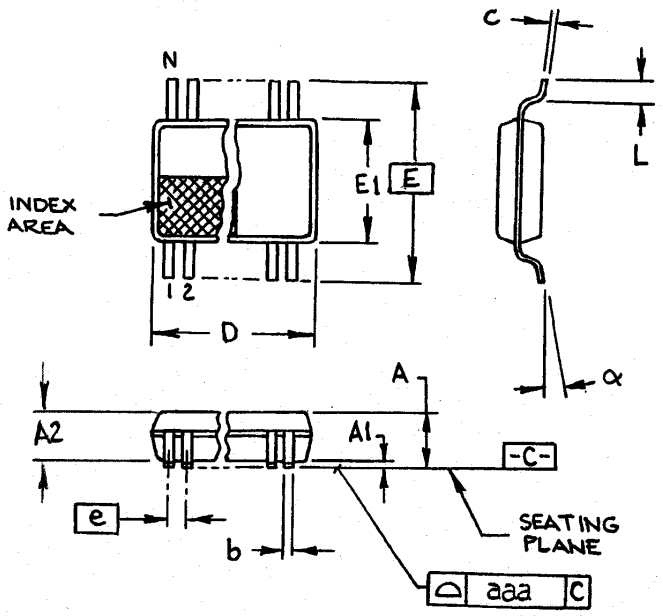

4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	2.90	3.10	.114	.122

MO-153 JEDEC 7/6/00 Rev B
Doc.# 10-0038

Ordering Information

ICS9112yG-26-T

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
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You may also like...

9112-26 (Single-ended I/O Fan-out and Zero Delay Buffers)

Description
Clock Buffer
Market Group
PC CLOCK
Additional Info
The ICS9112-26 is a high performance, low skew, low jitter clock driver. It is designed to distribute high speed clocks in PC systems operating at speeds from 0 to 133 MHz.

Related Orderable Parts

1 2

Attributes	9112AG-26	9112AG-26LF	9112AG-26LFT	9112AG-26T	9112AM-26	9112AM-26LF
Voltage	3.3 V (PG8)	3.3 V (PGG8)	3.3 V (PGG8)	3.3 V (PG8)	3.3 V (DC8)	3.3 V (DCG8)
Package	TSSOP 8	TSSOP 8	TSSOP 8	TSSOP 8	SOIC 8	SOIC 8
Speed	NA	NA	NA	NA	NA	NA
Temperature	C	C	C	C	C	C
Status	Active	Active	Active	Active	Active	Active
Sample	No	Yes	Yes	No	Yes	Yes
Minimum Order Quantity	192	192	2500	2500	194	194
Factory Order Increment	96	96	2500	2500	97	97

1 2

Related Documents

Type	Title	Size	Revision Date
Datasheet	9112-26 Datasheet	86 KB	05/14/2007

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Voltage	3.3 V (PG8)	3.3 V (PGG8)	3.3 V (PGG8)	3.3 V (PG8)	3.3 V (DC8)	3.3 V (DCG8)
Package	TSSOP 8	TSSOP 8	TSSOP 8	TSSOP 8	SOIC 8	SOIC 8
Speed	NA	NA	NA	NA	NA	NA
Temperature	C	C	C	C	C	C
Status	Active	Active	Active	Active	Active	Active
Sample	No	Yes	Yes	No	Yes	Yes
Minimum Order Quantity	192	192	2500	2500	194	194
Factory Order Increment	96	96	2500	2500	97	97

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Related Documents

Type	Title	Size	Revision Date
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