



ADC-574Z, -674Z

12-Bit, μ P-Compatible A/D Converter with S/H

PRODUCT DATA

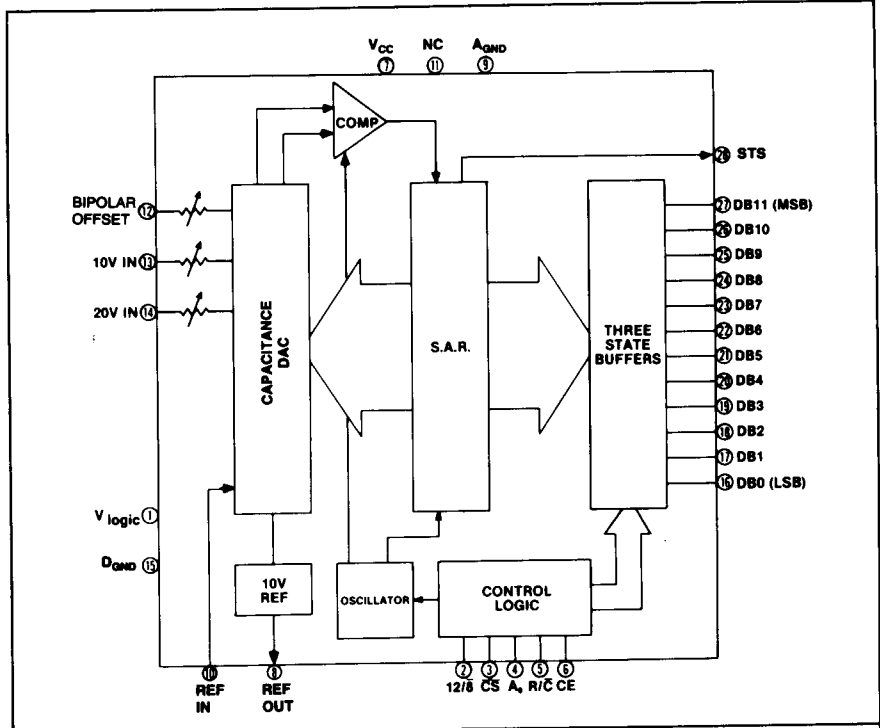
FEATURES

- Complete 12-Bit A/D converters with sample-hold, reference, and clock
- Pin-to-pin compatible with industry standard HI574A/674A
- No missing codes over temperature
- 15 μ Sec. Conversion time (ADC-674Z)
- 150 mW maximum power dissipation

GENERAL DESCRIPTION

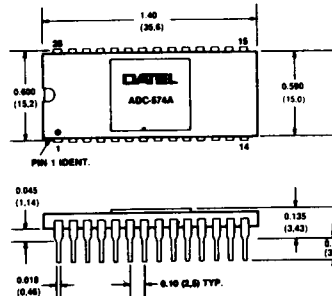
DATEL's ADC-574Z/674Z family of A/D converters are single chip monolithic CMOS versions of the industry standard devices. The sample-hold feature of this device allows conversion of input frequencies of up to 5 KHz without requiring an external circuit.

These units include a reference, clock, three-state outputs, and digital interface circuit which allows direct connection to the microprocessor address bus and control lines. The ADC-574Z completes a 12-bit conversion in microseconds, while the ADC-674Z converts in 15 microseconds. Four user selectable input ranges are provided: 0 to +10V, 0 to +20V, ± 5 V, and ± 10 V dc. Laser trimming ensures specified linearity, gain, and offset accuracy.



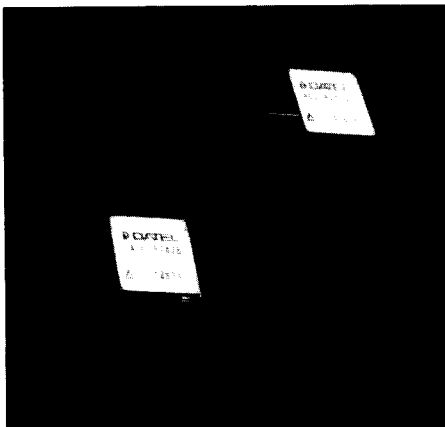
MECHANICAL DIMENSIONS

INCHES (MM)



INPUT/OUTPUT CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
|-----|---|-----|------------------|
| 1 | V _{logic} +5V | 15 | D _{GND} |
| 2 | 12/8, DATA MODE SELECT | 16 | DB0 (LSB) |
| 3 | CS, CHIP SELECT | 17 | DB1 |
| 4 | A _n , BYTE ADDRESS/SHORT CYCLE | 18 | DB2 |
| 5 | R/C, READ/CONVERT | 19 | DB3 |
| 6 | CE, CHIP ENABLE | 20 | DB4 |
| 7 | V _{CC} | 21 | DB5 |
| 8 | REFERENCE OUT | 22 | DB6 |
| 9 | A _{GND} | 23 | DB7 |
| 10 | REFERENCE IN | 24 | DB8 |
| 11 | NC | 25 | DB9 |
| 12 | BIPOLAR OFFSET | 26 | DB10 |
| 13 | 10V IN | 27 | DB11 (MSB) |
| 14 | 20V IN | 28 | STS |



ADC-574Z, -674Z 12-Bit, Microprocessor-Compatible A/D Converter with S/H

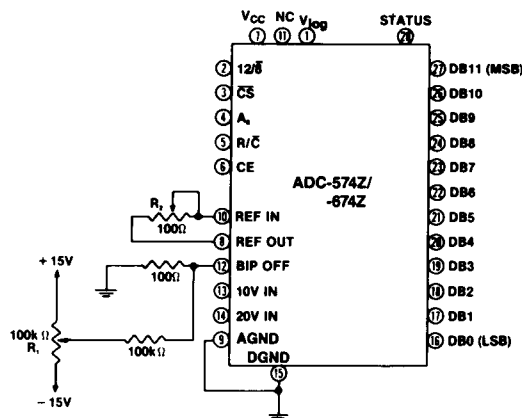
SPECIFICATION FOOTNOTES:

1. Available for external loads. External load should not change during conversion. When supplying an external load and operating on $\pm 12V$ supplies, a buffer amplifier must be provided for the reference output.
2. Logic Inputs — CE, \overline{CS} , R/\overline{C} , A_0 , 12/8.
3. Logic Outputs — DB11-DB0, STS.
4. Over temperature.
5. Adjustable to zero.
6. With 50 Ω fixed resistor from REF OUT to REF IN. Adjustable to zero.
7. No adjustment at 25°C.
8. With adjustment at 25°C.
9. Guaranteed maximum change, T_{min} to T_{max} (using internal reference).
10. Maximum change in full scale calibration.

TECHNICAL NOTES

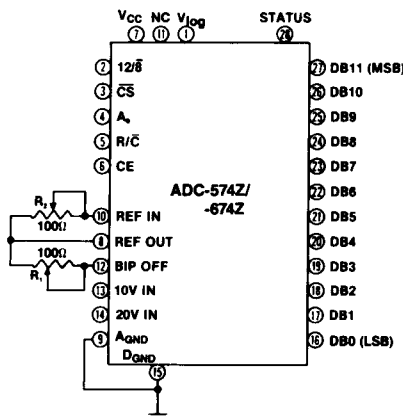
1. The ADC-574Z, -674Z may interface directly to a microprocessor which can take full control of each conversion, or the device can be operated in the "stand alone" mode (controlled only by the R/\overline{C} input). Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion and reading the output data when ready. The data may be read 12 bits at once or 8 followed by 4 in a left-justified format. There are five control inputs (12/8, \overline{CS} , A_0 , R/\overline{C} and CE) and all are TTL/CMOS compatible. (See Control Input Truth Table.)
2. A conversion is initiated by a logic transition on any of the three inputs: CE, \overline{CS} , R/\overline{C} . One, two, or all three may be dynamically controlled. The nominal delay for each of the three inputs is the same and if necessary, all three may change states simultaneously. If it is required that a particular input controls the start of conversion, the other two should be set up at least 50 nanoseconds earlier. (See Start Convert Timing.)
3. To read the output data, four conditions must be met (or the output buffers will remain in high impedance state): R/\overline{C} taken high, STS low, CE high and \overline{CS} low. When this is accomplished, the data lines are activated according to the state of the 12/8 and A_0 inputs. (See START CONVERT, READ CYCLE TIMING and APPLICATION.)
4. The analog signal source driving the ADC-574Z, -674Z's input will see a nominal load of 5 K Ω (10V range) or 10 K Ω (20V range). However, the other end of these input resistors may change 400 mV with each bit decision, causing sudden changes in current at the analog input. Therefore, the signal source must maintain its output voltage while supplying these step changes in load current which occur at 1.6 microsecond intervals. This requires low output impedance and fast settling by the signal source. If a sample/hold is required to precede the converter, DATEL's SHM-20 is recommended.
5. The power supply used should be low noise and well regulated. Voltage spikes can affect accuracy. If a switching supply is used, the outputs should be carefully filtered to assure "noise free" dc voltage to the converter. Decoupling capacitors should be used on all power supply pins; the +5V dc supply decoupling capacitor should be connected directly from + V_{logic} (Pin 1) to digital common (Pin 15). V_{CC} (Pin 7) should be decoupled directly to A_{GND} (Pin 9). It is recommended that a 10 μF tantalum type in parallel with a 0.1 μF ceramic type be used for decoupling.
6. The use of good circuit board layout techniques is required for rated performance. It is recommended that a double sided printed circuit board with a ground plane on the component side is used. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard will have an unpredictable effect on accuracy. Sensitive analog signals should be routed between ground traces and kept away from digital lines. If analog and digital lines must cross, they should do so at right angles.

TYPICAL CONNECTIONS



UNIPOLAR CONFIGURATION

NOTES: The trimpots shown are for calibration of offset and gain. If adjustment is not required in unipolar; replace R_2 with a 50 Ω , 1% metal film resistor, omit the network on Pin 12 and connect Pin 12 to Pin 9. In bipolar; either R_1 , or R_2 or both can be replaced by 50 Ω , 1% metal film resistors.



BIPOLAR CONFIGURATION

CODING TABLES

| INPUT RANGE | | OUTPUT CODING | | |
|-------------|-----------|---------------|------|-------|
| 0 to +10V | 0 to +20V | MSB | | LSB |
| +10.000 | +20.0000 | 1111 | 1111 | 1111 |
| +9.9963 | +19.9927 | 1111 | 1111 | 1110* |
| +5.0012 | +10.0024 | 1000 | 0000 | 0000* |
| +4.9988 | +9.9976 | 0000 | 0000 | 0000* |
| +4.9963 | +9.9927 | 0111 | 1111 | 1110* |
| +0.0012 | +0.0024 | 0000 | 0000 | 0000* |
| 0.0000 | +0.0000 | 0000 | 0000 | 0000 |

| INPUT RANGE | | OUTPUT CODING | | |
|-------------|-----------|---------------|------|-------|
| $\pm 5V$ | $\pm 10V$ | MSB | | LSB |
| +5.0000 | +10.0000 | 1111 | 1111 | 1111 |
| +4.9963 | +9.9927 | 1111 | 1111 | 1110* |
| +0.0012 | +0.0024 | 1000 | 0000 | 0000* |
| -0.0012 | -0.0024 | 0000 | 0000 | 0000* |
| -0.0037 | -0.0073 | 0111 | 1111 | 1110* |
| -4.9988 | -9.9976 | 0000 | 0000 | 0000* |
| -5.0000 | -10.0000 | 0000 | 0000 | 0000 |

*Voltages shown are theoretical values for the transitions indicated. Ideally, in the continuous conversion mode, the output bits indicated as \emptyset will change from "1" to "0" or "0" to "1" as the input voltage passes through the level indicated.

Output coding is straight binary for unipolar and offset binary for bipolar.

CALIBRATION

UNIPOLAR CALIBRATION

Offset Adjust

Apply an input of $+ \frac{1}{2}$ LSB (+1.22 mV for the 10V range; +2.44 mV for the 20V range). Adjust the offset trimpot (R_1) until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Gain Adjust

Apply $1\frac{1}{2}$ LSB's below the nominal full-scale (+9.9963V for the 10V range; +19.9927V for the 20V range). Adjust the gain trimpot (R_2) so that the output flickers between 1111 1111 1110 and 1111 1111 1111.

BIPOLAR CALIBRATION

Offset Adjust

Apply $\frac{1}{2}$ LSB above negative full-scale ($-4.9988V$ for the $\pm 5V$ range; $-9.9976V$ for the $\pm 10V$ range.) Adjust the offset trimpot (R_1) so that the output flickers between 0000 0000 0000 and 0000 0000 0001.

Gain Adjust

Apply $1\frac{1}{2}$ LSB's below positive full scale (+4.9963V for the $\pm 5V$ range; +9.9927V for the $\pm 10V$ range). Adjust the gain trimpot (R_2) so that the output flickers between 1111 1111 1110 and 1111 1111 1111.

TIMING CONTROL

The variety of the ADC-574Z, -674Z's control modes (as shown in the "CONTROL INPUTS TRUTH TABLE") allow for simple interface in most system applications.

The output signal STS indicates the status of the device; high during a conversion, and low at the completion of a conversion. During a conversion (STS output high), the output buffers remain in the high impedance state and data cannot be read. A start convert during conversion will not reset the converter or reinitiate a conversion. However, if A_0 changes state after a conversion begins, an additional start convert pulse will latch the new state of A_0 , causing a wrong cycle length for that conversion.

Control Inputs Truth Table

| CE | \overline{CS} | R/C | 12/8 | A_0 | OPERATION |
|-----|-----------------|-----|------|-------|---|
| 0 | X | X | X | X | None |
| X | 1 | X | X | X | None |
| 0-1 | 0 | 0 | X | 0 | Initiate 12-bit conversion |
| 0-1 | 0 | 0 | X | 1 | Initiate 8-bit conversion |
| 1 | 1-0 | 0 | X | 0 | Initiate 12-bit conversion |
| 1 | 1-0 | 0 | X | 1 | Initiate 8-bit conversion |
| 1 | 0 | 1-0 | X | 0 | Initiate 12-bit conversion |
| 1 | 0 | 1-0 | X | 1 | Initiate 8-bit conversion |
| 1 | 0 | 1 | 1 | X | Initiate 12-bit conversion |
| 1 | 0 | 1 | 0 | 0 | Enable's 8 MSB's only |
| 1 | 0 | 1 | 0 | 1 | Enable's 4 LSB's plus 4 trailing zeroes |

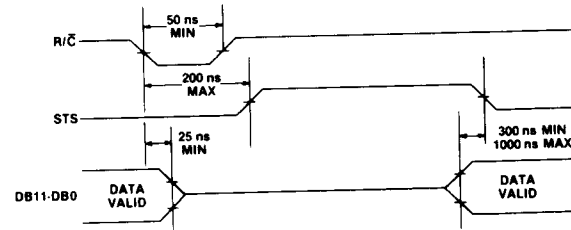
TIMING AND OPERATION

Stand-Alone Mode Timing

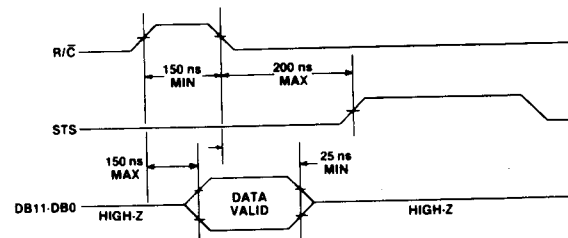
For stand-alone operation, all that is required is a single control line to R/C. CE and 12/8 are tied high, \overline{CS} and A_0 are tied low, and the output appears in words of 12 bits.

The R/C signal may have any duty cycle within the limits shown in the diagrams below.

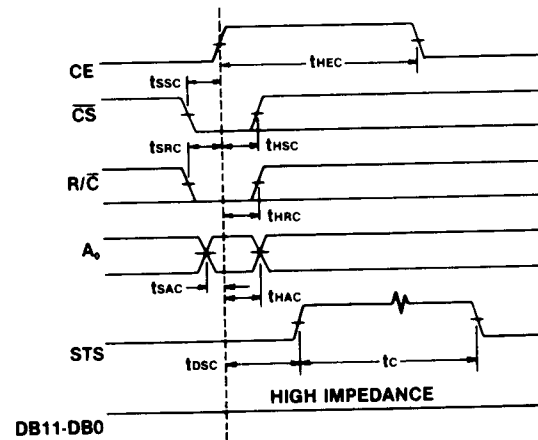
The data may be read when R/C is high unless STS is also high indicating a conversion is in progress.



Outputs Enabled After Conversion

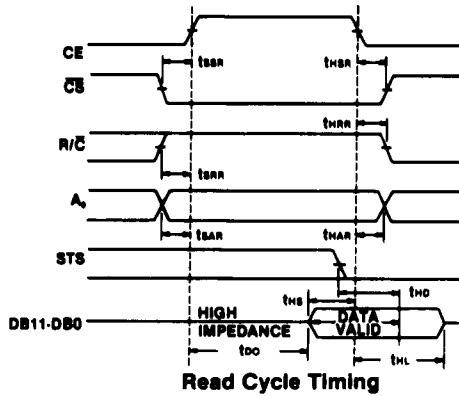


Outputs Enabled With R/C High



Start Convert Timing

A read operation in most applications begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. (See Technical Note 3.)



| Symbol | Parameter | Min. | Typ. | Max. |
|------------------|-----------------------------------|--------|--------|---------|
| t _{DD} | Access Time from CE | — | 75 nS | 150 nS |
| t _{HD} | Data Valid after CE low | 25 nS | 35 nS | — |
| t _{HL} | Output Float Delay | — | 100 nS | 150 nS |
| t _{SSR} | CS̄ to CE Setup | 50 nS | 0 | — |
| t _{SRR} | R/C̄ to CE Setup | 0 | 0 | — |
| t _{SAR} | A ₀ to CE Setup | 50 nS | 25 nS | — |
| t _{HSR} | CS̄ Valid after CE Low | 0 | 0 | 0 |
| t _{HRR} | R/C̄ High after CE Low | 0 | 0 | 0 |
| t _{HAR} | A ₀ Valid after CE Low | 50 nS | 25 nS | — |
| t _{HS} | STS Delay after Data Valid | | | |
| | -574Z | 300 nS | — | 1000 nS |
| | -674Z | 100 mS | — | 600 mS |

ADC-574Z, 674Z Convert Mode Timing

| Symbol | Parameter | Min. | Typ. | Max. |
|------------------|-------------------------------------|-------|--------|--------|
| t _{DSC} | STS Delay From CE | — | 100 nS | 200 nS |
| t _{HEC} | CE Pulse Width | 50 nS | 30 nS | — |
| t _{SSC} | CS̄ to CE Setup | 50 nS | 20 nS | — |
| t _{HSC} | CS̄ Low during CE High | 50 nS | 20 nS | — |
| t _{SRC} | R/C̄ to CE Setup | 50 nS | 0 | — |
| t _{HRC} | R/C̄ Low during CE High | 50 nS | 20 nS | — |
| t _{SAC} | A ₀ to CE Setup | 0 | 0 | 0 |
| t _{HAC} | A ₀ Valid during CD High | 50 nS | 20 nS | — |
| t _C | Conversion Time, -574Z | | | |
| | 12-bit cycle | 15 μS | 18 μS | 25 μS |
| | 8-bit cycle | 10 μS | 13 μS | 17 μS |
| | Conversion Time, -674Z | | | |
| | 12-bit cycle | 9 μS | — | 15 μS |
| | 8-bit cycle | 6 μS | — | 10 μS |

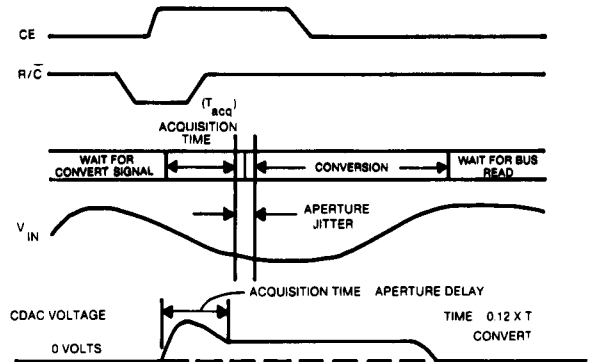
Built-in Sample/Hold

Both the ADC-574Z and the ADC-674Z contain internal sample-and-hold (S/H) capable of sampling inputs up to 5 KHz.

The R/C̄ line controls the internal S/H. The 574Z/674Z sampling and conversion sequence begins when the R/C̄ line makes a negative transition.

After the first two clock cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

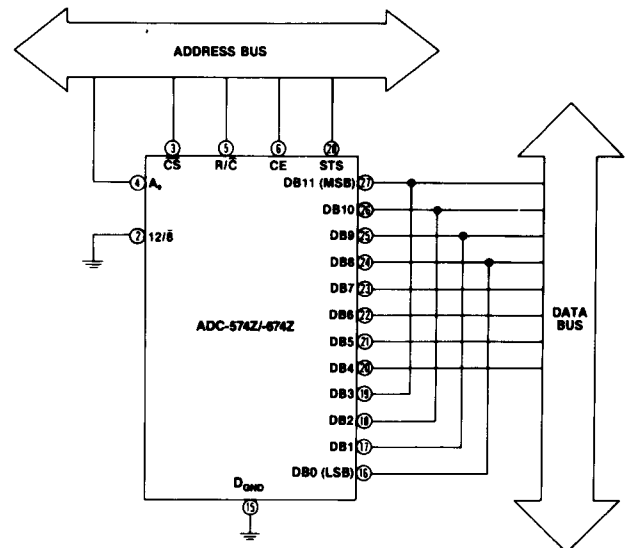
Since the sample is taken relative to the R/C̄ transition, T_{acq} is also the "aperture delay" of the S/H. The duration of T_{acq} is measured in clock cycles and is specified as 2.4 μS ± 0.6 μS for the 574Z and 1.4 μS ± 0.4 μS for the 674Z. The "aperture jitter" nominally allows converting signals of up to 5 KHz without an external sample-hold. Above 5 KHz, the internal S/H will be transparent.



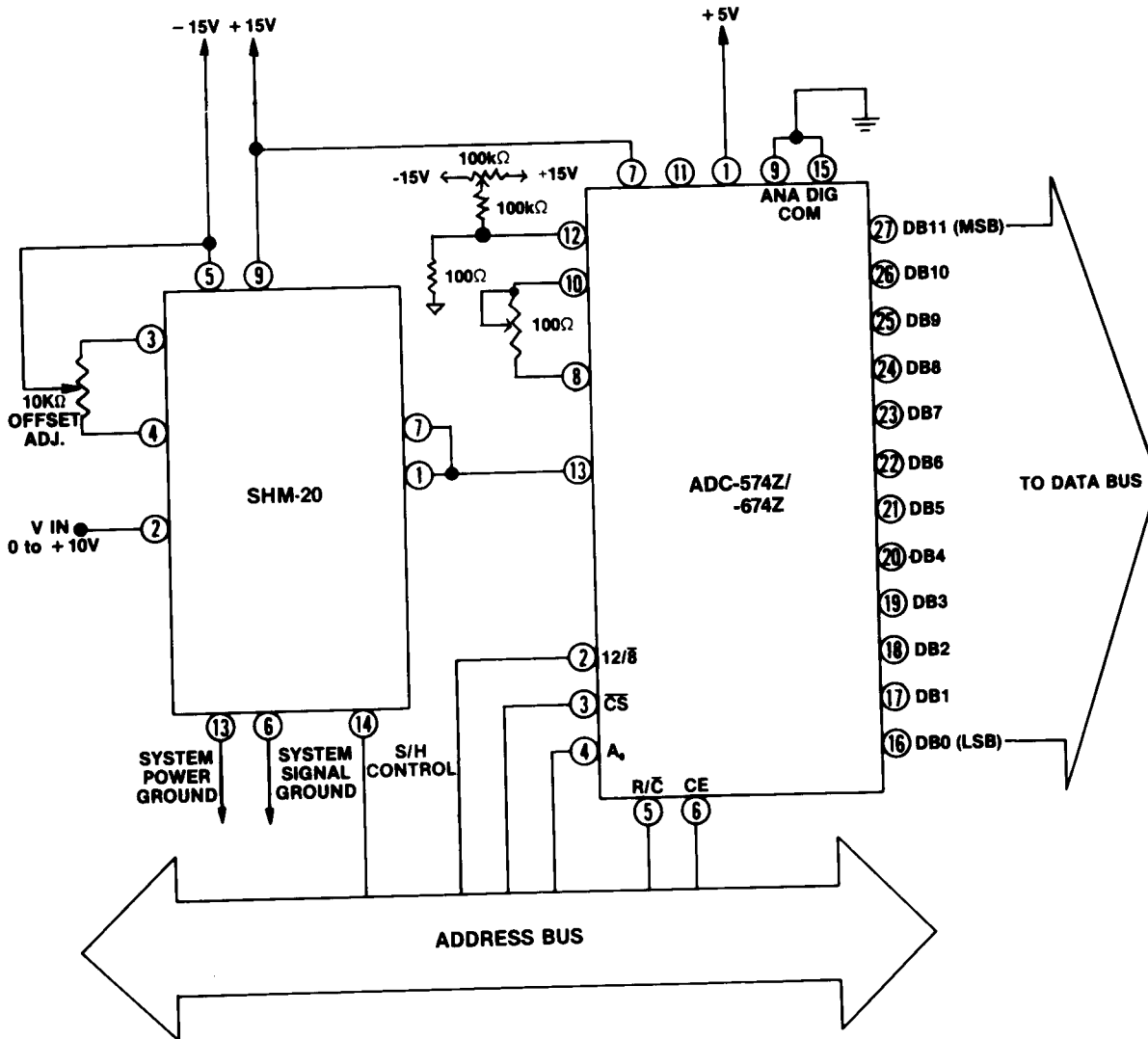
Interface To An 8-Bit Data Bus

Interface To An 8-Bit Data Bus

The 12/8̄ input will be tied either high or low in most applications. With 12/8̄ high, all 12 output lines become active simultaneously for interface to a 12- or 16-bit data bus. A₀ is ignored. Taking 12/8̄ low organizes the output in two 8-bit bytes, which are selected one at a time by A₀. This allows an 8-bit data bus to be connected as shown above. A₀ is normally tied to the LSB of the address bus for storing the converter's output in two consecutive memory locations. This two byte format is called "left justified data" for which a decimal point is assumed to the left of byte 1. In addition, A₀ may be toggled at any time without damage to the converter. Break-before-make switching is guaranteed between two data bytes, which assures that the outputs strapped together as shown are never enabled at the same time.



FAST A/D WITH SAMPLE HOLD



The above diagram shows the ADC-574Z, -674Z configured for unipolar (0 to + 10V) operation. Preceding the ADC-574Z, -674Z is DATEL's SHM-20, a 1 microsecond precision sample/hold. All sample/hold amplifiers are compatible with the ADC-574Z, -674Z; however, many will require an additional wide-band buffer amplifier to reduce their output impedance.

ORDERING INFORMATION

| MODEL NO. | TEMPCO |
|-----------|-----------|
| ADC-574ZC | 45 ppm/°C |
| ADC-574ZB | 25 ppm/°C |
| ADC-574ZA | 10 ppm/°C |
| ADC-674ZC | 45 ppm/°C |
| ADC-674ZB | 25 ppm/°C |
| ADC-674ZA | 10 ppm/°C |

ACCESSORIES

| Part Number | Description |
|-----------------|-------------------------|
| TP100 or TP100K | Trimming Potentiometers |

DS-0036B

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