PS4581/PS4582/PS4583

8-Channel CMOS Multiplexers
Triple SPDT Switch

Features

- Low On-resistance: 50 ohms typical, with ±5V Supplies
- On-Resistance Matching Between Channels: 4 ohms
- Guaranteed Low Leakage Currents: <1nA at +25°C
- Rail-to-Rail Analog Signal Range.
- Low Distortion: <0.02% (600ohms)
- Low Crosstalk: –96dB @1 MHz.
- TTL/CMOS Compatible
- Wide Supply Voltage Operation
  – Single Supply: 2V to 12V
  – Dual Supply: ±2V to ±6V
- Low Power Consumption.
- Pin-Compatible Upgrades for 74HC4051/4052/4053 and MAX4051/4052/4053
- 16-pin SOIC and QSOP Packages Save Board Area

Applications

- Audio and Video Switching and Routing
- Lab and Medical Instrumentation
- Low-Voltage Data-Acquisition and Process-Control Systems
- Battery-Powered Communication Systems

Description

The PS4581 is an eight-channel, single-ended multiplexer designed to select one of eight inputs to a common output. The input selected depends on the status of three address bits (ADDA,ADDB, and ADDC). The PS4582 is a differential four-channel multiplexer, controlled by two address bits: ADDA and ADDB. The PS4583 is a triple SPDT, single-pole, double-throw switch.

The INH (inhibit) pin is driven high to open all switches regardless of address bit status. All control inputs are TTL compatible with a single 5V or dual ±5V supply.

These devices are designed to operate with dual power supplies from ±2V to ±6V. Single-supply operation is possible from +2V to +12V.

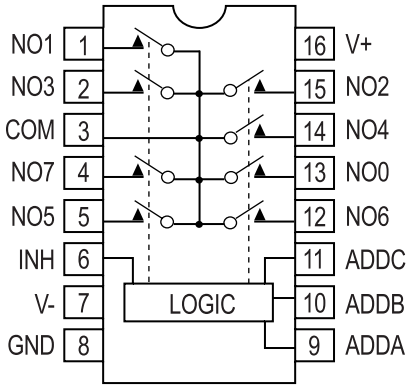
When on, each switch conducts current equally well in either direction and can handle rail-to-rail analog signals. In the off-state, each switch blocks voltages up to the power-supply rails. Off-leakage current is guaranteed to be less than 7nA at +25°C, or 50nA at +85°C

These devices are available in 16-pin DIP, SOIC, and QSOP packages for operation over the –40°C to +85°C temperature range.

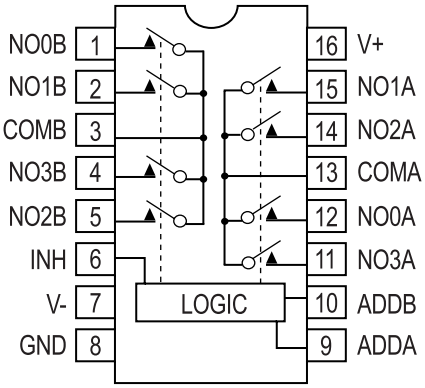
Functional Block Diagrams and Pin Configurations

Top Views

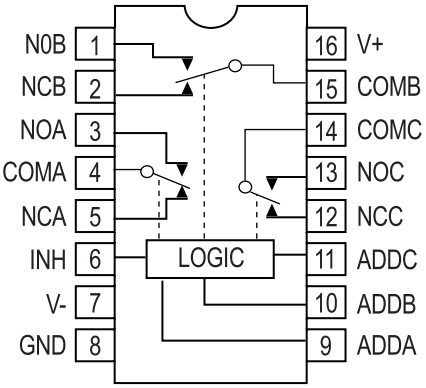
PS4581



PS4582



PS4583



INH = 1 Turn all switches OFF

Truth Tables

PS4581				
INH	**ADDC**	**ADDB**	**ADDA**	**On Switch**
1	X	X	X	All Switches OFF
0	0	0	0	NO0
0	0	0	1	NO1
0	0	1	0	NO2
0	0	1	1	NO3
0	1	0	0	NO4
0	1	0	1	NO5
0	1	1	0	NO6
0	1	1	1	NO7

PS4582			
INH	**ADDB**	**ADDA**	**On Switch**
1	X	X	All Switches OFF
0	0	0	NO0A,B
0	0	1	NO1A,B
0	1	0	NO2A,B
0	1	1	NO3A,B

PS4583						
INH	**ADDC**	**ADDB**	**ADDA**	**On Switches**		
1	X	X	X	All Switches OFF		
0	0	0	0	NOC	NOB	NOA
0	0	0	1	NOC	NOB	NCA
0	0	1	0	NOC	NCB	NOA
0	0	1	1	NOC	NCB	NCA
0	1	0	0	NCC	NOB	NOA
0	1	0	1	NCC	NOB	NCA
0	1	1	0	NCC	NCB	NOA
0	1	1	1	NCC	NCB	NCA

Logic "0", $V_{AL} \leq 0.8V$
Logic "1", $V_{IH} \geq 2.4V$

Absolute Maximum Ratings

Voltages Referenced to V-

V+ ..... –0.3V to +17V

GND ..... –0.3V to +17V

GND ..... –0.3V to (V+) +0.3V

V_{IN}, V_{COM}, V_{NO} (Note 1) ..... (V–)–2V to (V+) +2V
or 30mA, whichever occurs first

Current (any terminal) 30mA

Peak Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle) 100mA

ESD per method 3015.7 ..... >2000V

Thermal Information

Continuous Power Dissipation

Plastic DIP (derate 10.5mW/°C above +70°C) 800mW

Narrow SO and QSOP
(derate 8.7mW/°C above +70°C) 650mW

Storage Temperature ..... –65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Operating Temperature Ranges
PS458_C ..... 0°C to +70°C
PS458_E ..... –40°C to +85°C

Note 1: Signals on NO, COM, or logic inputs exceeding V+ or V– are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Pin Description

Pin			Name	Function
PS4581	PS4582	PS4583		
1,2,4,5,12 13,14,15	–	–	NO0-NO7	Analog Switch Inputs 0-7.
3	–	–	COM	Analog Switch Common Output.
–	11,12,14,15	–	NO0A, NO1A, NO2A, NO3A	Analog Switch Inputs 0-3.
–	13 (COMA)	14 (COMC)	COM	Analog Switch Common Output.
–	–	13	NOC	Analog Switch Normally Open Input.
–	–	12	NCC	Analog Switch Normally Closed Input.
–	–	1	NOB	Analog Switch Normally Open Input.
–	–	2	NCB	Analog Switch "Y" Normally Closed Input.
6	6	6	INH	Digital Enable Input. Normally connect to GND. Can be driven to logic high to set all switches off.
7	7	7	V	Negative Analog Supply-Voltage Input. Connect to GND for single-supply operation.
8	8	8	GND	Ground Connect to digital ground. (Analog signals have no ground reference; they are limited to V_{CC} and V_{EE}.
11	10	11	ADDC/ADDB/ADDC	Digital Address Input (LSB).
10	9	10	ADDB/ADDA/ADDB	Digital Address Input.
9	–	9	ADDA/–/ADDA	Digital Address "C" Input.
–	1,5,2,4	–	NO0B, NO2B, NO1B, NO3B	Analog Switch Inputs 0-3
–			–/COMB/COMB	Analog Switch Output
–			NCA	Analog Switch Normally Closed Input.
–			NOA	Analog Switch Normally Open Input.
–			COMA	Analog Switch Output
16	16	16	V_{CC}	Positive Analog and Digital Supply Voltage Input.

Note: Input and output pins are identical and interchangeable. Any may be considered an inutor output; signals pass equally well in both directions.

Electrical Specifications - Dual Supplies

($V\pm = \pm 5V \pm 10\%$, GND = 0V, $V_{AH} = V_{IH} = 2.4V$, $V_{AL} = V_{IL} = 0.8V$)

Parameter	Symbol	Conditions		Temp. (°C)	Min(2)	Typ(1)	Max(2)	Units
Analog Switch								
Analog Signal Range (3)	V_{ANALOG}			Full	V–		V+	V
On Resistance	R_{ON}	V+ = 4.5V, V– = –4.5.V, V_{COM} = +3.5V, I_{NO} = 1mA		25		50	80	Ω
				Full			100	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V_{COM} = ±3.5V, I_{NO} = 1mA, V+ = 4.5V, V– = 4.5V		25		1	4	Ω
				Full			6	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V+ = 5V, V– = –5V, I_{NO} = 1mA, V_{COM} = ±3V, 0V		25		4	10	Ω
				Full			12	
NO Off LeakageCurrent(6)	$I_{NO(OFF)}$	V+ = 5.5V, V– = –5.5V, V_{COM} = ± 4.5V, V_{NO} = ∓4.5V		25	–1.0		1.0	nA
				Full	–10		10	
COM-Off Leakage Current(6)	$I_{COM(OFF)}$	V+ = 5.5V, V– = –5.5V, V_{COM} = ± 4.5V, V_{NO} = ∓4.5V	PS4581	25	–2.0		2.0	nA
				Full	–100		100	
			PS4582 PS4583	25	–1.0		1.0	
				Full	–50		50	
COM On Leakage Current(6)	$I_{COM(ON)}$	V+ = 5.5V, V– = –5.5V, V_{COM} = ± 4.5V	PS4581	25	–2.0		2.0	nA
				Full	–100		100	
			PS4582 PS4583	25	–1.0		1.0	
				Full	–50		50	
Logic Input								
Logic High Input Voltage	V_{AH}, V_{IH}			Full	2.4			V
Logic Low Input Voltage	V_{AL}, V_{IL}			Full			0.8	V
Input Current with Input Voltage High or Low	I_{IH}, I_{IL}	$V_A = V_I$ = V+, 0V		Full	–1.0		1.0	µA

Electrical Specifications - Dual Supplies (continued)

($V\pm = \pm 5V \pm 10\%$, GND = 0V, $V_{AH} = V_{IH} = 2.4V$, $V_{AL} = V_{IL} = 0.8V$)

Parameter	Symbol	Conditions		Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Dynamic								
Transition Time	t_{TRANS}	$V_{NO} \pm 3V = R_L = 300\Omega$, $C_L = 35pF$, Fig. 1		25		60	200	ns
Break-Before-Make Time Delay	t_{OPEN}	$V_{NO} = 3V$, $R_L = 300\Omega$, $C_L = 35pF$, Fig. 3		25	4	10		ns
Turn-On Time	t_{ON}	$V_{NO} = 3V$, $R_L = 300\Omega$, $C_L = 35pF$, Fig. 2		25		64	200	ns
				Full			200	
Turn-Off Time	t_{OFF}	$V_{NO} = 3V$, $R_L = 300\Omega$, $C_L = 35pF$, Fig. 2		25		40	100	ns
				Full			150	
Charge Injection(3)	Q	$C_L = 1nF$, $V_S = 0V$, $R_S = 0$ ohm,		25		0.5	5	pC
Off Isolation(7)	OIRR	$C_L = 15pF$, $V_{INH} = 5V$, $R_L = 50\Omega$ f = 1 MHz, $V_{NO} = 1V_{RMS}$		25		–73		dB
Crosstalk (PS4582)	X_{TALK}	$C_L = 15pF$, $R_L = 50\Omega$, f = 1 MHz, Figure 6, $V_{NO} = 1V_{RMS}$		25		–96		dB
Crosstalk (PS4583)	X_{TALK}	$C_L = 15pF$, $R_L = 50\Omega$, f = 1 MHz, Figure 6, $V_{NO} = 1V_{RMS}$		25		–73		dB
Logic Input Capacitance	C_{IN}	f = 1MHz		25		4		pF
NO Off Capacitance	$C_{NO (OFF)}$	f = 1MHz, $V_{NO} = 0V$		25		4		pF
COM Off Capacitance	$C_{COM (OFF)}$	f = 1MHz, $V_{COM} = 0V$	PS4581	25		78		pF
			PS4582	25		10		
			PS4583	25		6		
COM On Capacitance	$C_{COM (ON)}$	f = 1MHz, $V_{COM} = 0V$	PS4581	25		25		pF
			PS4582	25		17		
			PS4583	25		12.5		
Supply								
Power-Supply Range				Full	±2.0		±8	V
Positive Supply Current	I+, I–	$V_{INH} = V_A$ = 0V or V+, V+ = 5.5V, V- = –5.5V		25	–1		1	µA
				Full	–10		10	

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}max - R_{ON}min$
5. Flatness is defined as the difference between the maximum and minimum values of on-resistance measured.
6. Leakage parameters guaranteed by design.
7. Off Isolation = $20\log_{10} V_{COM} / V_{NO}$. See Figure 5.

Electrical Characteristics - Single 5V Supply

(V+ = +5V ±10%, V– = 0V, GND = 0V, $V_{AH} = V_{IH} = 2.4V$, $V_{AL} = V_{IL} = 0.8V$)

Parameter	Symbol	Conditions		Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Switch								
Analog Signal Range(3)	V_{ANALOG}			Full	V–		V+	V
On Resistance	R_{ON}	V+ = 4.5V, I_{NO} = 1mA, V_{COM} = 3.5V		25		90	150	Ω
				Full			200	
ON Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 4.5V, V_{COM} = 3.5V, I_{NO} = 1mA		25		2	8	Ω
				Full			10	
NO-Off Leakage Current(6)	$I_{NO (OFF)}$	V+ = 5.5V, V_{NO} = 0V, V_{COM} = 1V/4.5V, V_{NO} = 4.5V/1V		25	–1.0		1.0	nA
				Full	–10		10	
COM-Off Leakage Current(6)	$I_{COM (OFF)}$	V+ = 5.5V, V_{NO} = 4.5V/1V, V_{COM} = 1V/4.5V	PS4581	25	–2		2	nA
				Full	–100		100	
			PS4582 PS4583	25	–1		1	
				Full	–50		50	
COM-On Leakage Current(6)	$I_{COM (ON)}$	V+ = 5.5V, V_{COM} = 4.5V/1V	PS4581	25	–2		2	nA
				Full	–100		100	
			PS4582 PS4583	25	–1		1	
				Full	–50		50	
Digital Logic Input								
Logic High Input Voltage	V_{AH}, V_{IH}			Full	2.4			V
Logic Low Input Voltage	V_{AL}, V_{IL}			Full			0.8	V
Input Current with Input Voltage High or Low	I_{IH}, I_{IL}	$V_A = V_I$ = V +, 0V		Full	–1		1	µA
Supply								
Supply Current	I+, I–	V+ = 5.5V, $V_A = V_I$ = 0V or V+		25	–1.0		1.0	µA
				Full	–10		10	
Dynamic								
Turn-OnTime	t_{ON}	V_{NO} = 3V, R_L = 300Ω, C_L =35pF, Figure 2		25			200	ns
				Full			250	
Turn-Off Time	t_{OFF}	V_{NO} = 3V, R_L = 300Ω, C_L =35pF, Figure 2		25		40	100	ns
				Full			150	
Transition Times	t_{TRANS}	V_{NO} = 3V, R_L = 300Ω, C_L =35pF, Figure 1		25		80	200	ns
				Full			250	
Break-Before-Make Interval	t_{OPEN}	V_{NO} = 3V, R_L = 300Ω, C_L =35pF, Figure 3		25	10	30		ns
Charge Injection (3)	Q	C_L = 1nF, V_S = 0V, R_S = 0ohm		25			5	pC

Electrical Characteristics - Single 3V Supply

(V+ = +2.7V to 3.6V, V– = 0V, GND = 0V, $V_{AH} = V_{IH} = 2.0V$, $V_{AL} = V_{IH} = 0.5V$)

Parameter	Symbol	Conditions		Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Switch								
Analog Signal Range(3)	V_{ANALOG}			Full	0V		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 1.5V, I_{NO} = 0.1mA, V+ = 2.7V		25			450	Ω
				Full			550	
No-Off Leakage	$I_{NO(OFF)}$	V_{NO} = 1V, 3V, V_{COM} = 3V, 1V, V+ = 3.6V		25	–1.0		1.0	nA
				Full	–10		10	
COM-Off Leakage Current(8)	$I_{COM(OFF)}$	V_{CC} = 3.6V, V_{NO} = 1V, 3V V_{COM} = 3V, 1V	PS4581	25	–2		2	nA
				Full	–100		100	
			PS4582 PS4583	25	–1		1	
				Full	–50		50	
COM-On Leakage Current(8)	$I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 3V, 1V	PS4581	25	–2		2	nA
				Full	–100		100	
			PS4582 PS4583	25	–1		1	
				Full	–50		50	
Digital Logic Input								
Logic High Input Voltage	V_{AL}, V_{IH}			Full	2.0			V
Logic Low Input Voltage	V_{AL}, V_{IL}			Full			0.5	V
Input Current with Input Voltage High or Low	I_{IH}, I_{IL}			Full	–1		1	µA
Dynamic (Guaranteed by Design)								
Turn-On Time	t_{ON}	V_{NO} = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 2		25			200	ns
				Full			250	
Turn-Off Time	t_{OFF}	V_{NO} = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 2		25		40	100	ns
				Full			150	
Transition Times	t_{TRANS}	V_{NO} = 1.5/0V, R_L = 300Ω, C_L = 35pF, Figure 1		25		80	200	ns
				Full			250	
Break-Before-Make Interval	t_{OPEN}	V_{NO} = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 3		25	10	30		ns
Charge Injection(3)	Q	C_L = 1nF, V_S = 0V, R_S = 0Ω		Full			5	pC
Supply								
Supply Current	I+, I–	V_{CC} = 3.6V, $V_A = V_I$ = 0V or V+		25	–1.0		1.0	µA
				Full	–10		10	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}max - R_{ON}min$
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are guaranteed by design.
7. Off isolation = $20\log V_{COM}/V_{NO}$, see Figure 5.

Test Circuits/Timing Diagrams

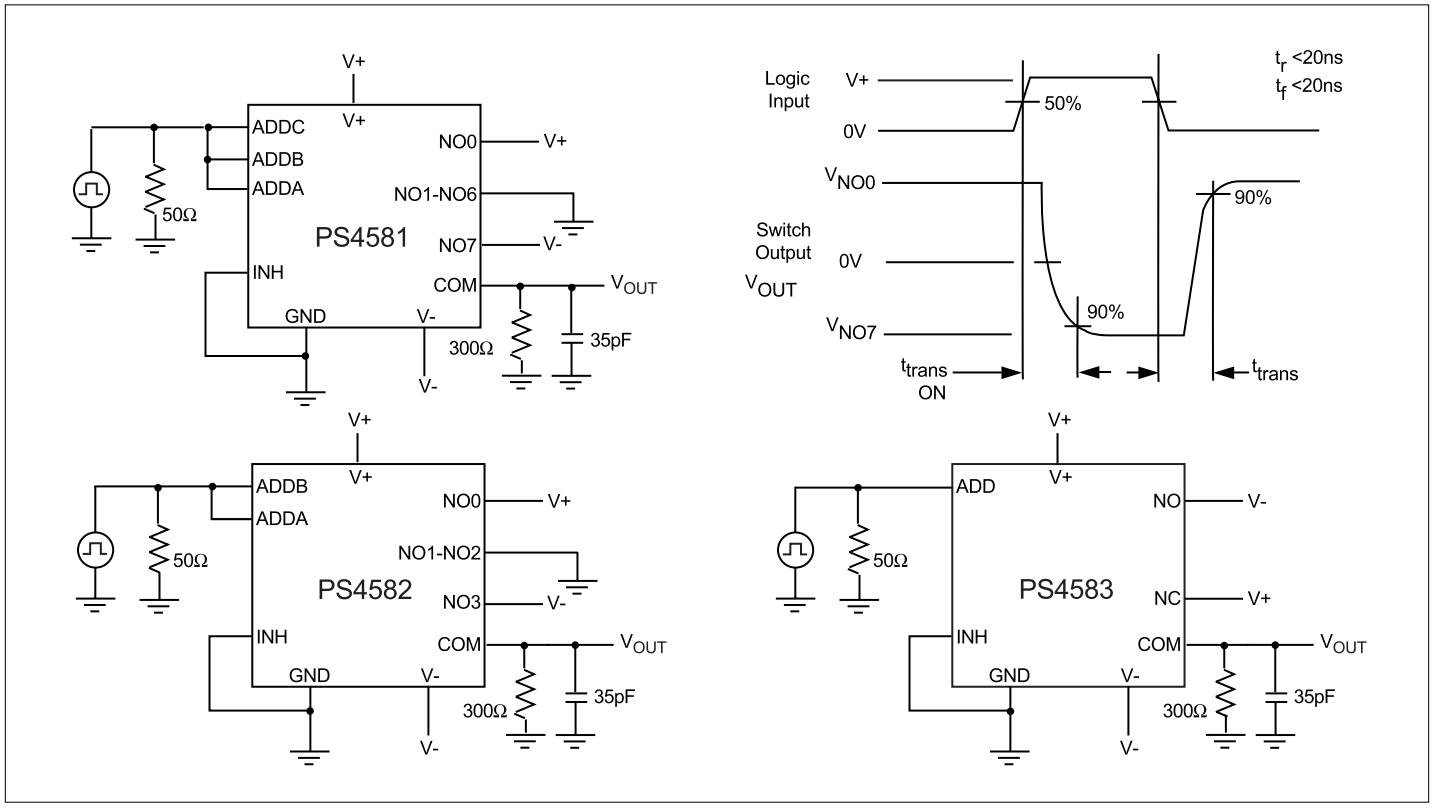


Figure 1. Transition Times

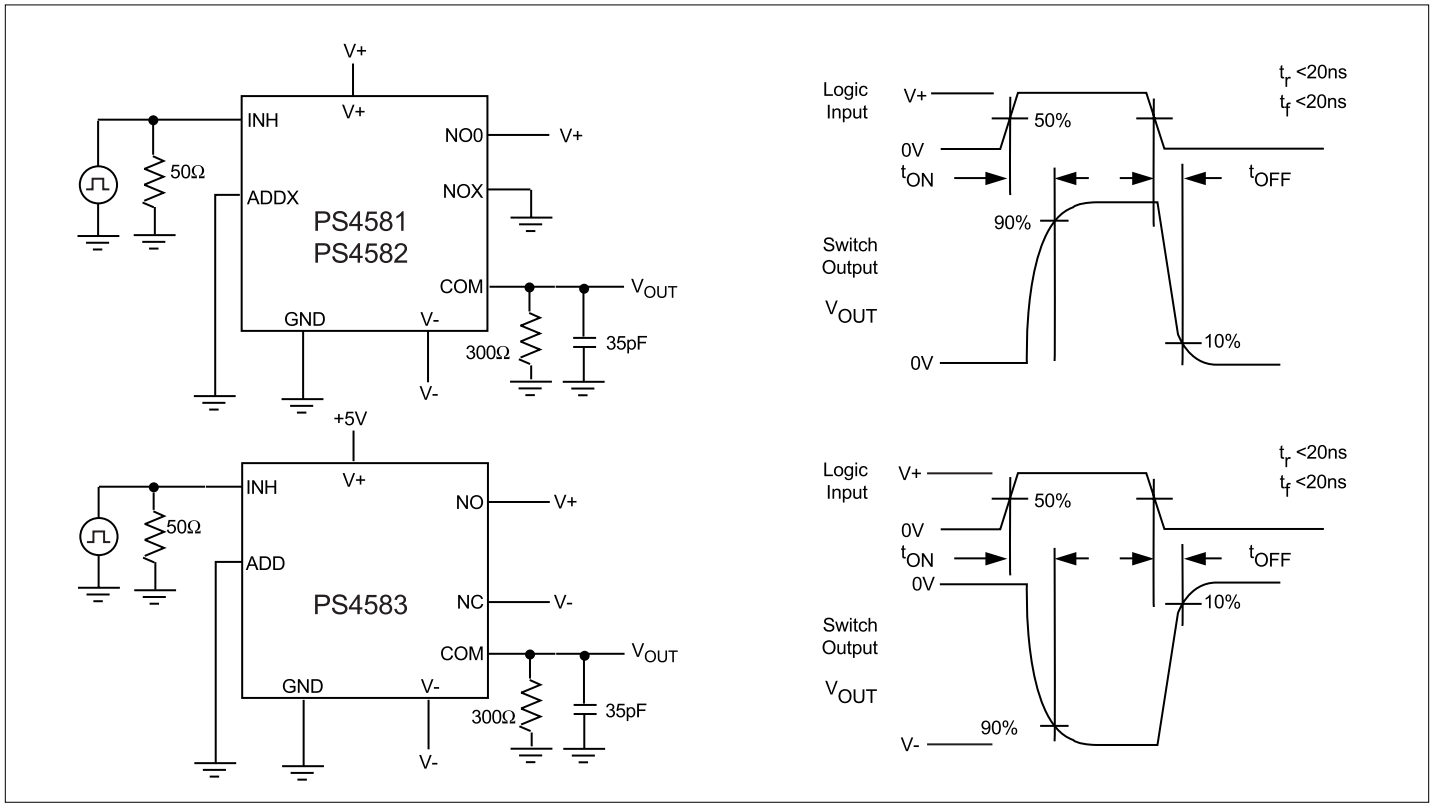


Figure 2. Switching Times

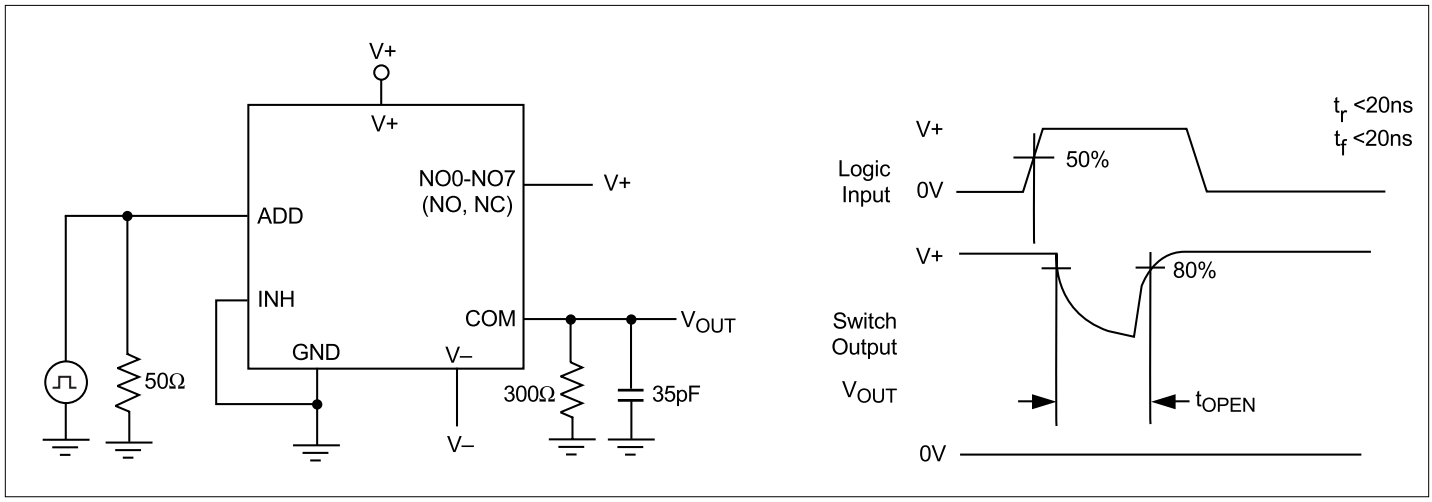


Figure 3. Break-Before-Make Interval

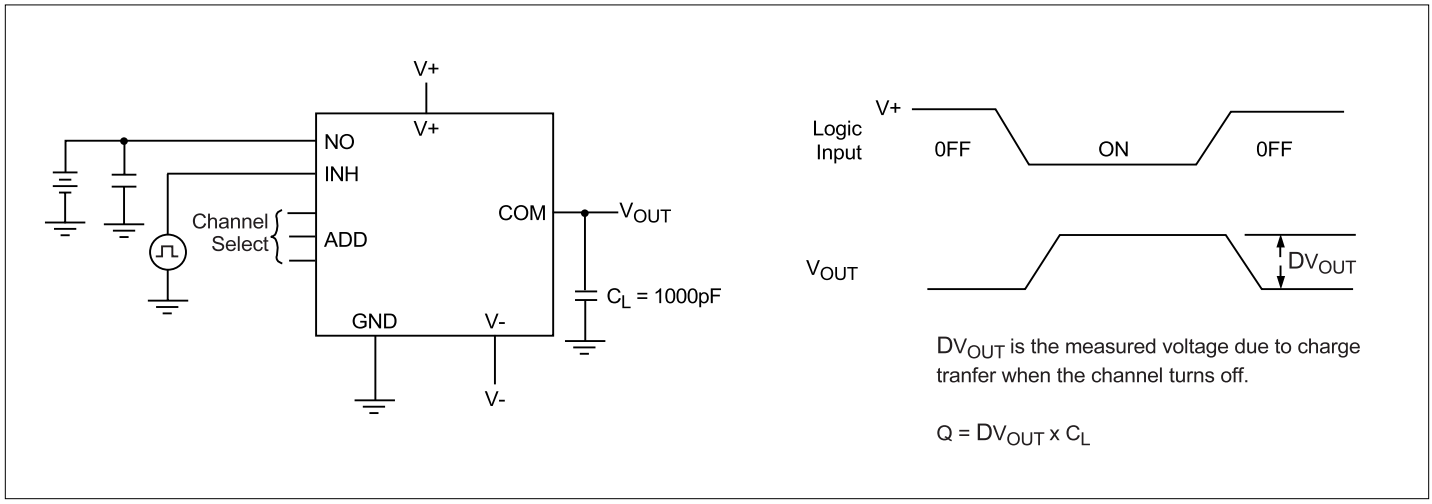


Figure 4. Charge Injection

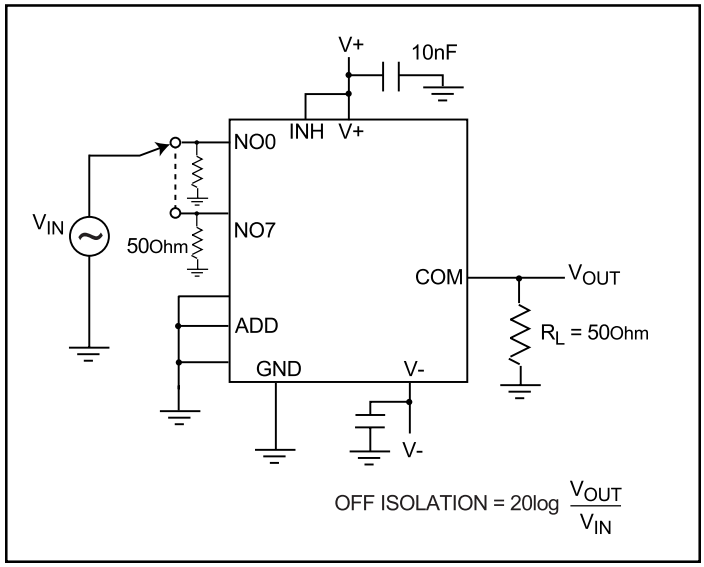


Figure 5. Off Isolation

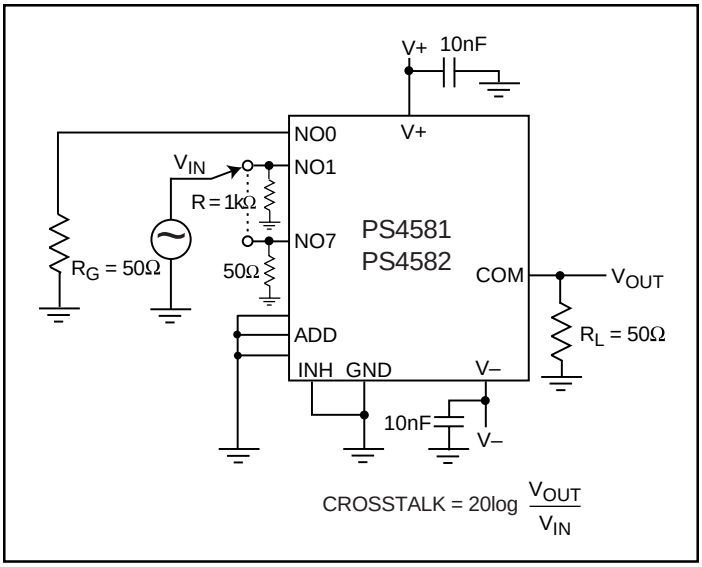


Figure 6. Crosstalk

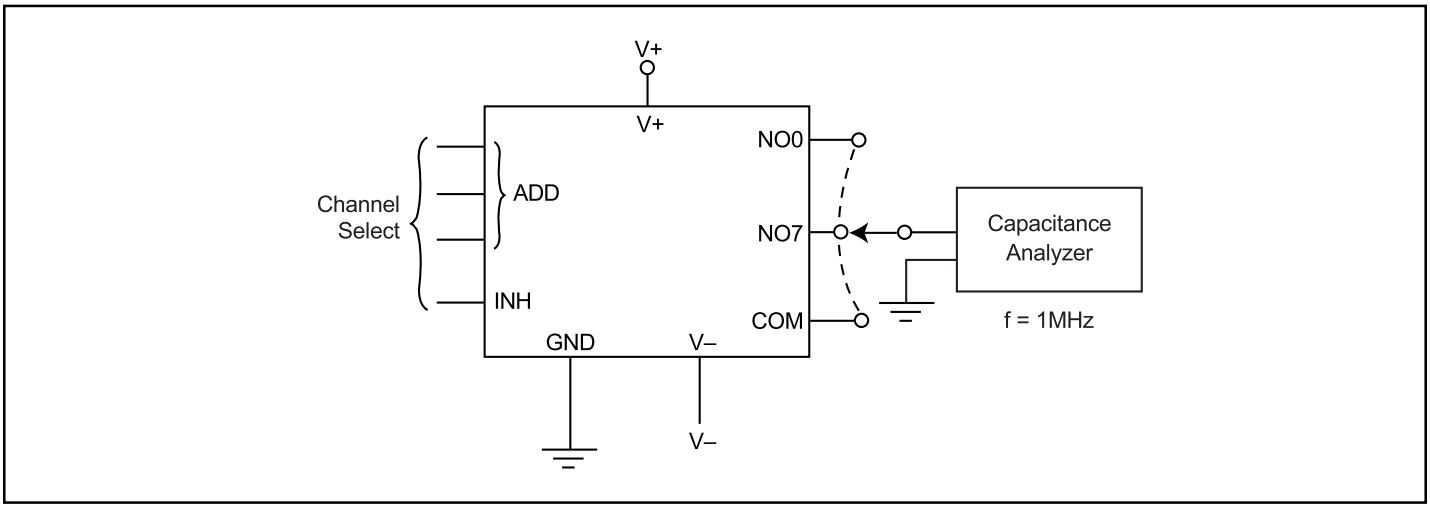


Figure 7. NO/COM Capacitance

Ordering Information

Part Number	Temperature	Package
PS4581CPE	0ºC to +70ºC	PDIP-16
PS4581CSE	0ºC to +70ºC	Narrow SOIC-16
PS4581CEE	0ºC to +70ºC	QSOP-16
PS4581EPE	– 40ºC to +85ºC	PDIP-16
PS4581ESE	– 40ºC to +85ºC	Narrow SOIC-16
PS4581EEE	– 40ºC to +85ºC	QSOP-16
PS4582CPE	0ºC to +70ºC	PDIP-16
PS4582CSE	0ºC to +70ºC	Narrow SOIC-16
PS4582CEE	0ºC to +70ºC	QSOP-16

Part Number	Temperature	Package
PS4582EPE	– 40ºC to +85ºC	PDIP-16
PS4582ESE	– 40ºC to +85ºC	Narrow SOIC-16
PS4582EEE	– 40ºC to +85ºC	QSOP-16
PS4583CPE	0ºC to +70ºC	PDIP-16
PS4583CSE	0ºC to +70ºC	Narrow SOIC-16
PS4583CEE	0ºC to +70ºC	QSOP-16
PS4583EPE	– 40ºC to +85ºC	PDIP-16
PS4583ESE	– 40ºC to +85ºC	Narrow SOIC-16
PS4583EEE	– 40ºC to +85ºC	QSOP-16