19-0051; Rev 0; 6/92

MAXIM

Low Charge-Injection, CMOS, TTL-Compatible Analog Switches

1.0 SCOPE

1.1 This specification covers the detail requirements for four CMOS switches with two switch configurations (SPST and DPST). These circuits are processed in accordance with MIL-STD-883 and are fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	IH5048M(X)/883B
-2	IH5049M(X)/883B
-3	IH5050M(X)/883B
-4	IH5051M(X)/883B

1.3 Package

(X)	Package	Description
JE	J-16	16-Pin Ceramic Dual-In-Line Package (CERDIP)
LP	L-20	20-Pin Ceramic Leadless Chip Carrier (LCC)

Note: See *Package Information* section for package drawing and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V+ to V- 44V
V+ to V_D 30V
V_D to V- 30V
V_D to V_S .... ±22V
V_L to V- 33V
V_L to V_{IN} 30V
V_L 20V
V_{IN} 20V
Current, Any Terminal 30mA
Power Dissipation (Tj = +150°C)
  up to +70°C 800mW
  derate above +70°C .... 10mW/°C
Operating Temperature Range .... -55°C to +125°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10 sec) .... +300°C

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1.5 Thermal Resistance Θ_{JC} = 50°C/W
Θ_{JA} = 100°C/W

2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Input Logic Current High	I_{INH}	V_{IN} = 2.4V	All	1, 3		±1	µA
				2		±10	
Input Logic Current Low	I_{INL}	V_{IN} = 0.8V	All	1, 3		±1	µA
				2		±10	
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -10mA, V_{ANALOG} = ±10V	All	1, 3		40	Ω
				2		60	
Switch-Off Leakage Current	$I_{D(OFF)}$	V_{ANALOG} = ±10V	All	1		±1.0	nA
				2		100	
	$I_{S(OFF)}$			1		±1.0	
				2		100	
Switch-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = ±10V	All	1		±2	nA
				2		200	
Positive Power-Supply Quiescent Current	I+		All	1, 3		1	µA
				2		10	
Negative Power-Supply Quiescent Current	I-		All	1, 3		1	µA
				2		10	
+5V Power-Supply Quiescent Current	I_L		All	1, 3		1	µA
				2		10	
GND-Supply Quiescent Current	I_{GND}		All	1, 3		1	µA
				2		10	
Switch-On Time (Note 2)	t_{ON}	Figure 1	All	9		500	ns
				10, 11		750	
Switch-Off Time (Note 2)	t_{OFF}	Figure 1	All	9		250	ns
				10, 11		500	

Note 1: V+ = 15V, V- = -15V, V_L = +5V, unless otherwise noted.
Note 2: Some channels are turned off by high (1) logic inputs and other channels by low (0) inputs; however, 0.8V and 2.4V describe the minimum range for proper switching. Refer to logic diagrams for logical input value for on or off states.

3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Interim and final electrical test requirements shall be as specified in Table 2.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 2.
(2) Selected subgroups in Table 1, Method 5005 of MIL-STD-883 shall be omitted.

3.4 Groups C and D inspections:
a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test (Method 1005 of MIL-STD-883):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,* 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 9, 10,** 11**
Groups C and D End-Point Electrical Parameters (Method 5005)	1

* PDA applies to Subgroup 1 only.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table 1.

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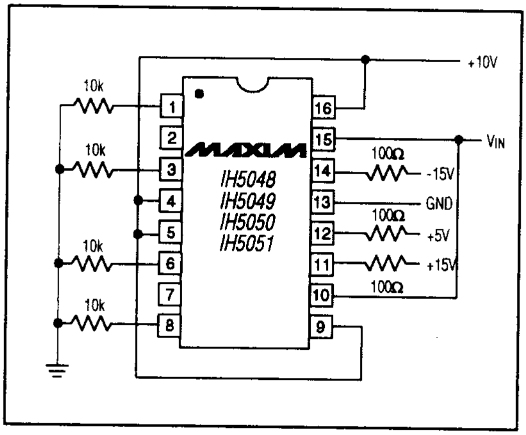
4.0 Life Test/Burn-In Circuit



4.1 Timing Diagram/Test Circuit

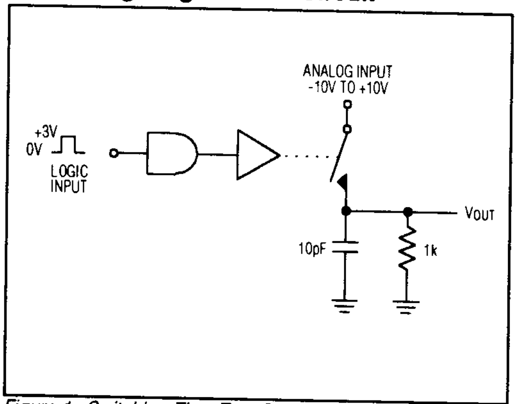
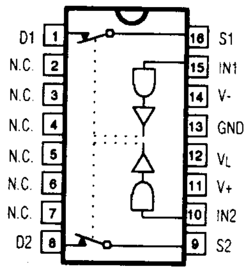


Figure 1. Switching-Time Test Circuit

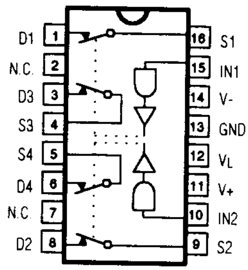
4.2 Pin Configurations/Functional Diagrams

TOP VIEW

LOGIC	SWITCH
0	OFF
1	ON



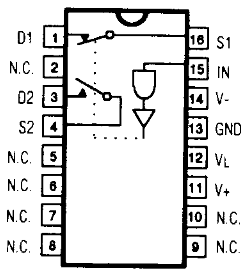
IH5048 - DUAL SPST



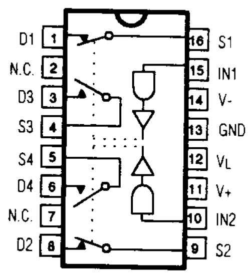
IH5049 - DUAL DPST

LOGIC	SWITCH
0	OFF
1	ON

LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF



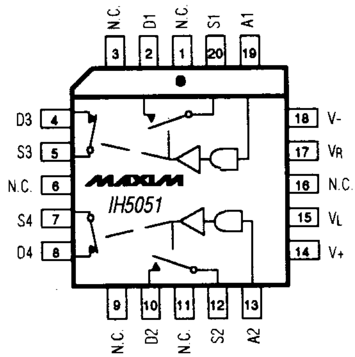
IH5050 - SPDT



IH5051 - DUAL SPDT

LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

4.2 Pin Configurations/Functional Diagrams (continued)



20-PIN LCC