

## 74F675A

### 16-Bit Serial-In, Serial/Parallel-Out Shift Register

#### General Description

The 'F675A contains a 16-bit serial in/serial out shift register and a 16-bit parallel out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

#### Features

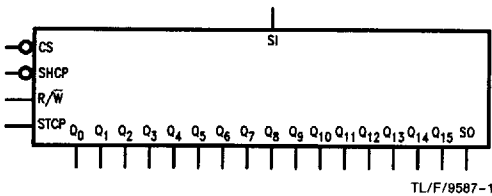
- Serial-to-parallel converter
- 16-Bit serial I/O shift register
- 16-Bit parallel out storage register
- Recirculating parallel transfer
- Expandable for longer words
- Slim 24 lead package
- 'F675A version prevents false clocking through  $\overline{CS}$  or R/ $\overline{W}$  inputs

**Ordering Code:** See Section 11

Commercial	Package Number	Package Description
74F675ASPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
74F675APC	N24A	24-Lead (0.600" Wide) Molded Dual-In-Line
74F675ASC (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC

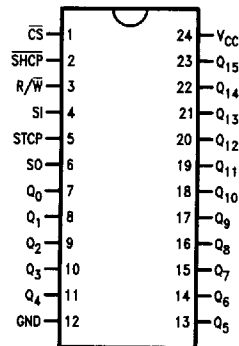
Note 1: Devices also available in 13" reel. Use suffix = SCX.

#### Logic Symbols



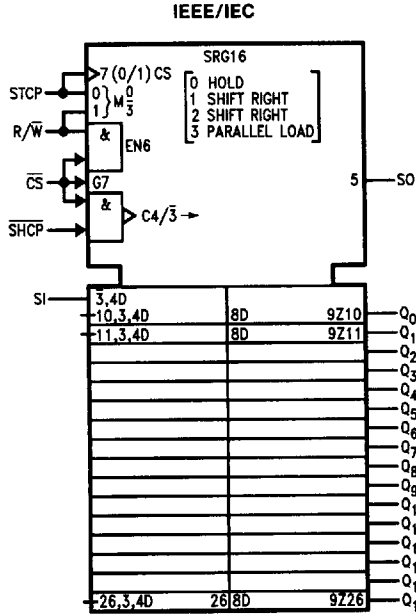
#### Connection Diagram

Pin Assignment  
for DIP and SOIC



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Logic Symbols (Continued)



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
SI	Serial Data Input	1.0/1.0	20 μA/ -0.6 mA
CS	Chip Select Input (Active LOW)	1.0/1.0	20 μA/ -0.6 mA
SHCP	Shift Clock Pulse Input (Active Falling Edge)	1.0/1.0	20 μA/ -0.6 mA
STCP	Store Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/ -0.6 mA
R/W	Read/Write Input	1.0/1.0	20 μA/ -0.6 mA
SO	Serial Data Output	50/33.3	-1 mA/20 mA
Q <sub>0</sub> -Q <sub>15</sub>	Parallel Data Outputs	50/33.3	-1 mA/20 mA

Functional Description

The 16-Bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select (CS), Read/Write (R/W) and Store Clock Pulse (STCP) input. State changes are indicated by the falling edge of the Shift Clock Pulse (SHCP). In the Shift Right mode, data enters D<sub>0</sub> from the Serial Input (SI) pin and exits from Q<sub>15</sub> via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either CS or R/W is HIGH. With CS and R/W both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register, SHCP should be in the LOW state during a LOW-to-HIGH transition of CS. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of CS if R/W is LOW, and should also be LOW during a HIGH-to-LOW transition of R/W if CS is LOW.

Shift Register Operations Table

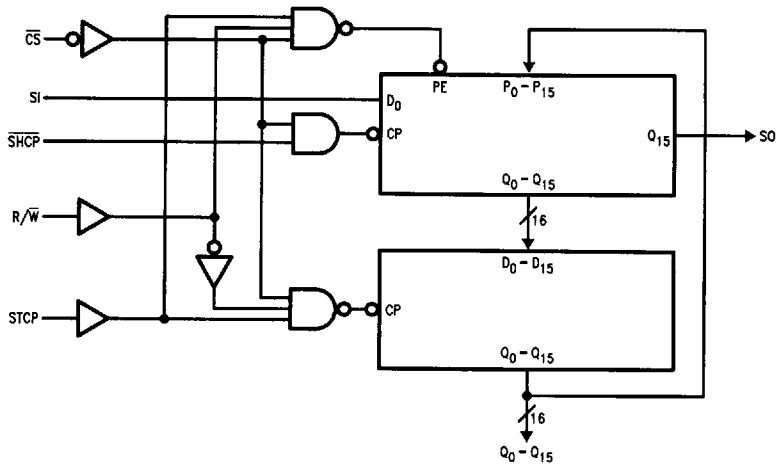
Control Inputs				Operating Mode
CS	R/W	SHCP	STCP	
H	X	X	X	Hold
L	L	~	X	Shift Right
L	H	~	L	Shift Right
L	H	~	H	Parallel Load, No Shifting

Storage Register Operations Table

Inputs			Operating Mode
CS	R/W	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	~	Parallel Load

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ~ = LOW-to-HIGH Transition  
 ~ = HIGH-to-LOW Transition

# Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Commercial	

**DC Electrical Characteristics**

Symbol	Parameter	74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	74F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				
V <sub>OL</sub>	Output LOW Voltage	74F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	74F		5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	74F		50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		106	160	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		106	160	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	100	130		85		MHz	2-1
t <sub>PLH</sub>	Propagation Delay	3.0	8.0	10.5	2.5	12.0	ns	2-3
t <sub>PHL</sub>	STCP to Q <sub>n</sub>	3.0	10.5	13.5	2.5	15.0		
t <sub>PLH</sub>	Propagation Delay	4.0	7.0	9.5	3.5	10.5	ns	2-3
t <sub>PHL</sub>	SHCP to SO	4.5	8.0	10.5	4.0	12.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	3.5		4.0		ns	2-6
t <sub>s</sub> (L)	CS or R/W to STCP	5.5		6.5			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	0		0		ns	2-6
t <sub>h</sub> (L)	CS or R/W to STCP	0		0			
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	3.0		3.5		ns	2-6
t <sub>s</sub> (L)	SI to SHCP	3.0		3.5			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	3.0		3.5		ns	2-6
t <sub>h</sub> (L)	SI to SHCP	3.0		3.5			
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	6.5		7.5		ns	2-6
t <sub>s</sub> (L)	R/W to SHCP	9.0		10.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	0		0		ns	2-6
t <sub>h</sub> (L)	R/W to SHCP	0		0			
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	7.0		8.0		ns	2-6
t <sub>s</sub> (L)	STCP to SHCP	7.0		8.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	0		0		ns	2-6
t <sub>h</sub> (L)	STCP to SHCP	0		0			
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	3.0		3.5		ns	2-6
t <sub>s</sub> (L)	CS to SHCP	3.0		3.5			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	3.0		3.5		ns	2-6
t <sub>h</sub> (L)	CS to SHCP	3.0		3.5			
t <sub>w</sub> (H)	SHCP Pulse Width	5.0		6.0		ns	2-4
t <sub>w</sub> (L)	HIGH or LOW	5.0		6.0			
t <sub>w</sub> (H)	STCP Pulse Width	6.0		7.0		ns	2-4
t <sub>w</sub> (L)	HIGH or LOW	5.0		6.0			
t <sub>s</sub> (L)	SHCP to STCP	8.0		9.0		ns	2-6
t <sub>h</sub> (H)	SHCP to STCP	0.0		0.0		ns	2-6