T-46-07-08

National Semiconductor

54AC/74AC74 • 54ACT/74ACT74
Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:
LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- I_{CC} reduced by 50%
- Output source/sink 24 mA
- 'ACT74 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'AC74: 5962-88520
 — 'ACT74: 5962-87525

Ordering Code: See Section 8

Logic Symbols
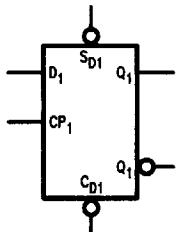
TL/F/9920–1
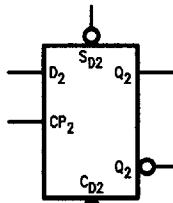
TL/F/9920–2

IEEE/IEC
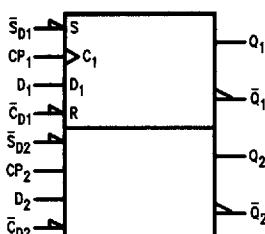
TL/F/9920–3

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Connection Diagrams

**Pin Assignment
for DIP, Flatpak and SOIC**
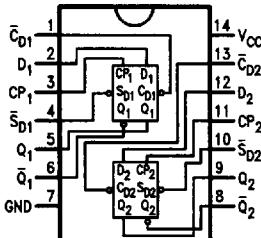
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Pin Assignment for LCC
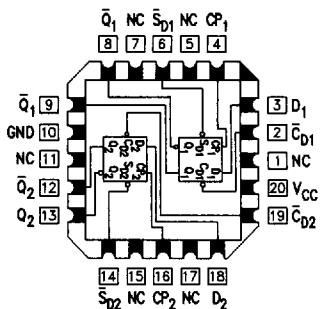
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Truth Table (Each Half)

Inputs				Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	╱	H	H	L
H	H	╱	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
╱ = LOW-to-HIGH Clock Transition
$Q_0(\bar{Q}_0)$ = Previous $Q(\bar{Q})$ before LOW-to-HIGH Transition of Clock

Logic Diagram
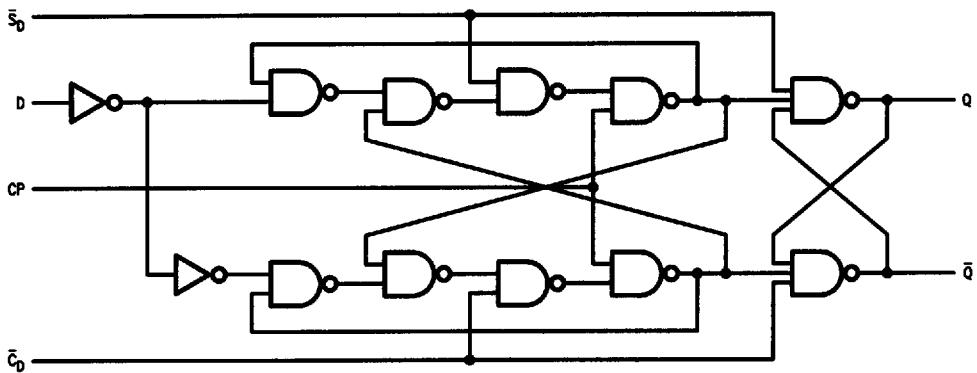
TL/F/9920-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	$-0.5V$ to $+7.0V$
DC Input Diode Current (I_{IK})	
$\quad V_I = -0.5V$	-20 mA
$\quad V_I = V_{CC} + 0.5V$	$+20$ mA
DC Input Voltage (V_I)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$\quad V_O = -0.5V$	-20 mA
$\quad V_O = V_{CC} + 0.5V$	$+20$ mA
DC Output Voltage (V_O)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	$-65°C$ to $+150°C$
Junction Temperature (T_J)	
$\quad$ CDIP	175°C
$\quad$ PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
$\quad$ 'AC	2.0V to 6.0V
$\quad$ 'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
$\quad$ 74AC/ACT	$-40°C$ to $+85°C$
$\quad$ 54AC/ACT	$-55°C$ to $+125°C$
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
$\quad$ 'AC Devices	
$\quad V_{IN}$ from 30% to 70% of V_{CC}	
$\quad V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
$\quad$ 'ACT Devices	
$\quad V_{IN}$ from 0.8V to 2.0V	
$\quad V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
				Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1		$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15	3.15	V	
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9		$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35	1.35	V	
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9		$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4	4.4	V	
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46		*$V_{IN} = V_{IL}$ or V_{IH} $\quad -12$ mA
		4.5		3.86	3.7	3.76	V	$I_{OH} \quad -24$ mA
		5.5		4.86	4.7	4.76		$\quad -24$ mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1		$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1	0.1	V	
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44		*$V_{IN} = V_{IL}$ or V_{IH} $\quad 12$ mA
		4.5		0.36	0.5	0.44	V	$I_{OL} \quad 24$ mA
		5.5		0.36	0.5	0.44		$\quad 24$ mA
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

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DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_CC (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_OLD	†Minimum Dynamic Output Current	5.5			50	75	mA	V_OLD = 1.65V Max
I_OHD		5.5			−50	−75	mA	V_OHD = 3.85V Min
I_CC	Maximum Quiescent Supply Current	5.5		2.0	40.0	20.0	μA	V_IN = V_CC or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
    I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_CC (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_IH	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_OUT = 0.1V or V_CC − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_IL	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_OUT = 0.1V or V_CC − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_OH	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_OUT = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_IN = V_IL or V_IH I_OH −24 mA
		5.5		4.86	4.70	4.76		−24 mA
V_OL	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_OUT = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_IN = V_IL or V_IH I_OL 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_IN	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_CC, GND
I_CCT	Maximum I_CC/Input	5.5	0.6		1.6	1.5	mA	V_I = V_CC − 2.1V
I_OLD	†Minimum Dynamic Output Current	5.5			50	75	mA	V_OLD = 1.65V Max
I_OHD		5.5			−50	−75	mA	V_OHD = 3.85V Min
I_CC	Maximum Quiescent Supply Current	5.5		2.0	40.0	20.0	μA	V_IN = V_CC or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	100	125		70		95		MHz	
		5.0	140	160		95		125			
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	3.5	8.0	12.0	1.0	13.0	2.5	13.0	ns	2-3, 4
		5.0	2.5	6.0	9.0	1.0	9.5	2.0	10.0		
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	4.0	10.5	12.0	1.0	14.0	3.5	13.5	ns	2-3, 4
		5.0	3.0	8.0	9.5	1.0	10.5	2.5	10.5		
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	4.5	8.0	13.5	1.0	17.5	4.0	16.0	ns	2-3, 4
		5.0	3.5	6.0	10.0	1.0	12.0	3.0	10.5		
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	3.5	8.0	14.0	1.0	13.5	3.5	14.5	ns	2-3, 4
		5.0	2.5	6.0	10.0	1.0	10.0	2.5	10.5		

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF	54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW D_n to CP_n	3.3	1.5	4.0	5.0	4.5	ns	2-7
		5.0	1.0	3.0	4.0	3.0		
t_h	Hold Time, HIGH or LOW D_n to CP_n	3.3	−2.0	0.5	0.5	0.5	ns	2-7
		5.0	−1.5	0.5	0.5	0.5		
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3	3.0	5.5	8.0	7.0	ns	2-4
		5.0	2.5	4.5	5.5	5.0		
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3	−2.5	0	0.5	0	ns	2-4, 7
		5.0	−2.0	0	0.5	0		

Note: Columns for t_s, t_h, t_w, t_{rec} are: Typ, then Guaranteed Minimum split into 74AC (+25°C), 54AC, 74AC (−40°C).

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

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AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_CC* (V)	74ACT T_A = +25°C C_L = 50 pF			54ACT T_A = −55°C to +125°C C_L = 50 pF		74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		85		125		MHz	
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	5.5	9.5	1.0	11.5	2.5	10.5	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	6.0	10.0	1.0	12.5	3.0	11.5	ns	2-3, 4
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	4.0	7.5	11.0	1.0	14.0	4.0	13.0.	ns	2-3, 4
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	3.5	6.0	10.0	1.0	12.0	3.0	11.5	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_CC* (V)	74ACT T_A = +25°C C_L = 50 pF	54ACT T_A = −55°C to +125°C C_L = 50 pF	74ACT T_A = −40°C to +85°C C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW D_n to CP_n	5.0	1.0	3.0	4.0	3.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP_n	5.0	−0.5	1.0	1.0	1.0	ns	2-7
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	7.0	6.0	ns	2-4
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	0	0.5	0	ns	2-4, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	35.0	pF	V_{CC} = 5.0V