

December 1996

Fast CMOS 1-of-8 Decoders

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- TTL Input and Output Levels
- Extremely Low Static Power
- Hysteresis on All Inputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT138TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT138ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT138CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT138TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT138ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT138CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT138TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT138ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT138CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT238TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT238ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT238CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT238TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT238ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT238CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT238TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT238ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT238CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

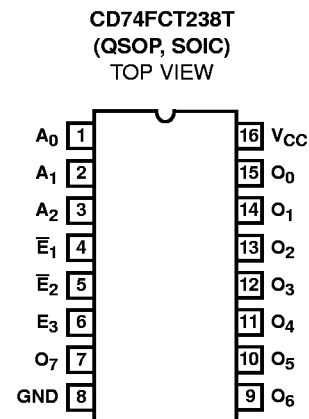
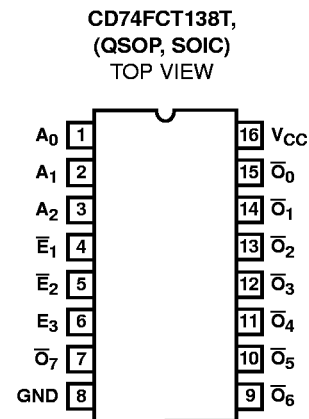
NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

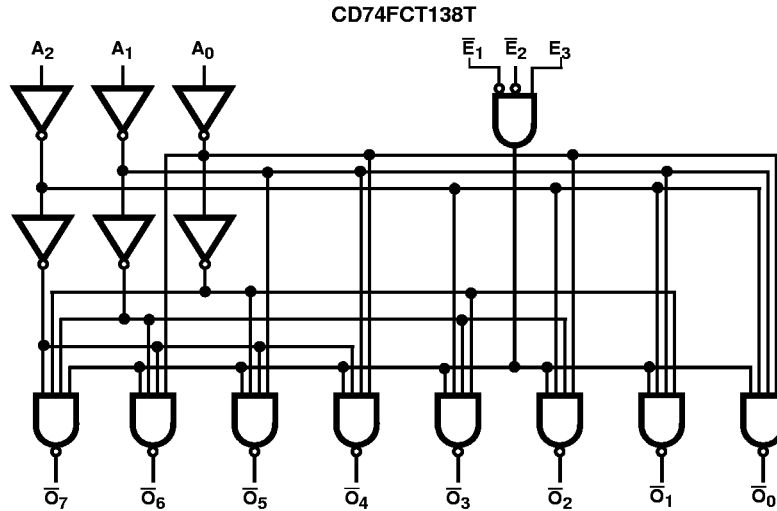
These high-speed decoders accept three binary weighted inputs (A_0, A_1, A_2) and gives eight mutually exclusive active LOW outputs (\bar{O}_0 - \bar{O}_7 : CD74FCT138T) or active HIGH outputs (O_0 - O_7 : CD74FCT238T) when enabled. These devices contain three enable inputs, two active LOW (\bar{E}_1, \bar{E}_2) and one active HIGH (E_3). On the CD74FCT138T all outputs will be HIGH and on the CD74FCT238T all outputs will be LOW, except when \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH.

Pinouts



CD74FCT138T, CD74FCT238T

Functional Block Diagram



CD74FCT138T TRUTH TABLE (NOTE 1)

INPUTS						OUTPUTS							FUNCTION	
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6		\bar{O}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H	Disable
X	H	X	X	X	X	H	H	H	H	H	H	H	H	Disable
X	X	L	X	X	X	H	H	H	H	H	H	H	H	Disable
L	L	H	L	L	L	L	H	H	H	H	H	H	H	A2-0 = 0
L	L	H	H	L	L	H	L	H	H	H	H	H	H	A2-0 = 1
L	L	H	L	H	L	H	H	L	H	H	H	H	H	A2-0 = 2
L	L	H	H	H	L	H	H	H	L	H	H	H	H	A2-0 = 3
L	L	H	L	L	H	H	H	H	H	L	H	H	H	A2-0 = 4
L	L	H	H	L	H	H	H	H	H	H	L	H	H	A2-0 = 5
L	L	H	L	H	H	H	H	H	H	H	H	L	H	A2-0 = 6
L	L	H	H	H	H	H	H	H	H	H	H	H	L	A2-0 = 7

CD74FCT238T TRUTH TABLE (NOTE 1)

INPUTS						OUTPUTS							FUNCTION	
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6		O_7
H	X	X	X	X	X	L	L	L	L	L	L	L	L	Disable
X	H	X	X	X	X	L	L	L	L	L	L	L	L	Disable
X	X	L	X	X	X	L	L	L	L	L	L	L	L	Disable
L	L	H	L	L	L	H	L	L	L	L	L	L	L	A2-0 = 0
L	L	H	H	L	L	L	H	L	L	L	L	L	L	A2-0 = 1
L	L	H	L	H	L	L	L	H	L	L	L	L	L	A2-0 = 2
L	L	H	H	H	L	L	L	L	H	L	L	L	L	A2-0 = 3
L	L	H	L	L	H	L	L	L	L	H	L	L	L	A2-0 = 4
L	L	H	H	L	H	L	L	L	L	L	H	L	L	A2-0 = 5
L	L	H	L	H	H	L	L	L	L	L	L	H	L	A2-0 = 6
L	L	H	H	H	H	L	L	L	L	L	L	L	H	A2-0 = 7

NOTE:

- 1. H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Don't Care

Pin Descriptions

PIN NAME	DESCRIPTION
CD74FCT138T PRODUCT PIN DESCRIPTION	
A ₀ -A ₂	Address Inputs
\bar{E}_1, \bar{E}_2	Enable Inputs (Active LOW)
E ₃	Enable Input (Active HIGH)
$\bar{O}_0-\bar{O}_7$	Outputs (Active LOW)
CD74FCT238T PRODUCT PIN DESCRIPTION	
A ₀ -A ₂	Address Inputs
\bar{E}_1, \bar{E}_2	Enable Inputs (Active LOW)
E ₃	Enable Input (Active HIGH)
O ₀ -O ₇	Outputs (Active HIGH)

CD74FCT138T, CD74FCT238T

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
 DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
 Supply Voltage to Ground Potential
 Inputs and V_{CC} Only -0.5V to 7.0V
 Supply Voltage to Ground Potential
 Outputs and D/O Only -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
 16 Lead SOIC (150 mil) Package 110
 16 Lead SOIC (300 mil) Package 97
 16 Lead QSOP Package 140
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS	MIN	(NOTE 4) TYP	MAX	UNITS	
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±5%							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V _{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I _{IH}	V _{CC} = Max	V _{IN} = V _{CC}	-	-	1	μA
Input LOW Current	I _{IL}	V _{CC} = Max	V _{IN} = GND	-	-	-1	μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I _{OS}	V _{CC} = Max (Note 5), V _{OUT} = GND		-60	-120	-225	mA
Power Down Disable	I _{OFF}	V _{CC} = GND, V _{OUT} = 4.5V		-	-	100	μA
Input Hysteresis	V _H			-	200	-	mV
CAPACITANCE T _A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C _{IN}	V _{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C _{OUT}	V _{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I _{CC}	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI _{CC}	V _{CC} = Max	V _{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I _{CCD}	V _{CC} = Max, Outputs Open One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	0.15	0.3	mA/ MHz
Total Power Supply Current (Note 10)	I _C	V _{CC} = Max, Outputs Open f _{cp} = 10MHz, 50% Duty Cycle Toggle $\bar{E}1$, $\bar{E}2$, or E3 One Bit toggling	V _{IN} = V _{CC} V _{IN} = GND	-	1.5	4.5 (Note 9)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	1.8	5.0 (Note 9)	mA

CD74FCT138T, CD74FCT238T

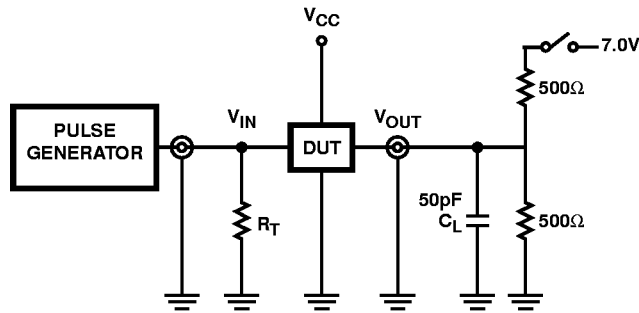
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T		AT		CT		UNIT
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
CD74FCT138T									
Propagation Delay An to $\bar{O}n$	t_{PLH} , t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	9.0	1.5	5.8	1.5	5.1	ns
Propagation Delay $\bar{E}1$ or $\bar{E}2$ to $\bar{O}n$	t_{PLH} , t_{PHL}		1.5	9.0	1.5	5.9	1.5	5.2	ns
Propagation Delay E3 to $\bar{O}n$	t_{PLH} , t_{PHL}		1.5	9.0	1.5	5.9	1.5	5.2	ns
CD74FCT238T									
Propagation Delay An to On	t_{PLH} , t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	9.0	1.5	5.8	1.5	5.0	ns
Propagation Delay $\bar{E}1$ or $\bar{E}2$ to On	t_{PLH} , t_{PHL}		1.5	8.0	1.5	5.9	1.5	5.0	ns
Propagation Delay E3 to On	t_{PLH} , t_{PHL}		1.5	8.0	1.5	5.9	1.5	5.0	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at $V_{CC} = 5.0V$, $25^\circ C$ ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_O N_O)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_O = Output Frequency
 N_O = Number of Outputs at f_O
All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ} ; t_{PZL}	Closed
t_{PHZ} ; t_{PZH} ; t_{PLH} ; t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

13. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $Z_{OUT} \leq$ 50 Ω ;
 t_f , $t_r \leq$ 2.5ns.

FIGURE 1. TEST CIRCUIT

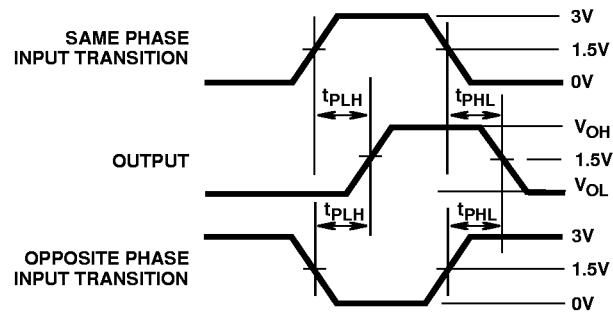


FIGURE 2. PROPAGATION DELAY