

54F/74F377

Octal D Flip-Flop with Clock Enable

General Description

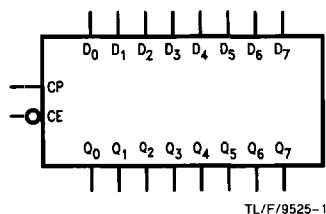
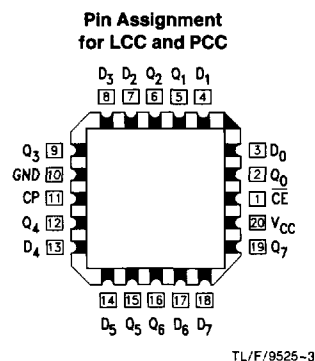
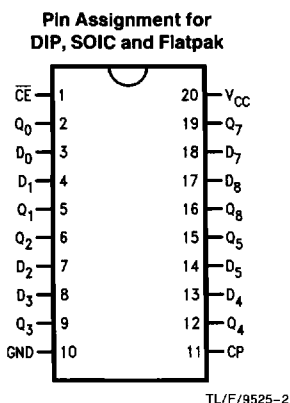
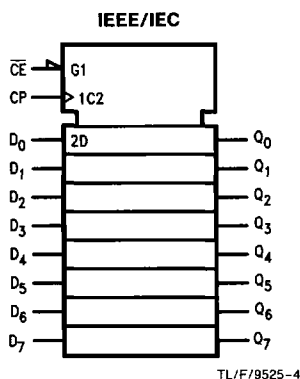
The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'F273 for master reset version
- See 'F373 for transparent latch version
- See 'F374 for TRI-STATE[®] version

Logic Symbols

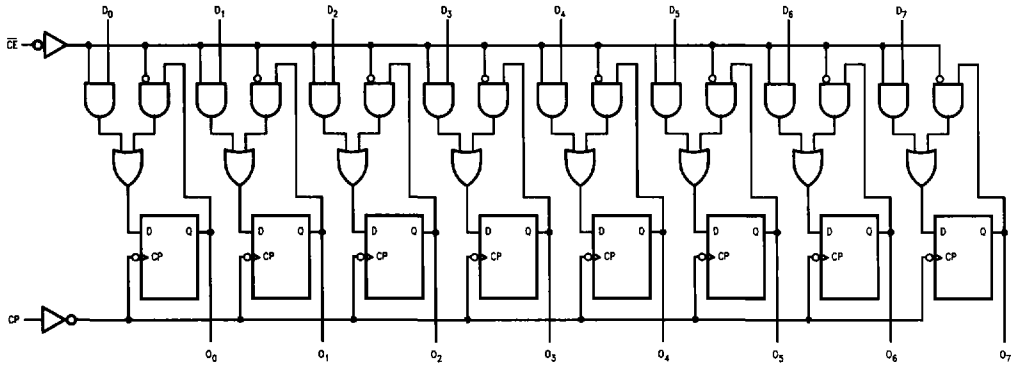


Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	\overline{CE}	D_n	Q_n
Load "1"	↗	L	h	H
Load "0"	↘	L	L	L
Hold (Do Nothing)	↗	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
 h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
 L = LOW Voltage Level
 l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
 X = Immaterial
 ↗ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/9525-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.