CD54HC564/3A
CD54HCT564/3A

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay Clock to Output	t_{PLH} t_{PHL}	2	—	165	—	—	—	250	—	—	ns
		4.5	—	33•	—	35•	—	50•	—	53•	
		6	—	28	—	—	—	43	—	—	
Propagation Delay Output Disable to Q	t_{PLZ} t_{PHZ}	2	—	135	—	—	—	205	—	—	
		4.5	—	27•	—	30•	—	41•	—	45•	
		6	—	23	—	—	—	35	—	—	
Propagation Delay Output Enable to Q	t_{PZL} t_{PZH}	2	—	150	—	—	—	225	—	—	
		4.5	—	30•	—	35•	—	45•	—	53•	
		6	—	26	—	—	—	38	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	90	—	—	
		4.5	—	12	—	12	—	18	—	18	
		6	—	10	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I OPEN	GROUND	V_{CC} (6V)	STATIC BURN-IN II OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT564	12-19	1-11	20	12-19	10	1-9,11,20
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR 50 kHz**	**25 kHz**
CD54HC/HCT564	—	1,10	12-19	20	11	2-9

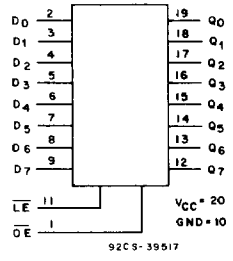
NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

Octal Transparent Latch, 3-State

CD54HC573/3A
CD54HCT573/3A

The RCA CD54HC573 and CD54HCT573 are high speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices. The CD54HCT573 is functional as well as pin compatible with the standard 54LS573.

The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the three-state outputs. When the output enable ($\overline{OE}$) is high the outputs are in the high impedance state. The latch operation is independent of the state of the output enable. The 573 and 373 are identical in function and differ only in their pinout arrangements.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 13

CD54HC573/3A
CD54HCT573/3A

Static Electrical Characteristics (Limits with black dots (•) are tested 100%) — Bus Type

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Output High (Source) Current I_{OH} Min. - TTL Load	25°C	4.5	3.98	—	—	0, 4.5	0, 4.5	-6•	—	mA
	-55°C / +125°C	4.5	3.70	—	—	0, 4.5	0, 4.5	-6•	—	
Output Low (Sink) Current I_{OL} Min. - TTL Load	25°C	4.5	0.26	—	—	0, 4.5	0, 4.5	6•	—	
	-55°C / +125°C	4.5	0.40	—	—	0, 4.5	0, 4.5	6•	—	
High Level Output Voltage V_{OH} - TTL Load	25°C	4.5	—	-6	—	1.35, 3.15	0.8, 2.0	3.98•	—	V
	-55°C / +125°C	4.5	—	-6	—	1.35, 3.15	0.8, 2.0	3.70•	—	
Low Level Output Voltage V_{OL} - TTL Load	25°C	4.5	—	6	—	1.35, 3.15	0.8, 2.0	—	0.26•	
	-55°C / +125°C	4.5	—	6	—	1.35, 3.15	0.8, 2.0	—	0.40•	
Quiescent Device Current I_{CC}	25°C	6	—	—	6, 0	—	—	—	8•	μA
	-55°C / +125°C	6	—	—	6, 0	—	—	—	160•	

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
$\overline{OE}$	1.25
Dn	0.3
$\overline{LE}$	0.65

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{CC} V	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay Data on Qn	t_{PLH} t_{PHL}	2	—	175	—	—	—	265	—	—	ns
		4.5	—	35•	—	40•	—	53•	—	60•	
		6	—	30	—	—	—	45	—	—	
$\overline{LE}$ to Qn	t_{PLH} t_{PHL}	2	—	175	—	—	—	265	—	—	
		4.5	—	35•	—	35•	—	53•	—	53•	
		6	—	30	—	—	—	45	—	—	
Output Enabling Time	t_{PZL} t_{PZH}	2	—	150	—	—	—	225	—	—	
		4.5	—	30•	—	35•	—	45•	—	53•	
		6	—	26	—	—	—	38	—	—	
Output Disabling Time	t_{PLZ} t_{PHZ}	2	—	150	—	—	—	225	—	—	
		4.5	—	30•	—	35•	—	45•	—	53•	
		6	—	26	—	—	—	38	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	90	—	—	
		4.5	—	12	—	12	—	18	—	18	
		6	—	10	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	

CD54HC573/3A
CD54HCT373/3A

Burn-In Test-Circuit Connections

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT573	12-19	1-11	20	12-19	10	1-9,11,20
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	**25 kHz**
CD54HC/HCT573	—	1,10	12-19	20	11	2-9

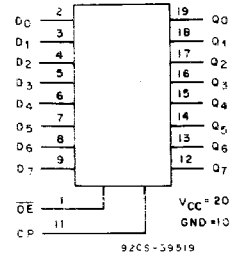
NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms
Connect pins marked (*) without using a resistor.

Octal D-Type Flip-Flop, 3-State

CD54HC574/3A
CD54HCT574/3A

5

The RCA CD54HC574 and CD54HCT574 are octal D-type flip-flops with three-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The Output Enable ($\overline{OE}$) controls the three-state outputs and is independent of the register operation. When Output Enable ($\overline{OE}$) is HIGH the outputs will be in the high impedance state. The 574 and 374 are identical in function and differ only in their pinout arrangements.



FUNCTIONAL DIAGRAM

Package Specifications
See Section 11, Fig. 13

Static Electrical Characteristics (Limits with black dots (•) are tested 100%) — Bus Type

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Output High (Source) Current I_{OH} Min. - TTL Load	25°C	4.5	3.98	—	—	0, 4.5	0, 4.5	-6•	—	mA
	-55°C / +125°C	4.5	3.70	—	—	0, 4.5	0, 4.5	-6•	—	
Output Low (Sink) Current I_{OL} Min. - TTL Load	25°C	4.5	0.26	—	—	0, 4.5	0, 4.5	6•	—	
	-55°C / +125°C	4.5	0.40	—	—	0, 4.5	0, 4.5	6•	—	
High Level Output Voltage V_{OH} - TTL Load	25°C	4.5	—	-6	—	1.35, 3.15	0.8, 2.0	3.98•	—	V
	-55°C / +125°C	4.5	—	-6	—	1.35, 3.15	0.8, 2.0	3.70•	—	
Low Level Output Voltage V_{OL} - TTL Load	25°C	4.5	—	6	—	1.35, 3.15	0.8, 2.0	—	0.26•	
	-55°C / +125°C	4.5	—	6	—	1.35, 3.15	0.8, 2.0	—	0.40•	
Quiescent Device Current I_{CC}	25°C	6	—	—	6, 0	—	—	—	8•	μA
	-55°C / +125°C	6	—	—	6, 0	—	—	—	160•	

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.