QUAD EXCLUSIVE-OR GATE WITH OPEN COLLECTOR OUTPUTS — 54/74136

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A,F

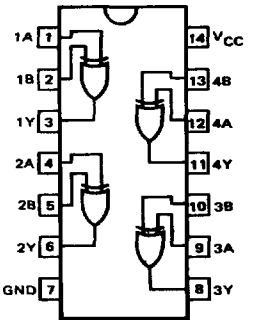
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: Y=A B=$\overline{A}B+A\overline{B}$

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15pF,		18	30	ns
t_{PHL}			R_L = 2kΩ		18	30	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					18	30	

★t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and typical waveforms shown in front of book.

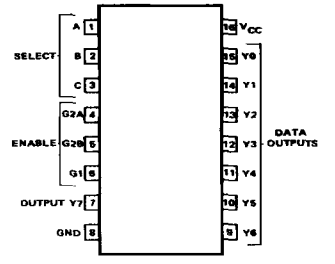
3-TO-8 LINE DECODER/DEMULTIPLEXER — 54/74138

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B,F
54S F,W 74S B,F

PIN CONFIGURATION

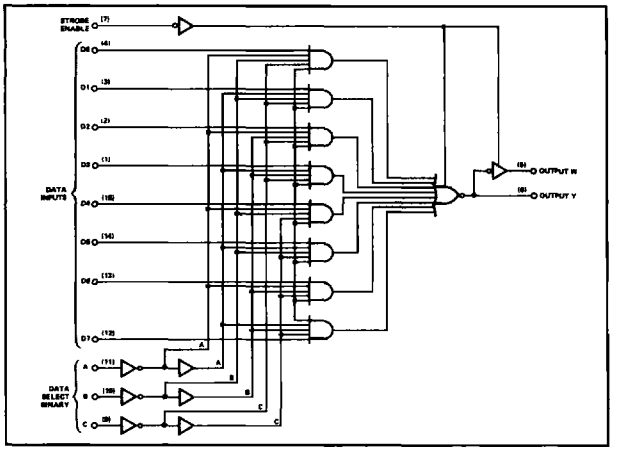
B,F,W PACKAGE



DESCRIPTION

The S54LS138 and N74LS138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications. Typical delay time through the three-level address circuitry is 22 nanoseconds. Typical power dissipation is 32 milliwatts.

BLOCK DIAGRAM



TRUTH TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

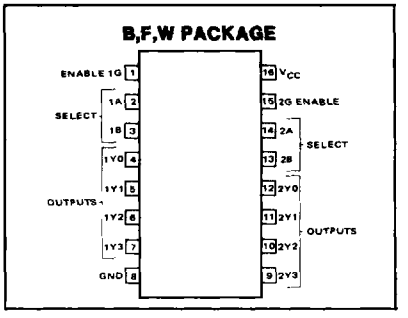
TEST CONDITIONS				54/74LS C_L=15pF R_L=2KΩ			54/74S C_L=15pF R_L=280Ω				
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	LEVELS OF DELAY	UNIT
Propagation delay time											
t_{PLH}	Low-to-high	Binary Select	Any		13	20		4.5	7	2	ns
t_{PHL}	High-to-low				27	41		7	10.5		
t_{PLH}	Low-to-high				18	27		7.5	12	3	
t_{PHL}	High-to-low				26	39		8	12		
t_{PLH}	Low-to-high	Enable	Any		12	18		5	8	2	
t_{PHL}	High-to-low				21	32		7	11		
t_{PLH}	Low-to-high				17	26		7	11	3	
t_{PHL}	High-to-low				25	38		7	11		

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B,F
54S F,W 74S B,F

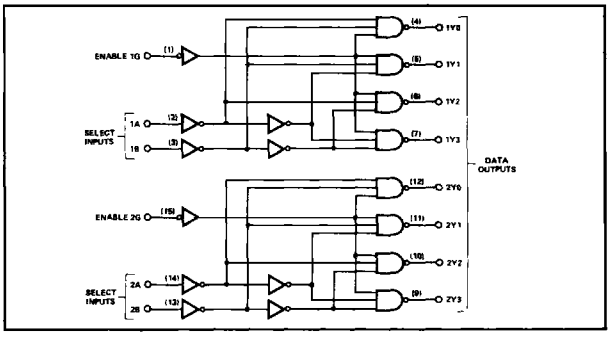
PIN CONFIGURATION



DESCRIPTION

The S54LS139 and N74LS139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. Typical total delay time is 22 nanoseconds through the three-gate-level address circuitry and power consumption is typically 34 milliwatts total.

BLOCK DIAGRAM



TRUTH TABLE (Each Decoder/Demultiplexer)

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H=high level, L=low level, X=irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74LS C_L=15pF R_L=2KΩ			54/74S C_L=15pF R_L=280Ω				
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	LEVELS OF DELAY	UNIT
Propagation delay time											
t_{PLH}	Low-to-high	Binary	Any		13	20		5	7.5	2	ns
t_{PHL}	High-to-low	Select			22	33		6.5	10		
t_{PLH}	Low-to-high				18	29		7	12	3	
t_{PHL}	High-to-low				25	38		8	12		
t_{PLH}	Low-to-high	Enable	Any		16	24		5	8	2	
t_{PHL}	High-to-low				21	32		6.5	10		

Load circuit and typical waveforms shown at the front of section.

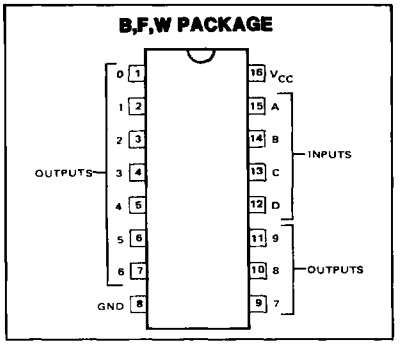
BCD-TO-DECIMAL DECODER/DRIVER 54/74145

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F
54LS F,W 74LS B,F

PIN CONFIGURATION

B,F,W PACKAGE



DESCRIPTION

This monolithic BCD-to-decimal decoder/driver consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. This decoder features high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) will sink up to 80 milliamperes of current. Each input is one standard load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 35 milliwatts.

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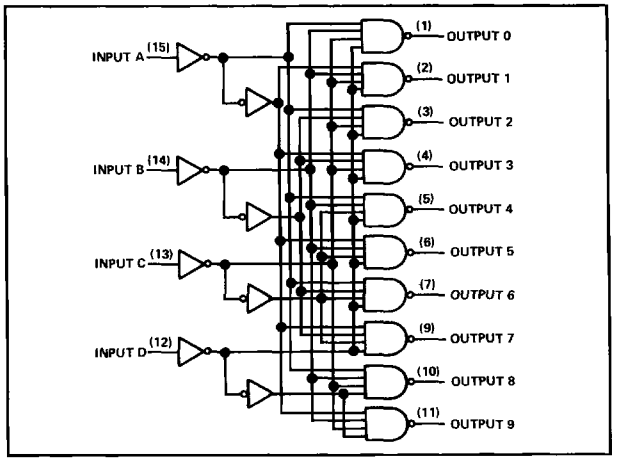


FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, (off), L = low level (on)

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

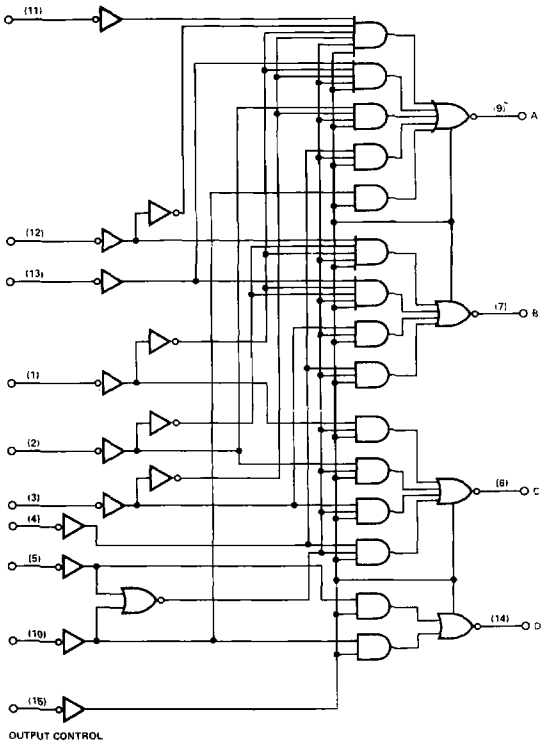
TEST CONDITIONS	54/74 C_L=15pF R_L=100Ω			54/74LS C_L=45pF R_L=665Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time							
t_{PLH} Low-to-high			50			50	ns
t_{PHL} High-to-low			50			50	ns

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

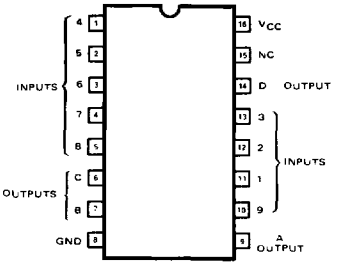
BLOCK DIAGRAM



Pin (16) = V_{CC}, Pin (8) - GND
Pin (15) = No connection

PIN CONFIGURATION

B,F,W PACKAGE



NC - no internal connection

TRUTH TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L = 15pF R_L = 400Ω				
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	WAVEFORM	UNIT
Propagation delay time							
t_{PLH} Low-to-high	Any	Any		9	14	In phase output	ns
t_{PHL} High-to-low				7	11		
t_{PLH} Low-to-high				13	19	Out of phase output	
t_{PHL} High-to-low				10	15		

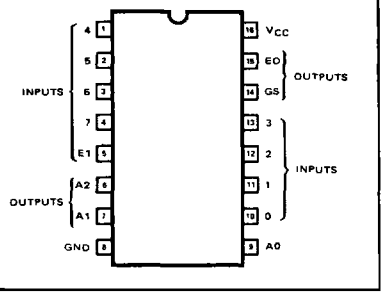
Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

PIN CONFIGURATION

B,F,W PACKAGE



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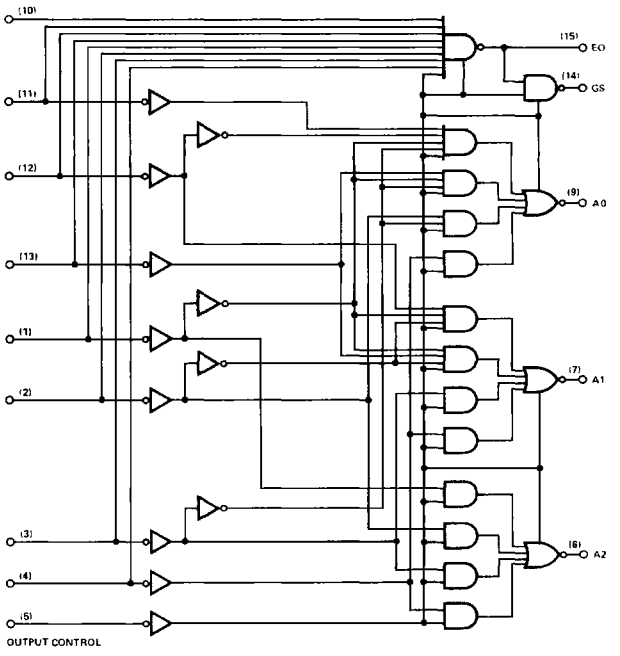

Pin (16)=V_{CC}, pin (8)=GND

TRUTH TABLE

INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω				
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	WAVEFORM	UNIT
Propagation delay time								
t_{PLH}	Low-to-high	0-7	A_0,A_1,A_2		10	15	In phase output	ns
t_{PHL}	High-to-low				9	14		
t_{PLH}	Low-to-high				13	19	Out of phase output	
t_{PHL}	High-to-low				10	15		
t_{PLH}	Low-to-high	0-7	E_0		6	10	Out of phase output	
t_{PHL}	High-to-low				9	14		
t_{PLH}	Low-to-high	0-7	GS		14	21	In phase output	
t_{PHL}	High-to-low				12	18		
t_{PLH}	Low-to-high	E_1	A_0,A_1,A_2		10	15	In phase output	
t_{PHL}	High-to-low				10	15		
t_{PLH}	Low-to-high	E_1	GS		8	12	In phase output	
t_{PHL}	High-to-low				10	15		
t_{PLH}	Low-to-high	E_1	E_0		8	13	In phase output	
t_{PHL}	High-to-low				13	19		

Load circuit and typical waveforms are shown at the front of section.