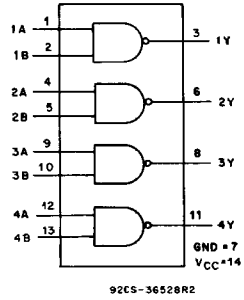
CD54AC00/3A
CD54ACT00/3A

Quad 2-Input NAND Gate

The RCA CD54AC00/3A and CD54ACT00/3A are quad 2-input NAND gates that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC00/3A and CD54ACT00/3A are supplied in 14-lead dual-in-line ceramic packages (F suffix).



92CS-36528R2

FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Package Specifications
See Section 11, Fig. 10

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				+25		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (SSI) I_{CC}	V_{CC} or GND	0	5.5	—	4•	—	80•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54AC/ACT00	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR 50 kHz**	**25 kHz**
CD54AC/ACT00	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54AC00/3A
CD54ACT00/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delay Input to Output	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 3.1 2.2	91 10.2 7.3•	ns
Power Dissipation Capacitance	C_{PD}§	—	45 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delay Input to Output	t_{PLH}	5†	3.2	10.8•	ns
	t_{PHL}		4	13.2•	
Power Dissipation Capacitance	C_{PD}§	—	45 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per gate.
For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage

(Limits with black dots (•) are tested 100%.)

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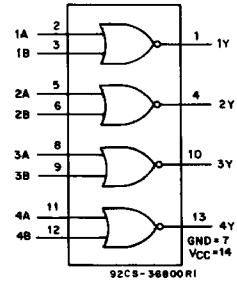
Quad 2-Input NOR Gate

CD54AC02/3A
CD54ACT02/3A

The RCA CD54AC02/3A and CD54ACT02/3A are quad 2-input NOR gates that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC02/3A and CD54ACT02/3A are supplied in 14-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Package Specifications

See Section 11, Fig. 10