
HD74LV2G74A

Single D-type Flip Flops with Preset and Clear

HITACHI

ADE-205-346 (Z)
1st. Edition
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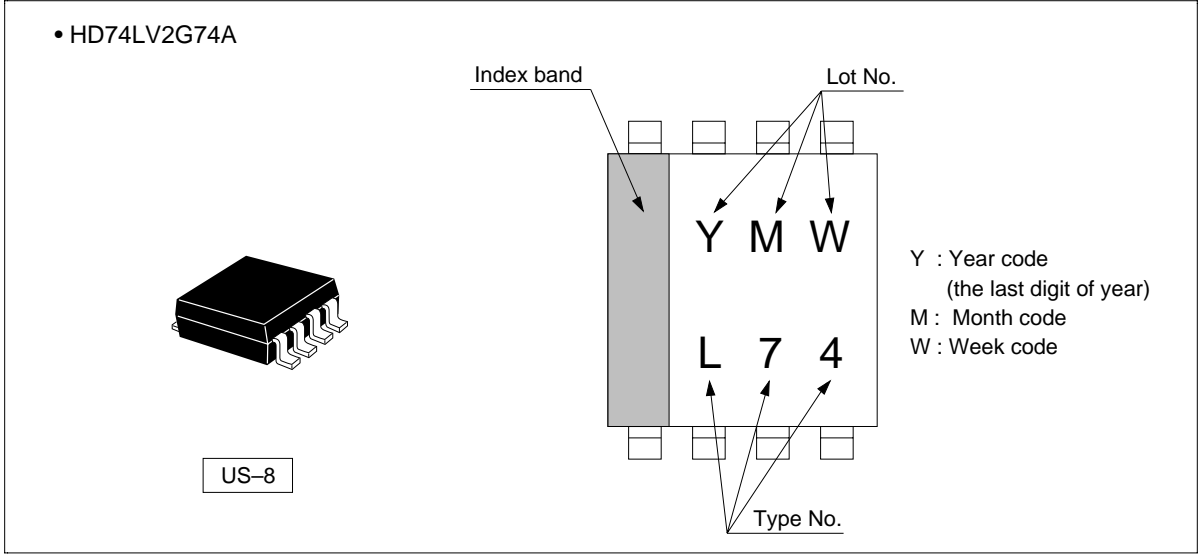
Description

The HD74LV2G74A has independent data, preset, clear, and clock inputs Q and \bar{Q} outputs in a 8 pin package. The input data is transferred to the output at the rising edge of clock pulse CLK. Low voltage and high speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- The basic gate function is lined up as hitachi uni logic series.
- Supplied on emboss taping for high speed automatic mounting.
- Electrical characteristics equivalent to the HD74LV74A
Supply voltage range : 1.65 to 5.5 V
Operating temperature range : -40 to +85°C
- All inputs V_{IH} (Max.) = 5.5 V (@ V_{CC} = 0 V to 5.5 V)
All outputs V_O (Max.) = 5.5 V (@ V_{CC} = 0 V)
- Output current ± 6 mA (@ V_{CC} = 3.0 V to 3.6 V), ± 12 mA (@ V_{CC} = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.

Outline and Article Indication



Function Table

Inputs				Outputs	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ^{*1}	H ^{*1}
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	↓	X	Q ₀	$\overline{\text{Q}}_0$

H : High level

L : Low level

X : Immaterial

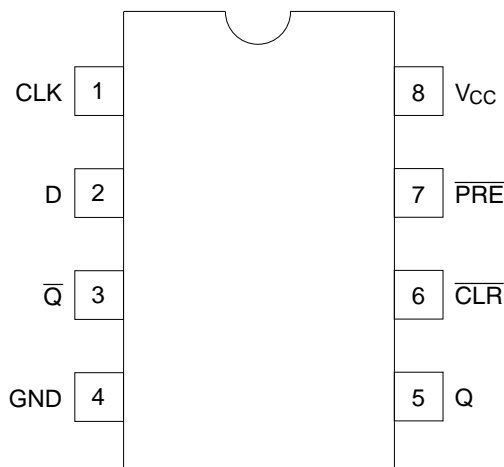
↑ : Low to high transition

↓ : High to low transition

Q₀ : The level of Q immediately before the input conditions shown in the above table are determined.

Note : 1. Q and $\overline{\text{Q}}$ will remain high as long as preset and clear are low, but Q and $\overline{\text{Q}}$ are unpredictable, if preset and clear go high simultaneously.

Pin Arrangement



(Top view)

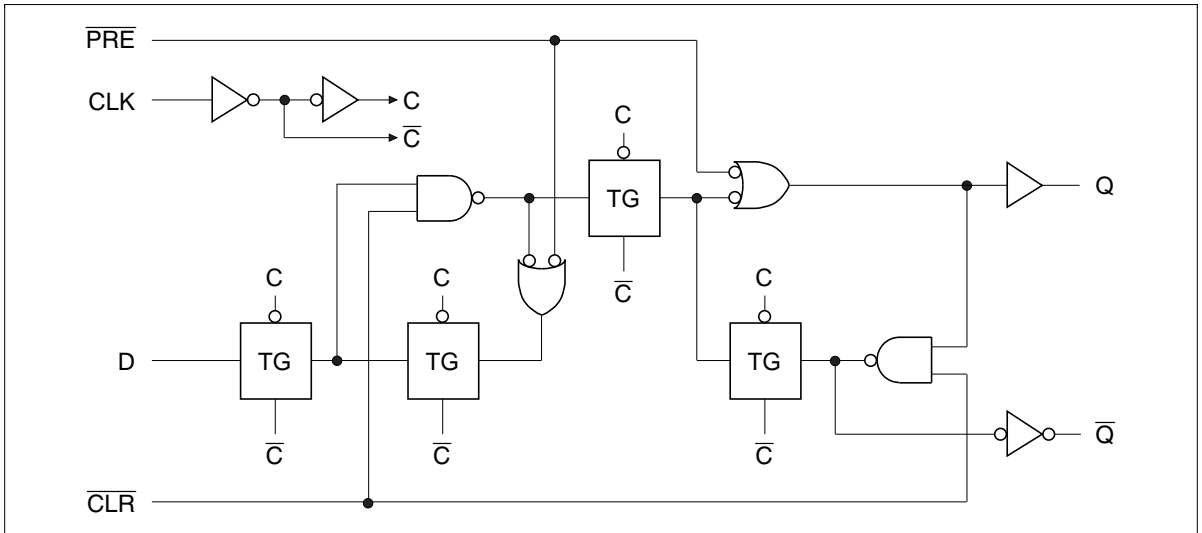
Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage	V_{CC}	-0.5 to 7.0	V	
Input voltage	V_{IN}	-0.5 to 7.0	V	
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output : H or L V_{CC} : OFF
Input diode current	I_{IK}	-20	mA	
Output diode current	I_{OK}	± 50	mA	
Output current	I_{OUT}	± 25	mA	
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA	
Power dissipation	P_T	200	mW	
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	1.65 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to +85	°C
Input rise / fall time	t_r, t_f	0 to 300 ($V_{CC} = 1.65$ to 1.95 V)	ns
		0 to 200 ($V_{CC} = 2.3$ to 2.7 V)	
		0 to 100 ($V_{CC} = 3.0$ to 3.6 V)	
		0 to 20 ($V_{CC} = 4.5$ to 5.5 V)	

Logic Diagram



Electrical Characteristic

• Ta = -40 to 85°C

Item	Symbol	V _{CC} (V) *	Min	Typ	Max	Unit	Test condition
Input voltage	V _{IH}	1.65 to 1.95	V _{CC} ×0.75	—	—	V	
		2.3 to 2.7	V _{CC} ×0.7	—	—		
		3.0 to 3.6	V _{CC} ×0.7	—	—		
		4.5 to 5.5	V _{CC} ×0.7	—	—		
	V _{IL}	1.65 to 1.95	—	—	V _{CC} ×0.25		
		2.3 to 2.7	—	—	V _{CC} ×0.3		
		3.0 to 3.6	—	—	V _{CC} ×0.3		
		4.5 to 5.5	—	—	V _{CC} ×0.3		
Hysteresis voltage	V _H	1.8	—	0.25	—	V	V _T ⁺ - V _T ⁻
		2.5	—	0.30	—		
		3.3	—	0.35	—		
		5.0	—	0.45	—		
Output voltage	V _{OH}	Min to Max	V _{CC} -0.1	—	—	V	I _{OH} = -50 μA
		1.65	1.4	—	—		I _{OH} = -1 mA
		2.3	2.0	—	—		I _{OH} = -2 mA
		3.0	2.48	—	—		I _{OH} = -6 mA
		4.5	3.8	—	—		I _{OH} = -12 mA
	V _{OL}	Min to Max	—	—	0.1		I _{OL} = 50 μA
		1.65	—	—	0.3		I _{OL} = 1 mA
		2.3	—	—	0.4		I _{OL} = 2 mA
		3.0	—	—	0.44		I _{OL} = 6 mA
		4.5	—	—	0.55		I _{OL} = 12 mA
Input current	I _{IN}	0 to 5.5	—	—	±1	μA	V _{IN} = 5.5 V or GND
Quiescent supply current	I _{CC}	5.5	—	—	10	μA	V _{IN} = V _{CC} or GND, I _O = 0
Output leakage current	I _{OFF}	0	—	—	5	μA	V _O = 5.5 V
Input capacitance	C _{IN}	3.3	—	2.5	—	pF	V _{IN} = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

• $V_{CC} = 1.8 \pm 0.15 \text{ V}$

Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{\max}	30	60	—	20	—	MHz	$C_L = 15 \text{ pF}$		
		20	40	—	15	—		$C_L = 50 \text{ pF}$		
Propagation delay time	t_{PLH}	—	16.3	27.0	1.0	29.0	ns	$C_L = 15 \text{ pF}$	PRE/CLR	Q or \bar{Q}
	t_{PHL}	—	17.9	29.0	1.0	32.0			CLK	
		—	21.6	34.0	1.0	36.5	ns	$C_L = 50 \text{ pF}$	PRE/CLR	Q or \bar{Q}
		—	24.5	39.5	1.0	42.5			CLK	
Setup time	t_{su}	13.0	—	—	14.0	—	ns		D	
		9.0	—	—	9.0	—			PRE or CLR inactive	
Hold time	t_h	0.5	—	—	0.5	—	ns			
Pulse width	t_w	12.0	—	—	13.0	—	ns		PRE or CLR	"L"
		12.0	—	—	13.0	—			CLK	"H" or "L"

• $V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{\max}	50	100	—	40	—	MHz	$C_L = 15 \text{ pF}$		
		30	70	—	25	—		$C_L = 50 \text{ pF}$		
Propagation delay time	t_{PLH}	—	9.8	14.8	1.0	17.0	ns	$C_L = 15 \text{ pF}$	PRE/CLR	Q or \bar{Q}
	t_{PHL}	—	11.1	16.4	1.0	19.0			CLK	
		—	13.0	17.4	1.0	20.0	ns	$C_L = 50 \text{ pF}$	PRE/CLR	Q or \bar{Q}
		—	14.2	20.0	1.0	23.0			CLK	
Setup time	t_{su}	8.0	—	—	9.0	—	ns		D	
		7.0	—	—	7.0	—			PRE or CLR inactive	
Hold time	t_h	0.5	—	—	0.5	—	ns			
Pulse width	t_w	8.0	—	—	9.0	—	ns		PRE or CLR	"L"
		8.0	—	—	9.0	—			CLK	"H" or "L"

Switching Characteristics (cont)

• $V_{CC} = 3.3 \pm 0.3$ V

Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40$ to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{\max}	80	140	—	70	—	MHz	$C_L = 15$ pF		
		50	90	—	45	—		$C_L = 50$ pF		
Propagation delay time	t_{PLH}	—	6.9	12.3	1.0	14.5	ns	$C_L = 15$ pF	$\overline{\text{PRE}}/\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$
	t_{PHL}	—	7.9	11.9	1.0	14.0			CLK	
		—	9.2	15.8	1.0	18.0	ns	$C_L = 50$ pF	$\overline{\text{PRE}}/\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$
		—	10.2	15.4	1.0	17.5			CLK	
Setup time	t_{su}	6.0	—	—	7.0	—	ns		D	
		5.0	—	—	5.0	—		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive		
Hold time	t_h	0.5	—	—	0.5	—	ns			
Pulse width	t_w	6.0	—	—	7.0	—	ns		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ "L"	
		6.0	—	—	7.0	—		CLK "H" or "L"		

• $V_{CC} = 5.0 \pm 0.5$ V

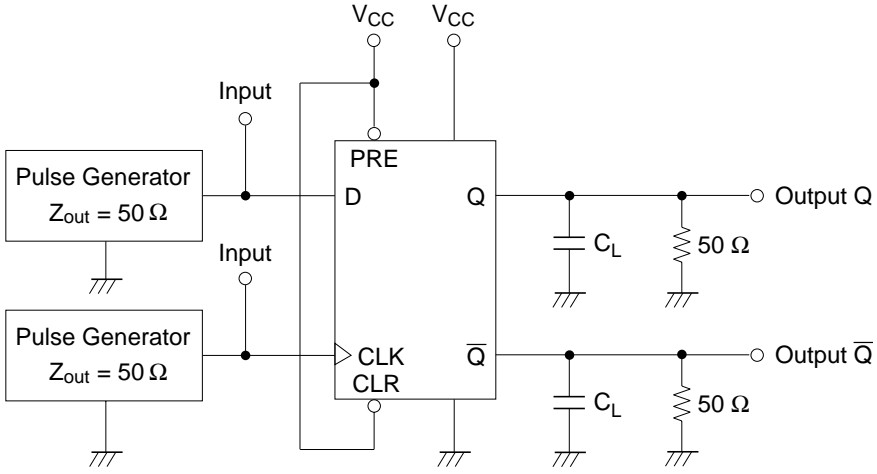
Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40$ to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{\max}	130	180	—	110	—	MHz	$C_L = 15$ pF		
		90	140	—	75	—		$C_L = 50$ pF		
Propagation delay time	t_{PLH}	—	5.0	7.7	1.0	9.0	ns	$C_L = 15$ pF	$\overline{\text{PRE}}/\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$
	t_{PHL}	—	5.6	7.3	1.0	8.5			CLK	
		—	6.6	9.7	1.0	11.0	ns	$C_L = 50$ pF	$\overline{\text{PRE}}/\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$
		—	7.2	9.3	1.0	10.5			CLK	
Setup time	t_{su}	5.0	—	—	5.0	—	ns		D	
		3.0	—	—	3.0	—		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive		
Hold time	t_h	0.5	—	—	0.5	—	ns			
Pulse width	t_w	5.0	—	—	5.0	—	ns		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ "L"	
		5.0	—	—	5.0	—		CLK "H" or "L"		

Operating Characteristics

- $C_L = 50 \text{ pF}$

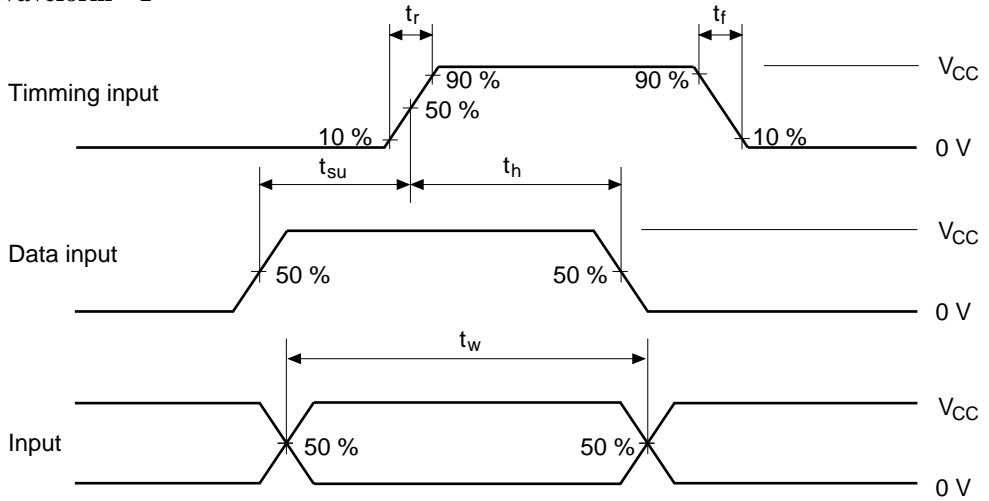
Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation	C_{PD}	3.3	—	13.0	—	pF	f = 10 MHz
capacitance		5.0	—	14.0	—		

Test Circuit

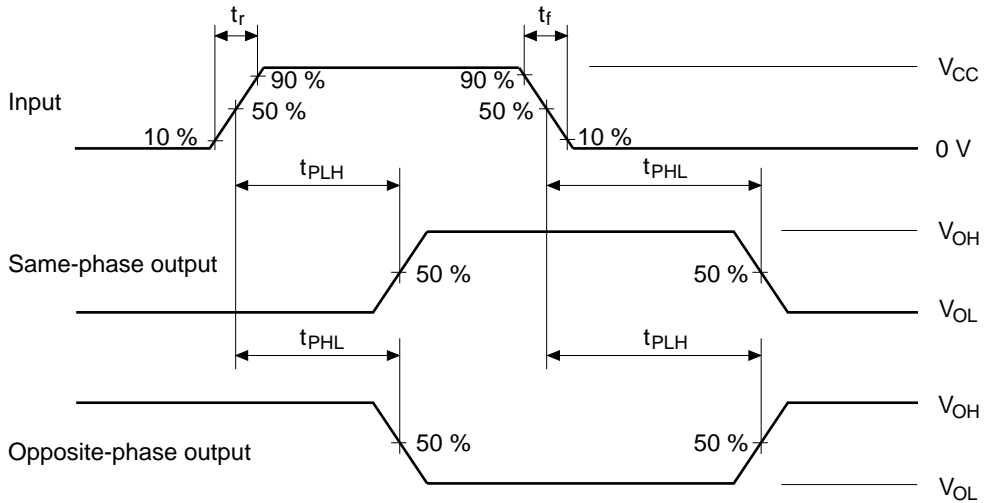


- Notes: 1. C_L includes probe and jig capacitance.
2. Test is put into the each flip flops.

• Waveform – 1



• Waveform – 2

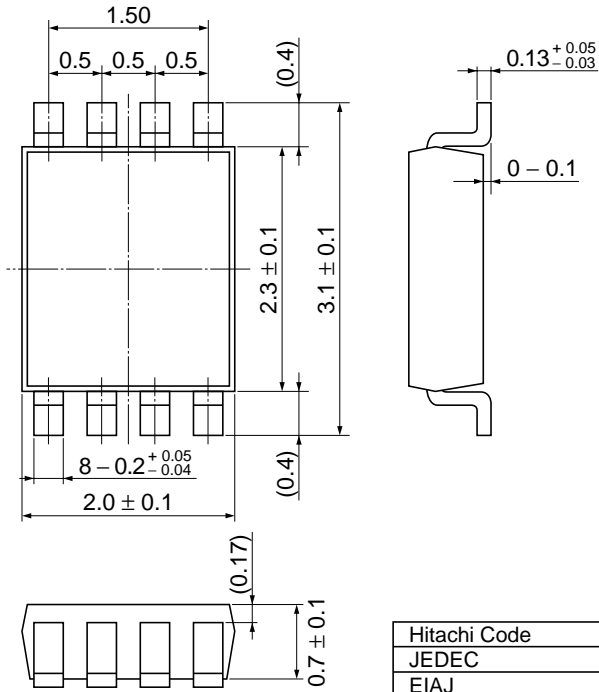


Notes: 1. Input waveform : PRR = 1 MHz, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$

2. The output are measured one at a time with one transition per measurement.

Package Dimensions

Unit : mm



Hitachi Code	US-8
JEDEC	SSOP-8
EIAJ	—
Mass (reference value)	—

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