Standard Products

UT54ACS164646S

RadHard Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver
Advanced Datasheet

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www.aeroflex.com/radhard

FEATURES

- Voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Flow-through architecture optimizes PCB layout
- Cold- and Warm-sparing
  - 1MΩ minimum input impedance power-off
  - Guranteed output tri-state while one power supply is "off" and the other is "on"
- Schmitt trigger inputs to filter noisy signals
- 0.6µm Commercial RadHard^{TM} CMOS
  - Total dose: 100K rad(Si)
  - Single Event Latchup immune
  - SEU Onset LET >40 MeV-cm^2/mg
- High speed, low power consumption
- Available QML Q or V processes
- Standard Microcircuit Drawing: 5962-06234
- Package:
  - 56-pin ceramic flatpack

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$x	Output Enable Input (Active Low)
DIRx	Direction Control Inputs
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)
xSAB	Select real-time or stored A bus data to B bus
xSBA	Select real-time or stored B bus data to A bus
xCLKAB	Store A bus data
xCLKBA	Store B bus data

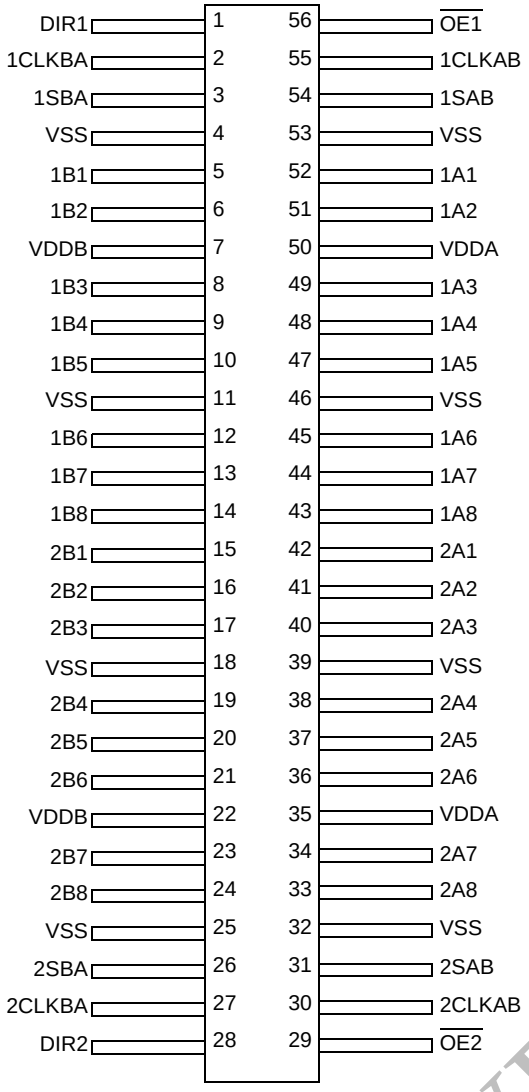
DESCRIPTION

The UT54ACS164646S is a 16-bit, MultiPurpose, registered, level shifting, bus transceiver consisting of D-type flip-flops, control circuitry, and 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The high-speed, low power UT54ACS164646S transceiver is designed to perform multiple functions including: asynchronous two-way communication, signal buffering, voltage translation, cold- and warm-sparing. The device can be used as two independant 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. With either V_{DD} supply equal to zero volts, the UT54ACS164646S outputs and inputs present a minimum impedance of 1MΩ making it ideal for “cold-spare” and "warm-spare" applications. By virtue of its flexible power supply interface, the UT54ACS164646S may operate as a 3.3-volt only, 5-volt only, or mixed 3.3V/5V bus transceiver.

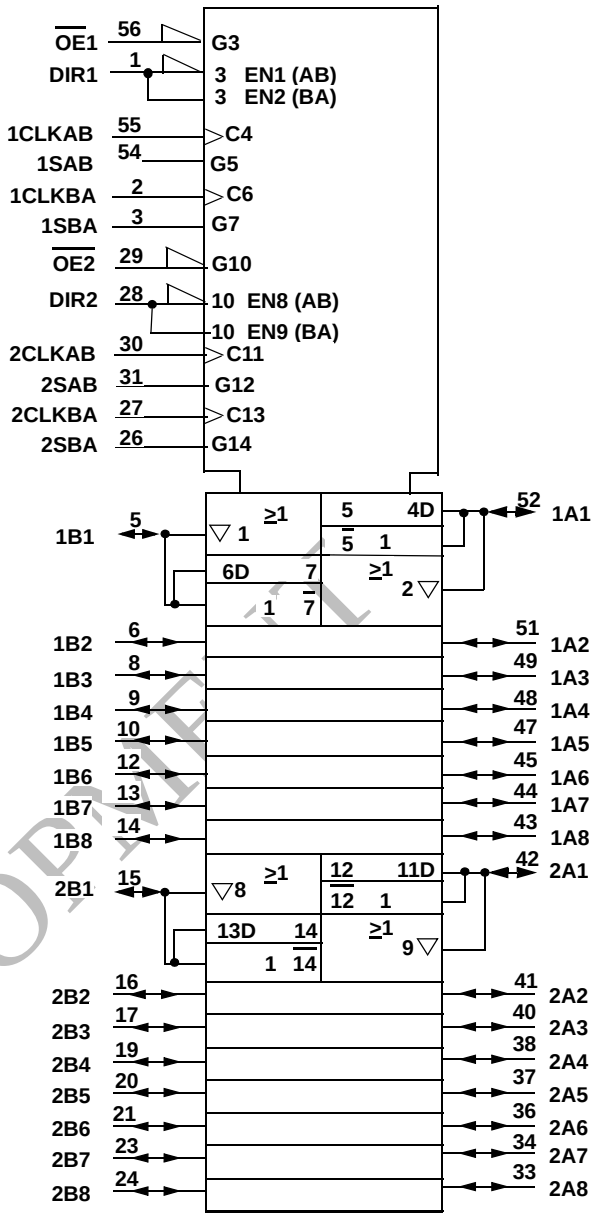
The Output-enable ($\overline{OE}$x) and direction-control (DIRx) inputs are provided to control the tri-state function and input/output direction of the transceiver respectively. The select controls (SAB and SBA) select whether stored register data or real-time data is driven to the outputs as determined by the DIRx inputs. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Regardless of the selected operating mode ("real-time" or "recall"), a rising edge on the port input clocks (xCLKAB and xCLKBA) will latch the corresponding I/O states into their respective registers. Furthermore, when a data port is isolated ($\overline{OE}$x = high), A-port data may be stored into its corrsponding register while B-port data may be independantly stored into its corresponding registers. Therefore, when an output function is disabled, the input function is still enabled and may be used to store and transmit data. Lastly, only one of the two buses, xA-port or xB-port, may be driven at a time.

56-Lead Flatpack

Pinout



LOGIC SYMBOL



POWER TABLE

Port B	Port A	OPERATION
5 Volts	3.3 Volts	Voltage Translator
5 Volts	5 Volts	Non Translating
3.3 Volts	3.3 Volts	Non Translating
V_{SS}	V_{SS}	Cold Spare
V_{SS}	3.3V or 5V	Port B Warm Spare
3.3V or 5V	V_{SS}	Port A Warm Spare

I/O GUIDELINES

Control signals DIRx, $\overline{OEx}$, xSAB, xSBA, xCLKAB, and xCLKBA are 5-volt tolerant inputs power by V_{DDA}. Therefore, when V_{DDA} is at 3.3-volts, either 3.3- or 5-volt CMOS logic levels may be applied to all control inputs. Additionally, it is recommended that all unused inputs be tied to V_{SS} through a 1KΩ resistor. Input signal transistion should be driven to the UT54ACS164646S with a rise and fall time that is $\leq$ 100µs.

POWER APPLICATION GUIDELINES

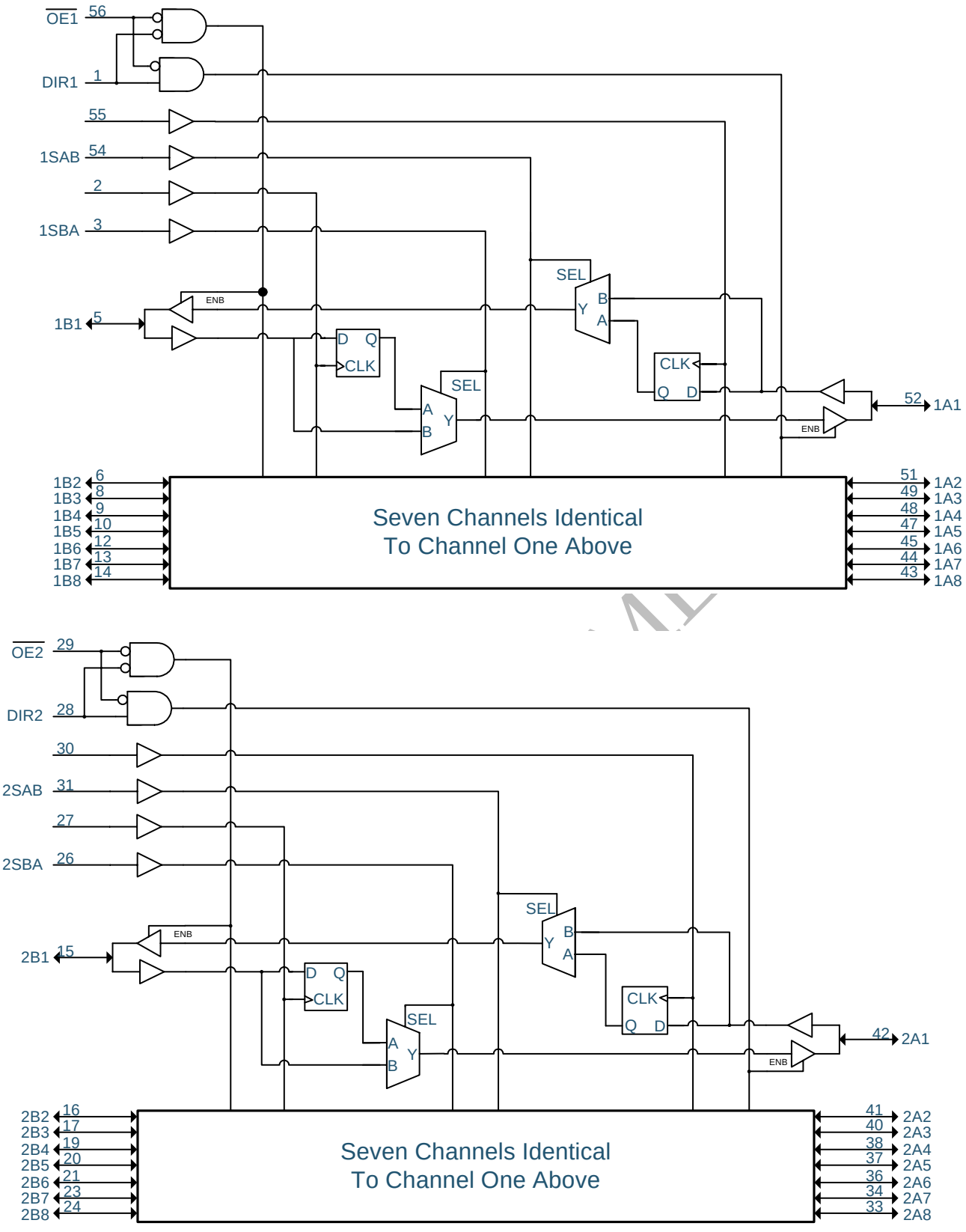
For proper operation connect power to all V_{DDx} and ground all V_{SS} pins (i.e., no floating V_{DDx} or V_{SS} input pins). By virtue of the UT54ACS164646S warm-spare feature, power supplies V_{DDB} and V_{DDA} may be applied to the device in any order. To ensure the device is in cold-spare, both supplies, V_{DDB} and V_{DDA} , must be equal to V_{SS} +/- 0.3V. Warm-spare operation is in effect when on power supply is >1V and the other power supply is equal to V_{SS} +/- 0.3V. If V_{DDB} has a power-on ramp rate longer than 1 second, then V_{DDA} should be powered-on first to ensure proper control of DIRx and $\overline{OEx}$. During normal operation of the part, after power-up, ensure $V_{DDB} \geq V_{DDA}$.

FUNCTION TABLE

Inputs						Data I/O+		Operation or Function
$\overline{OEx}$	DIRx	xCLKAB	xCLKBA	xSAB	xSBA	xA1-xA8	xB1-xB8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified+
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified+
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Recall stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B Bus
L	H	H or L	X	H	X	Input	Output	Recall stored A data to B bus

+ The data-output functions may be enabled or disabled by various signals $\overline{OEx}$ or DIRx. Data-input functions are always enabled, i.e. data at the bus terminals is stored on every low-to-high transition of the clock inputs.

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rad(Si)
SEL LET Threshold	>111	MeV-cm^2/mg
SEU Onset LET Threshold	TBD	MeV-cm^2/mg
SEU Error Rate[2]	TBD	errors/bit-day
Neutron Fluence[3]	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Adams 90% worst case particle environment, geosynchronous orbit, 100mils of Aluminum shielding
3. Not tested, inherent of CMOS technology.

WEIBUL PARAMETERS

SHAPE PARAMETER	WIDTH PARAMETER	SATURATED CROSS-SECTION	ONSET LET	DEVICE DEPTH	FUNNEL DEPTH
TBD	TBD	TBD	TBD	TBD	TBD

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
$V_{I/OB}$ (Port B)[2]	Voltage any pin	-0.3 to V_{DDB} +0.3	V
$V_{I/OA}$ (Port A)[2]	Voltage any pin	-0.3 to V_{DDA} +0.3	V
V_{DDB}	Supply voltage	-0.3 to 6.0	V
V_{DDA}	Supply voltage	-0.3 to 6.0	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. For cold spare mode (V_{DDx} = V_{SS} +/- 0.3V), $V_{I/Ox}$ may be -0.3V to the maximum recommended operating V_{DDx} + 0.3V.

DUAL SUPPLY OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DDB} [1]	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V_{DDA} [1]	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V_{INB} (Port B)	Input voltage any pin	0 to V_{DDB}	V
V_{INA} (Port A)	Input voltage any pin	0 to V_{DDA}	V
T_C	Temperature range	-55 to + 125	°C

Note:
1. During normal operation, $V_{DDB} \geq V_{DDA}$.

DC ELECTRICAL CHARACTERISTICS [1]
(T_C = -55°C to +125°C for "C" screening and -40°C to +125°C for "W" screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_T+	Schmitt Trigger, positive going threshold[2]	V_{DDx} from 3.00 to 5.5		$.7V_{DDx}$	V
V_T-	Schmitt Trigger, negative going threshold[2]	V_{DDx} from 3.00 to 5.5	$.3V_{DDx}$		V
V_{H1}	Schmitt Trigger range of hysteresis[10]	V_{DDx} from 4.5 to 5.5	0.7		V
V_{H2}	Schmitt Trigger range of hysteresis[10]	V_{DDx} from 3.00 to 3.6	0.5		V
I_{IN}	Input leakage current[10]	V_{DDx} from 3.6 to 5.5 V_{IN} = V_{DDx} or V_{SS}	-1	3	µA
I_{OZ}	Three-state output leakage current[10]	V_{DDx} from 3.6 to 5.5 V_{IN} = V_{DDx} or V_{SS}	-1	3	µA
I_{CS}	Cold sparing input leakage current[3] (any pin)	V_{IN} = 5.5 V_{DDB} = V_{DDA} = V_{SS} +/- 0.3V	-5	5	µA
I_{WSB}	Warm sparing input leakage current[3] (any pin)	V_{IN} = 5.5; V_{DDA} = 3V to 5.5V V_{DDB} = V_{SS} +/- 0.3V	-5	5	µA
I_{WSA}	Warm sparing input leakage current[3] (any pin)	V_{IN} = 5.5; V_{DDB} = 3V to 5.5V V_{DDA} = V_{SS} +/- 0.3V	-5	5	µA
I_{OS1}	Short-circuit output current [6, 11]	V_O = V_{DDx} or V_{SS} V_{DDx} from 4.5 to 5.5	-200	200	mA
I_{OS2}	Short-circuit output current [6, 11]	V_O = V_{DDx} or V_{SS} V_{DDx} from 3.00 to 3.6	-100	100	mA
V_{OL1}	Low-level output voltage[4, 10]	V_{DDx} = 4.5V; I_{OL}= 8mA		0.4	V
		V_{DDx} = 4.5V; I_{OL}= 100µA		0.2	

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{OL2}	Low-level output voltage[4, 10]	V_{DDx} = 3.00V; I_{OL}= 8mA		0.5	V
		V_{DDx} = 3.00V; I_{OL}= 100µA		0.2	
V_{OH1}	High-level output voltage[4, 10]	V_{DDx} = 4.5V; I_{OH}= -8mA	V_{DDx} - 0.7		V
		V_{DDx} = 4.5V; I_{OH}= -100µA	V_{DDx} - 0.2		
V_{OH2}	High-level output voltage[4, 10]	V_{DDx} = 3.00V; I_{OH}= -8mA	V_{DDx} - 0.9		V
		V_{DDx} = 3.00V; I_{OH}= -100µA	V_{DDx} - 0.2		
P_{total1}	Power dissipation [5,7, 8]	C_L = 50pF V_{DDB} = V_{DDA} = 4.5V to 5.5V		2.0	mW/ MHz
P_{total2}	Power dissipation [5, 7, 8]	C_L = 50pF V_{DDB} = V_{DDA} = 3.00V to 3.6V		1.5	mW/ MHz
I_{DD}	Standby Supply Current V_{DDB} or V_{DDA} Pre-Rad 25°C	V_{IN} = V_{DDx} or V_{SS} V_{DDB} = V_{DDA} = 5.5V $\overline{OE}$ = V_{DDA}		10	µA
	Standby Supply Current V_{DDB} or V_{DDA} Pre-Rad -55°C to +125°C			100	
	Standby Supply Current V_{DDB} or V_{DDA} Post-Rad 25°C			500	
C_{IN}	Input capacitance [9]	*f* = 1MHz @ 0V V_{DDx} from 3.00V to 5.5V		15	pF
C_{OUT}	Output capacitance[9]	*f* = 1MHz @ 0V V_{DDx} from 3.00V to 5.5V		15	pF

Notes:

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
3. All combinations of $\overline{OE}$x and DIRx
4. Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
5. Guaranteed by characterization.
6. Not more than one output may be shorted at a time for maximum duration of one second.
7. Power does not include power contribution of any CMOS output sink current.
8. Power dissipation specified per switching output.
9. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
10. Guaranteed; tested on a sample of pins per device.
11. Supplied as a design limit, but not guaranteed or tested.

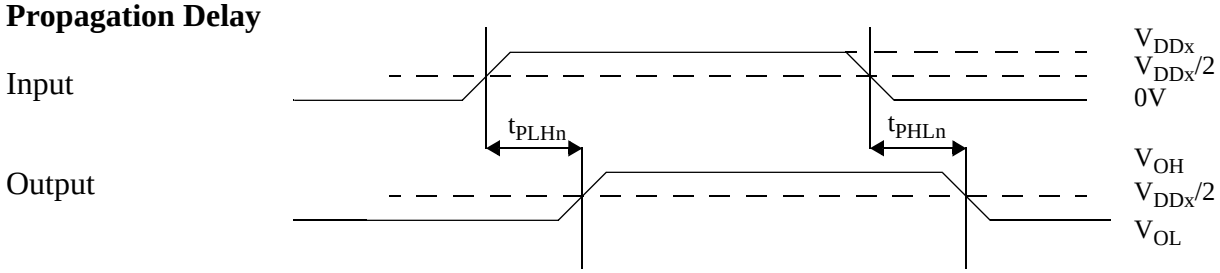
AC ELECTRICAL CHARACTERISTICS[1] (Port B = 5 Volt, Port A = 3.3 Volt)

(V_{DDB} = 5V ±10%; V_{DDA} = 3.3V ±0.3V) (T_C = -55°C to +125°C for "C" screening and -40°C to +125°C for "W" screening)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH1}	Propagation delay Data to Bus	3.5	9	ns
t_{PHL1}	Propagation delay Data to Bus	3.5	9	ns
t_{PLH2}	xCLKAB or xCLKBA to Bus	4.5	12	ns
t_{PHL2}	xCLKAB or xCLKBA to Bus	4.5	12	ns
t_{PLH3}[2]	xSAB or xSBA (with A or B high) to Bus	4	10.5	ns
t_{PHL3}[2]	xSAB or xSBA (with A or B high) to Bus	4	10.5	ns
t_{PLH4}[2]	xSBA or xSAB (with A or B high) to Bus	4	10.5	ns
t_{PHL4}[2]	xSBA or xSAB (with A or B high) to Bus	4	10.5	ns
t_{PZH1}	Output enable time $\overline{OE}$x to Bus	4	12	ns
t_{PZL1}	Output enable time $\overline{OE}$x to Bus	4	10	ns
t_{PLZ1}	Output disable time $\overline{OE}$x to Bus high impedance	5	11	ns
t_{PHZ1}	Output disable time $\overline{OE}$x to Bus high impedance	5	16	ns
t_{PZH2}[3]	Output enable time DIRx to Bus	1	18	ns
t_{PZL2}[3]	Output enable time DIRx to Bus	1	18	ns
t_{PLZ2}[3]	Output disable time DIRx to Bus high impedance	1	20	ns
t_{PHZ2}[3]	Output disable time DIRx to Bus high impedance	1	20	ns
t_{SKEW}[4]	Skew between outputs	0	600	ps
t_{OST}[5]	Dfiferential skew between outputs	0	1000	ps

Notes:
1. All specifications valid for radiation dose ≤ 1E5 rads(Si) per MIL-STD-883, Method 1019.
2. These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
3. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested.
4. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs. low-to-high.
5. Differential output skew is defined as the comparison of two outputs tramsitioning in opposite directions low-to-high and high-to-low.

Propagation Delay



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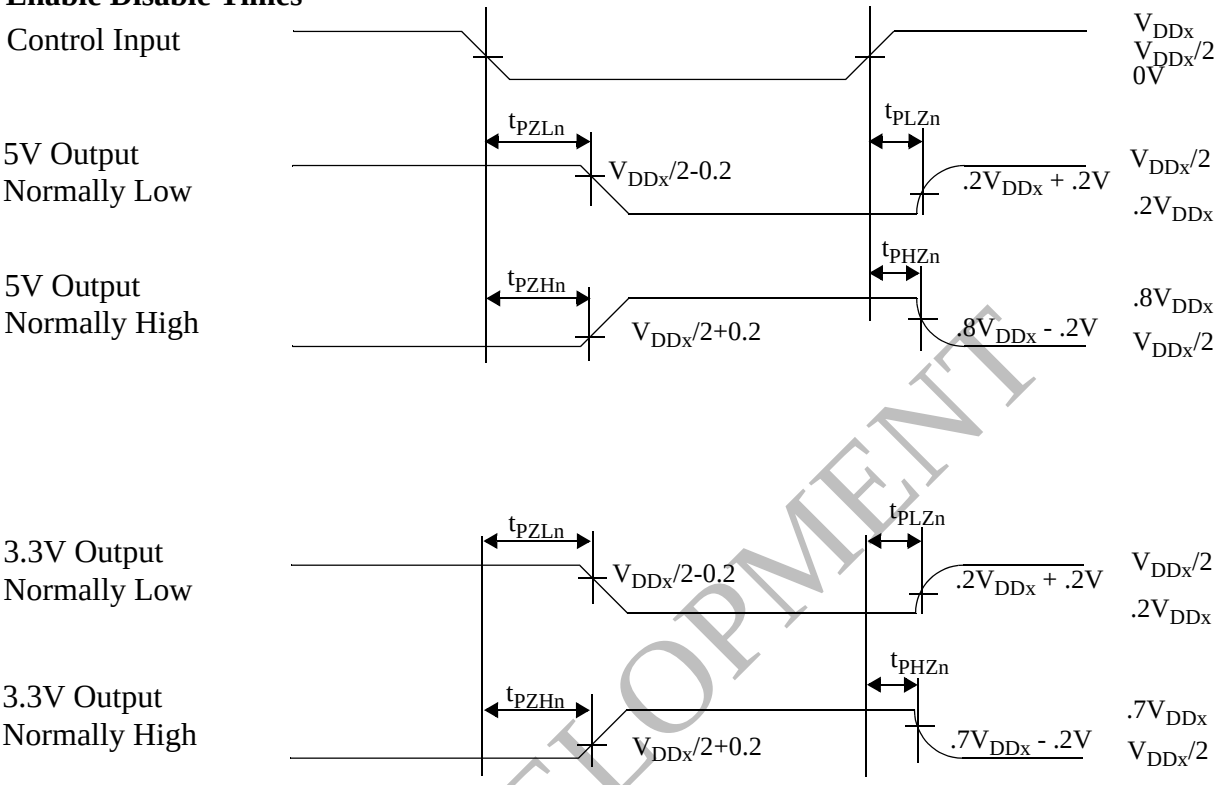

AC ELECTRICAL CHARACTERISTICS[1] (Port A = Port B, 5 Volt Operation)

(V_{DDB} = 5V ±10%; V_{DDA} = 5V ±10%) (T_C = -55°C to +125°C for "C" screening and -40°C to +125°C for "W" screening)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH1}	Propagation delay Data to Bus	3.5	7.5	ns
t_{PHL1}	Propagation delay Data to Bus	3.5	7.5	ns
t_{PLH2}	xCLKAB or xCLKBA to Bus	4	9	ns
t_{PHL2}	xCLKAB or xCLKBA to Bus	4	9	ns
t_{PLH3}[2]	xSAB or xSBA (with A or B high) to Bus	4	8	ns
t_{PH3L}[2]	xSAB or xSBA (with A or B high) to Bus	4	8	ns
t_{PLH4}[2]	xSBA or xSAB (with A or B high) to Bus	4	8	ns
t_{PHL4}[2]	xSBA or xSAB (with A or B high) to Bus	4	8	ns
t_{PZH1}	Output enable time $\overline{OE}$x to Bus	3.5	8	ns
t_{PZL1}	Output enable time $\overline{OE}$x to Bus	4.5	10	ns
t_{PLZ1}	Output disable time $\overline{OE}$x to Bus high impedance	4	9	ns
t_{PHZ1}	Output disable time $\overline{OE}$x to Bus high impedance	4	9	ns
t_{PZH2}[3]	Output enable time DIRx to Bus	1	12	ns
t_{PZL2}[3]	Output enable time DIRx to Bus	1	12	ns
t_{PLZ2}[3]	Output disable time DIRx to Bus high impedance	1	15	ns
t_{PHZ2}[3]	Output disable time DIRx to Bus high impedance	1	15	ns
t_{SKEW}[4]	Skew between outputs	0	400	ps
t_{OST}[5]	Differential output skew	0	600	ps

Notes:
1. All specifications valid for radiation dose ≤ 1E5 rads(Si) per MIL-STD-883, Method 1019.
2. These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
3. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested.
4. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs. low-to-high.
5. Differential output skew is defined as the comparison of two outputs tramsitioning in opposite directions low-to-high and high-to-low.

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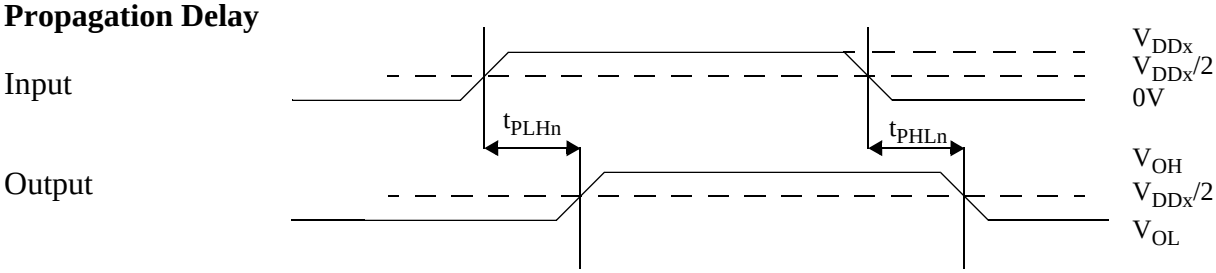

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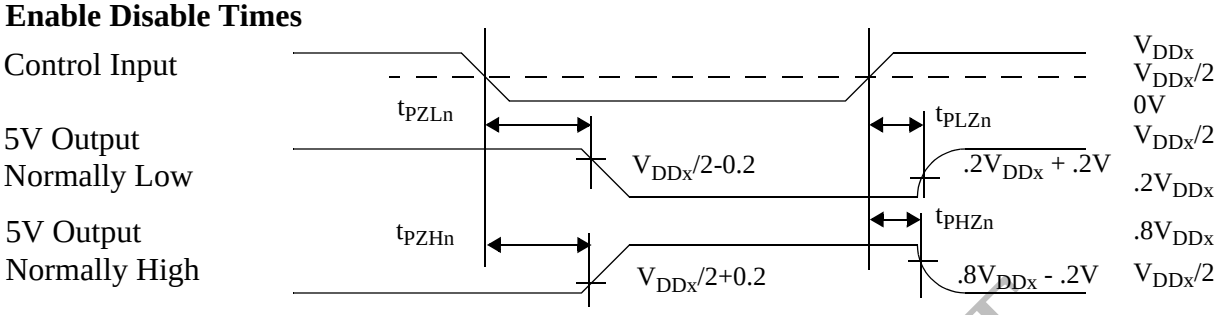


AC ELECTRICAL CHARACTERISTICS[1] (Port A = Port B, 3.3 Volt Operation)

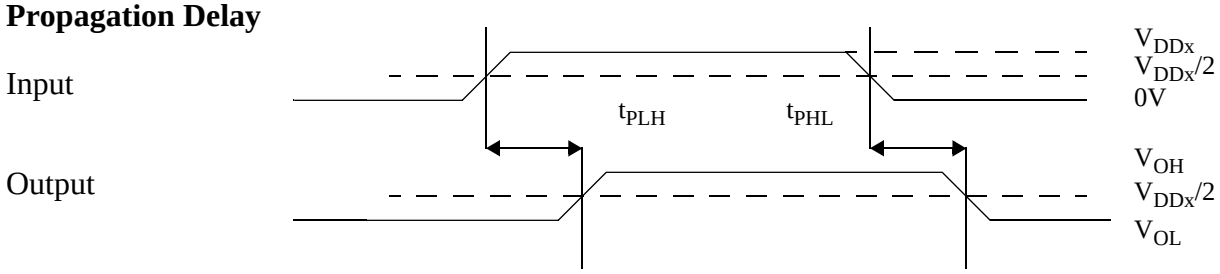
(V_{DDB} = V_{DDA} = 3.3V ±0.3V) (T_C = -55°C to +125°C for "C" screening and -40°C to +125°C for "W" screening)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH1}	Propagation delay Data to Bus	4	11	ns
t_{PHL1}	Propagation delay Data to Bus	4	11	ns
t_{PLH2}	xCLKAB or xCLKBA to Bus	4.5	12.5	ns
t_{PH2}	xCLKAB or xCLKBA to Bus	4.5	12.5	ns
t_{PLH3}[2]	xSAB or xSBA (with A or B high) to Bus	4.5	11	ns
t_{PHL3}[2]	xSAB or xSBA (with A or B high) to Bus	4.5	11	ns
t_{PLH4}[2]	xSBA or xSAB (with A or B high) to Bus	4.5	11	ns
t_{PHL4}[2]	xSBA or xSAB (with A or B high) to Bus	4.5	11	ns
t_{PZH1}	Output enable time $\overline{OE}$x to Bus	4	11	ns
t_{PZL1}	Output enable time $\overline{OE}$x to Bus	4	11	ns
t_{PLZ1}	Output disable time $\overline{OE}$x to Bus high impedance	4	10	ns
t_{PHZ1}	Output disable time $\overline{OE}$x to Bus high impedance	4	16	ns
t_{PZH2}[3]	Output enable time DIRx to Bus	1	18	ns
t_{PZL2}[3]	Output enable time DIRx to Bus	1	18	ns
t_{PLZ2}[3]	Output disable time DIRx to Bus high impedance	1	20	ns
t_{PHZ2}[3]	Output disable time DIRx to Bus high impedance	1	20	ns
t_{SKEW}[4]	Skew between outputs	0	700	ps
t_{OST}[5]	Differential output skew	0	1300	ps

Notes:

1. All specifications valid for radiation dose ≤ 1E5 rads(Si) per MIL-STD-883, Method 1019.
2. These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
3. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested.
4. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs. low-to-high.
5. Differential output skew is defined as the comparison of two outputs transitioning in opposite directions low-to-high and high-to-low.

Propagation Delay



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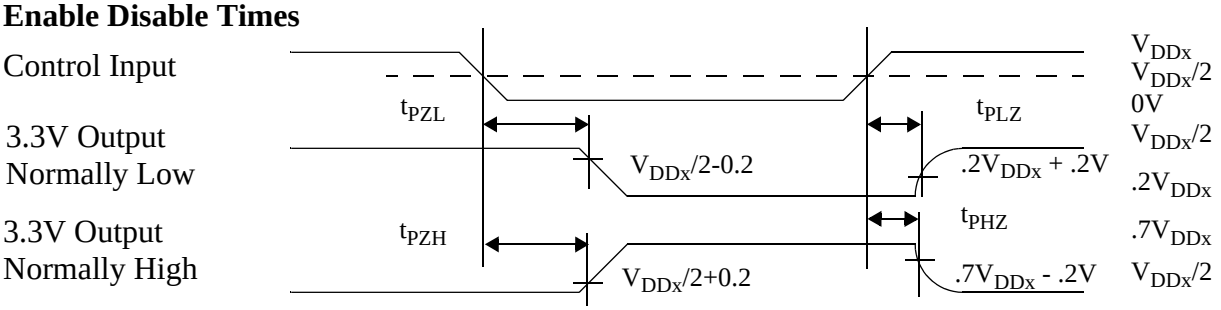
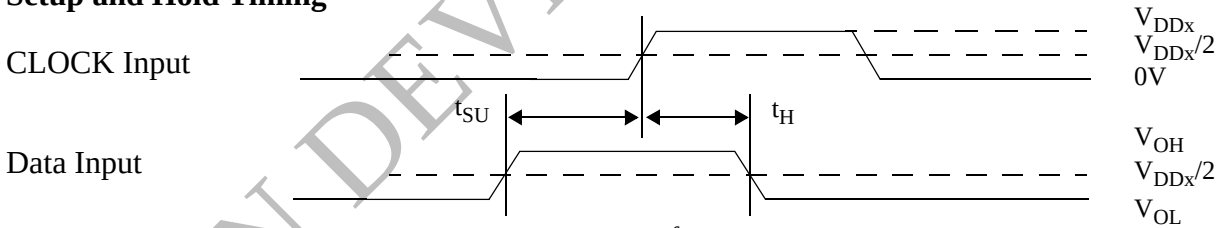


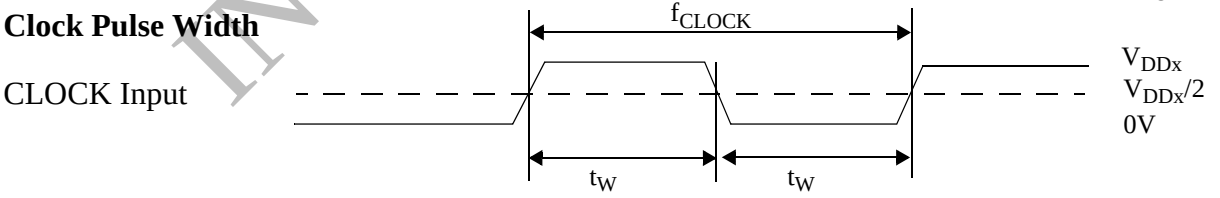
AC ELECTRICAL CHARACTERISTICS (Clock Input Timing Relationships)
(All Power Supply Operating Ranges, -55°C < T_C < +125°C)

SYMBOL	PARAMETER		MINIMUM	MAXIMUM	UNIT
f_{CLOCK}	Clock Frequency		0	100	MHz
t_W	Pulse duration. CLKAB or CLKBA high or low		5		ns
t_{SU}	Setup time. A before CLKAB rising edge or B before CLKBA rising edge	Data High	4		ns
		Data Low	6		
t_H	Hold time. A after CLKAB rising edge or B after CLKBA rising edge		1.5		ns

Setup and Hold Timing



Clock Pulse Width

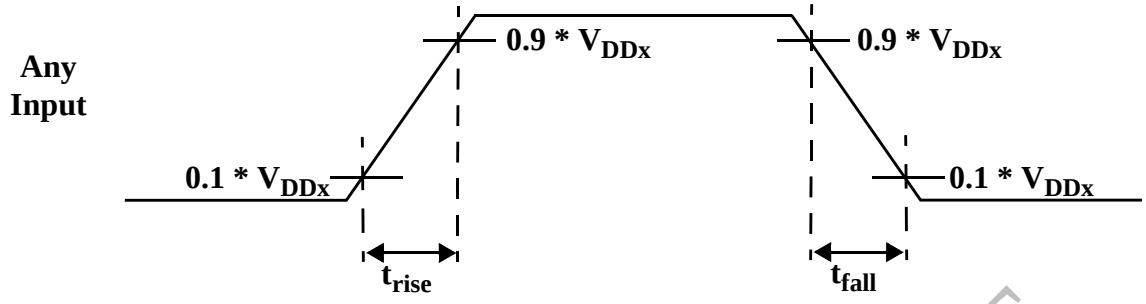


AC ELECTRICAL CHARACTERISTICS[1] (Input Rise and Fall Requirements)
(All Power Supply Ranges, -55°C < T_C < +125°C)

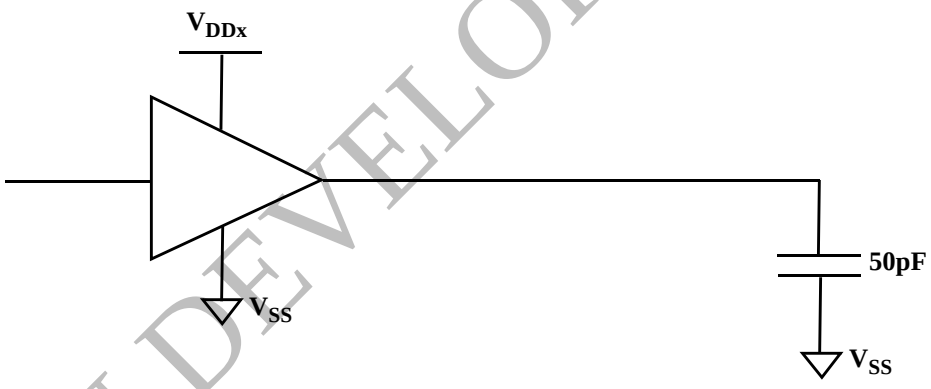
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{rise}	Input rise time	--	100	µs
t_{fall}	Input fall time	--	100	µs

Note: The input rise and fall parameter is guaranteed by characterization, and is not tested.

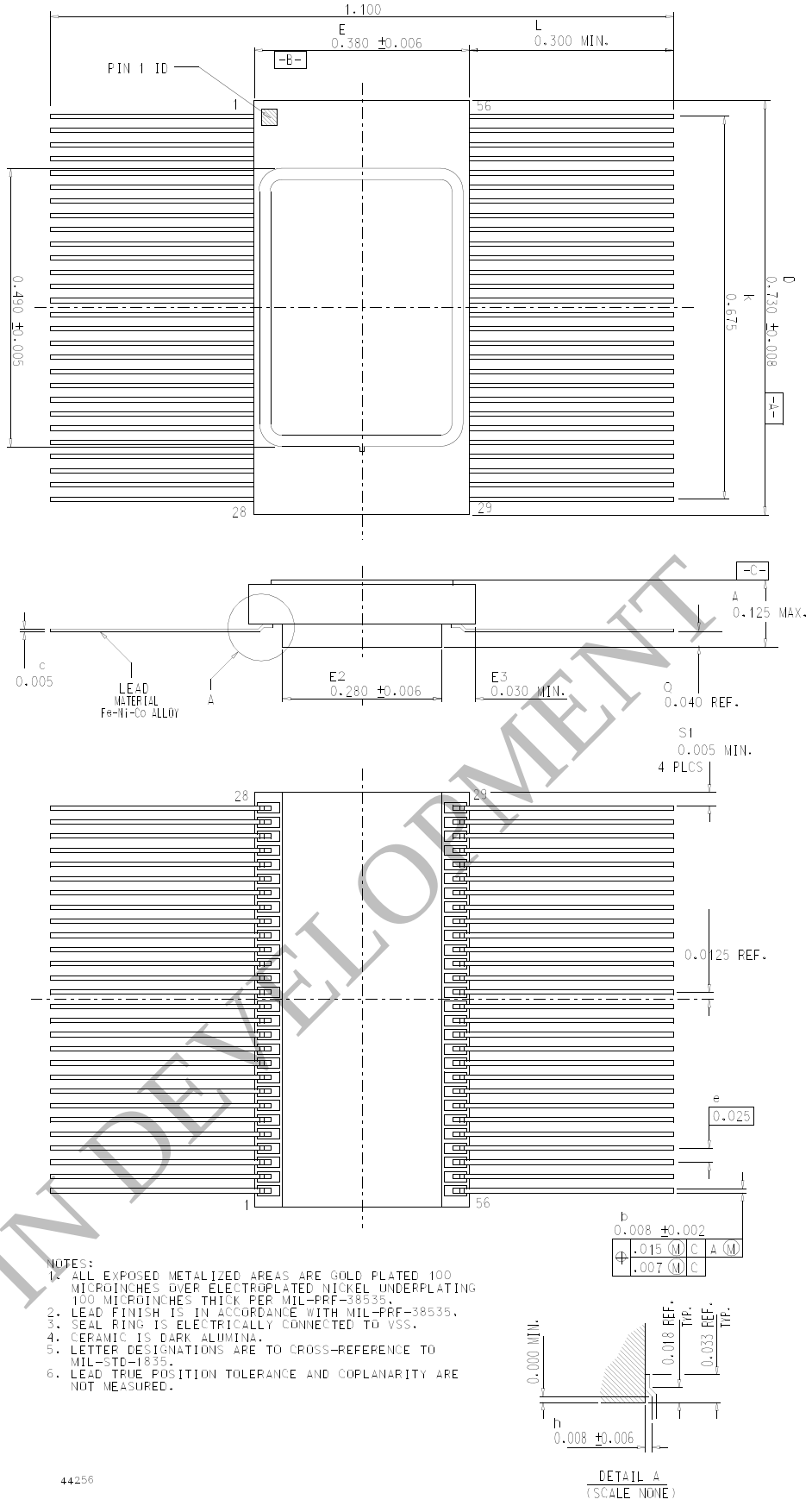
INPUT RISE AND FALL TIMING:



TEST LOAD CIRCUIT:



PACKAGE

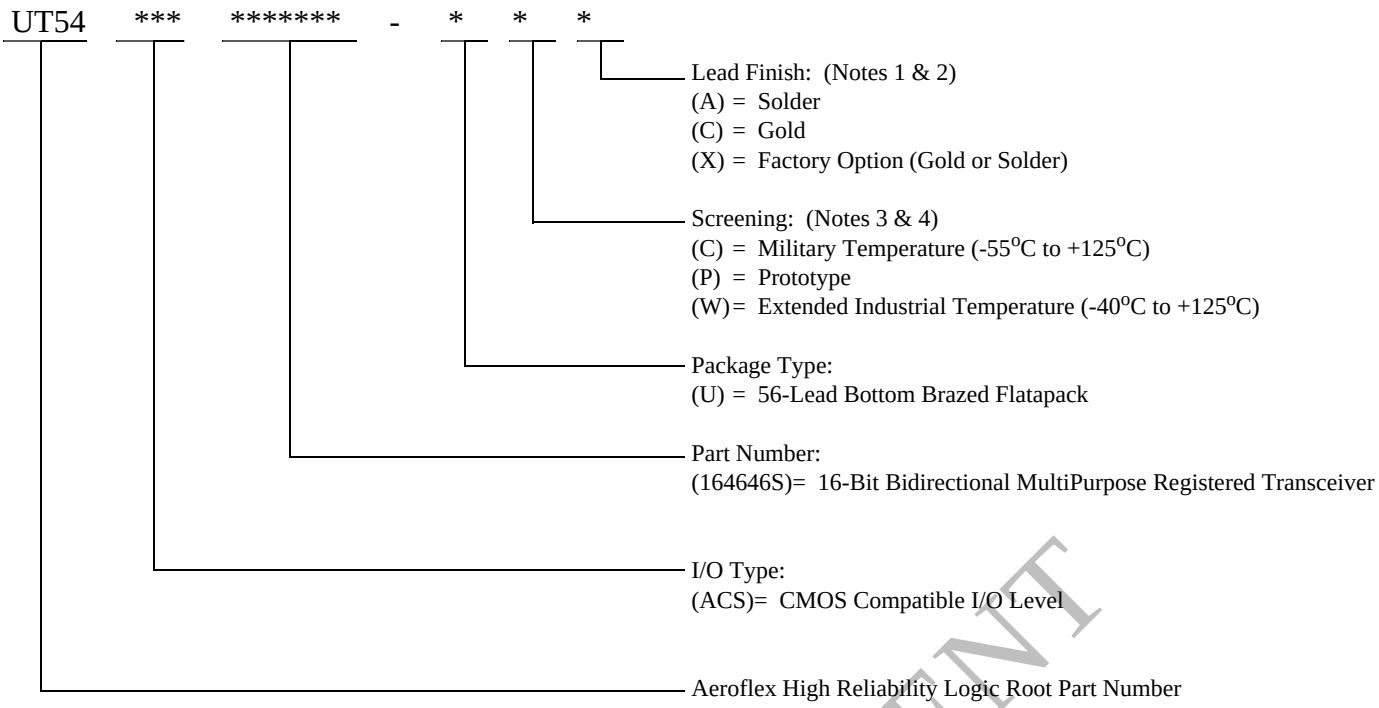


NOTES:
1. ALL EXPOSED METALIZED AREAS ARE GOLD PLATED 100 MICROINCHES OVER ELECTROPLATED NICKEL UNDERPLATING 100 MICROINCHES THICK PER MIL-PRF-38535.
2. LEAD FINISH IS IN ACCORDANCE WITH MIL-PRF-38535.
3. SEAL RING IS ELECTRICALLY CONNECTED TO VSS.
4. CERAMIC IS DARK ALUMINA.
5. LETTER DESIGNATIONS ARE TO CROSS-REFERENCE TO MIL-STD-1835.
6. LEAD TRUE POSITION TOLERANCE AND COPLANARITY ARE NOT MEASURED.

44256

ORDERING INFORMATION

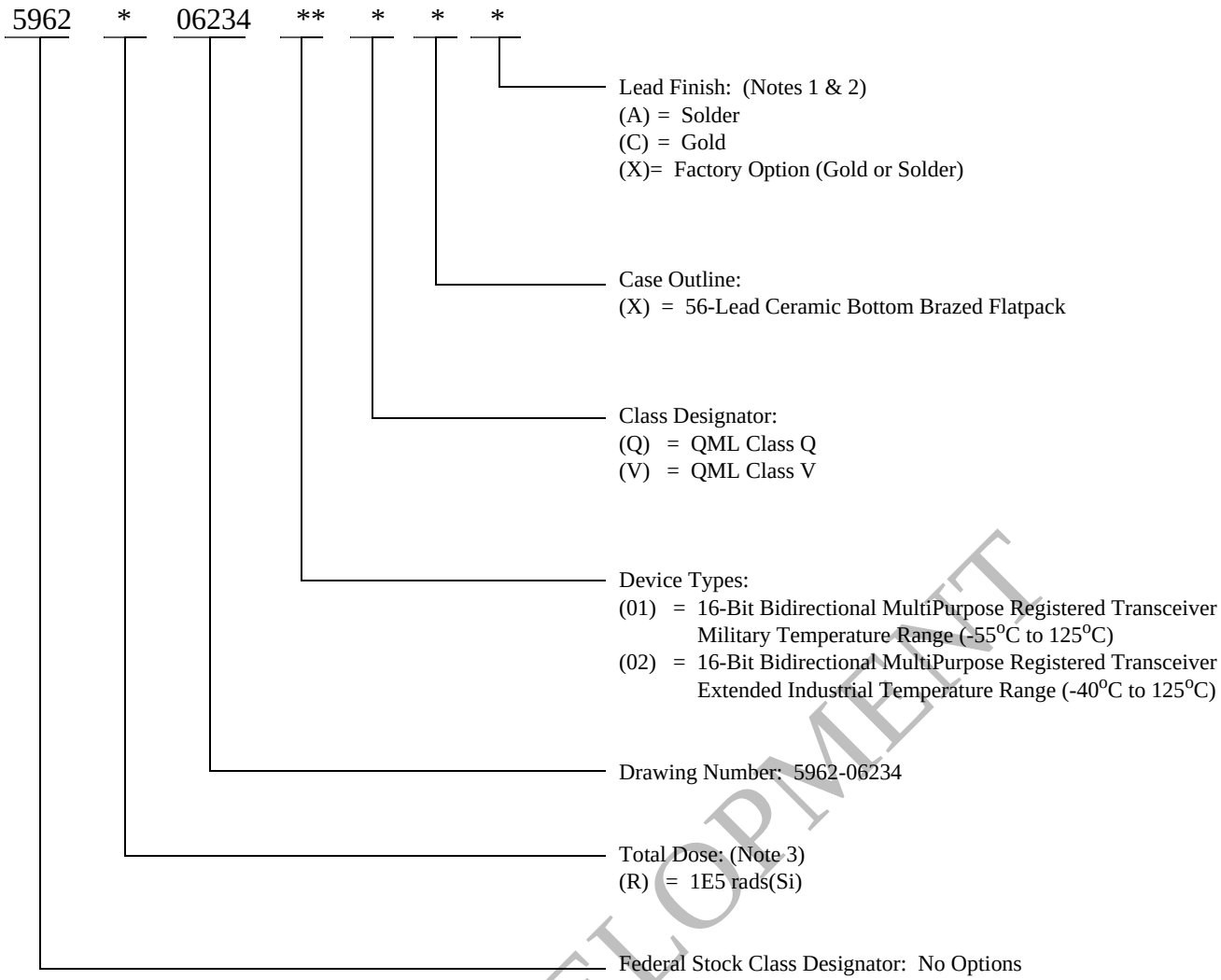
UT54ACS164646S



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are test at -55°C, room temp, and 125°C. Radiation neither tested nore guranteed.

UT54ACS164646S: SMD



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML-Q and QML-V are not available without radiation hardening.

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Fax: 719-594-8468

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Tel: 805-778-9229
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Tel: 949-362-2260
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AEROFLEX
A passion for performance.

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused

Aeroflex Colorado Springs Errata

Date: **May 19, 2006**

Part Number: **UT54ACS164646S MultiPurpose Transceiver**

Silicon Revision: **A**

Affected Date Codes: **All Revision A**

Data Sheet Specification:

DC ELECTRICAL CHARACTERISTICS [1]
(T_C = -55°C to +125°C for "C" screening and -40°C to +125°C for "W" screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
I_{CS}	Cold sparing input leakage current (any pin)	V_{IN} = 5.5 V_{DDB} = V_{DDA} = V_{SS} +/- 0.3 V	-1	5	µA
I_{WSA}	Warm sparing input leakage current (any pin)	V_{IN} = 5.5; V_{DDB} = 3V to 5.5V V_{DDA} = V_{SS} +/- 0.3 V	-1	5	µA
I_{WSB}	Warm sparing input leakage current (any pin)	V_{IN} = 5.5; V_{DDA} = 3V to 5.5V V_{DDB} = V_{SS} +/- 0.3 V	-1	5	µA

Errata Specification:

DC ELECTRICAL CHARACTERISTICS [1]
(T_C = -55°C to +125°C for "C" screening and -40°C to +125°C for "W" screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
I_{CS}	Cold sparing input leakage current (any pin)	V_{IN} = 5.5 V_{DDB} = V_{DDA} = V_{SS} +/- 0.3 V	-3	400	µA
I_{WSA}	Warm sparing input leakage current (any pin)	V_{IN} = 5.5; V_{DDB} = 3V to 5.5V V_{DDA} = V_{SS} +/- 0.3 V	-3	400	µA
I_{WSB}	Warm sparing input leakage current (any pin)	V_{IN} = 5.5; V_{DDA} = 3V to 5.5V V_{DDB} = V_{SS} +/- 0.3 V	-3	400	µA

Corrective Action, Rev B silicon 3Q2006

DC ELECTRICAL CHARACTERISTICS :[1]

(T_C = -55°C to +125°C for "C" screening and -40°C to +125°C for "W" screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
I_{CS}	Cold sparing input leakage current (any pin)	V_{IN} = 5.5 V_{DDB} = V_{DDA} = V_{SS} +/- 0.3 V	-1	5	µA
I_{WSA}	Warm sparing input leakage current (any pin)	V_{IN} = 5.5; V_{DDB} = 3V to 5.5V V_{DDA} = V_{SS} +/- 0.3 V	-1	5	µA
I_{WSB}	Warm sparing input leakage current (any pin)	V_{IN} = 5.5; V_{DDA} = 3V to 5.5V V_{DDB} = V_{SS} +/- 0.3 V	-1	5	µA