

# SN74CBTLV16235

## LOW-VOLTAGE 18-BIT 1-OF-2 FET MULTIPLEXER/DEMUTIPLEXER

SCDS060F – MARCH 1998 – REVISED OCTOBER 2003

- 4-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Break-Before-Make Feature

### description/ordering information

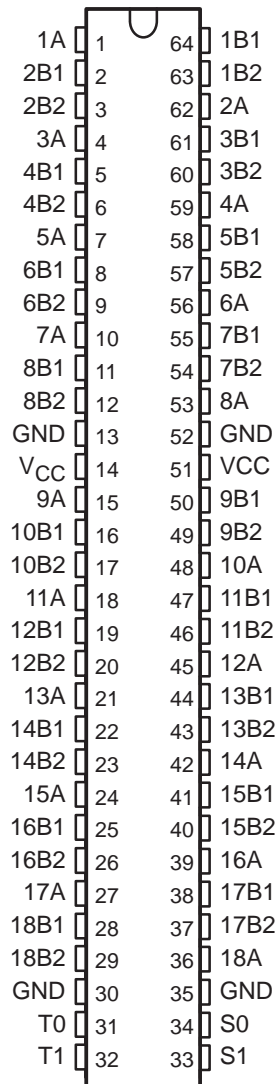
The SN74CBTLV16235 is an 18-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously.

The device is organized as a dual 9-bit 1-of-2 multiplexer/demultiplexer with separate control inputs. It can be used as two 9-bit multiplexers/demultiplexers or as one 18-bit multiplexer/demultiplexer. Two select (S0 and S1) inputs control the data flow. When the test (T0 and T1) inputs are asserted, port A is connected to both ports B1 and B2. The control inputs can be driven with a low-voltage TTL or an SSTL\_3 driver.

The SN74CBTLV16235 is specified by the break-before-make design to have no through current when switching directions.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

DGG PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG   Tape and reel	SN74CBTLV16235GR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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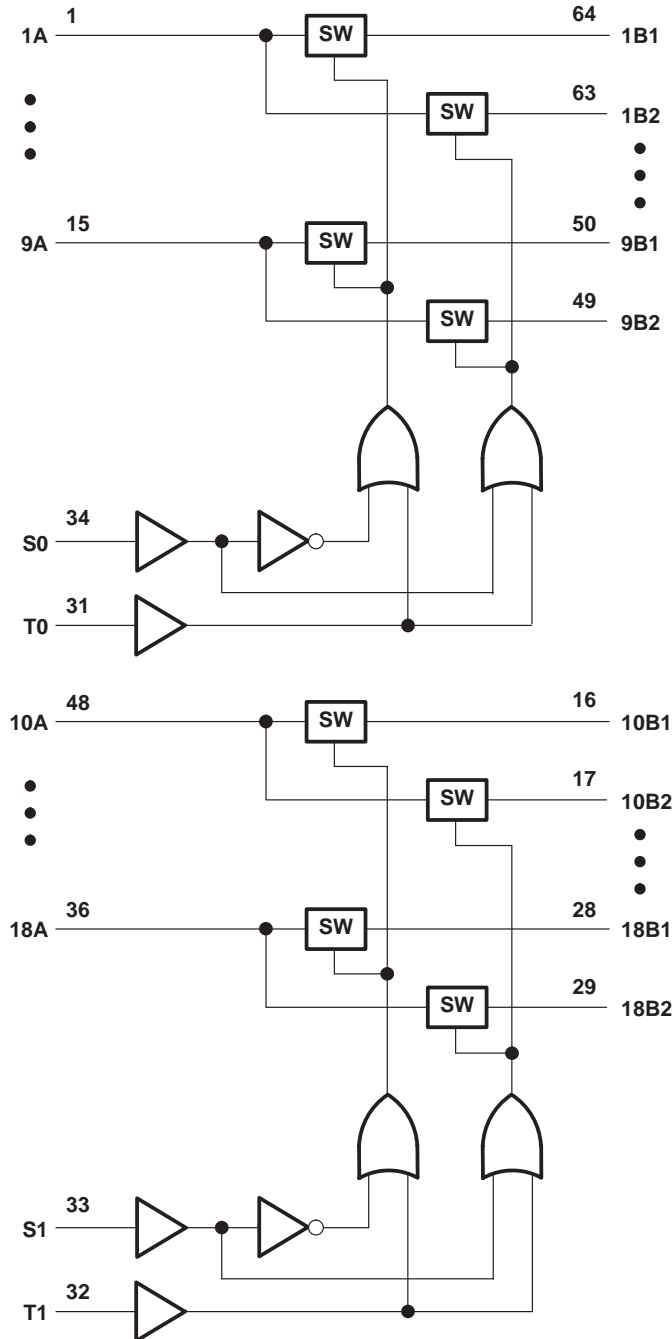
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**FUNCTION TABLE**  
(each 9-bit multiplexer/demultiplexer)

INPUTS		FUNCTION
T	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	A port = B1 port = B2 port

logic diagram (positive logic)



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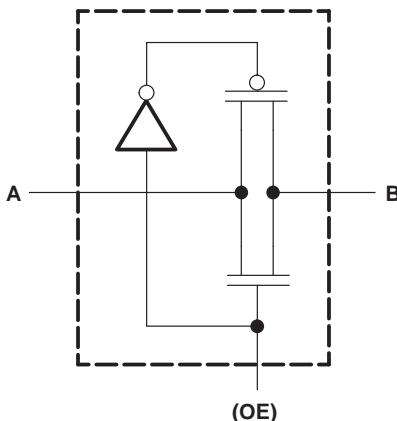
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## LOW-VOLTAGE 18-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

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simplified schematic, each FET switch



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	55°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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# SN74CBTLV16235

## LOW-VOLTAGE 18-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 3\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$I_I$		$V_{CC} = 3.6\text{ V}$ ,	$V_I = V_{CC}$ or GND			$\pm 5$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to $3.6\text{ V}$			10	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ ,	$I_O = 0$ , $V_I = V_{CC}$ or GND			10	$\mu\text{A}$
$\Delta I_{CC}‡$	Control input	$V_{CC} = 3.6\text{ V}$ ,	One input at $3\text{ V}$ , Other inputs at $V_{CC}$ or GND			300	$\mu\text{A}$
$C_i$	Control input	$V_I = 3\text{ V}$ or $0$					pF
$C_{io}(\text{OFF})$	A port	$V_O = 3\text{ V}$ or $0$					pF
	B port						
$r_{on}§$	$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$			$\Omega$	
			$I_I = 24\text{ mA}$				
		$V_I = 1.7\text{ V}$ ,	$I_I = 15\text{ mA}$				
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$				
			$I_I = 24\text{ mA}$				
		$V_I = 2.4\text{ V}$ ,	$I_I = 15\text{ mA}$				

† All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}¶$	A or B	B or A					ns
$t_{en}$	S	A or B					ns
$t_{dis}$	S	A or B					ns
$t_{en}$	T	A or B					ns
$t_{dis}$	T	A or B					ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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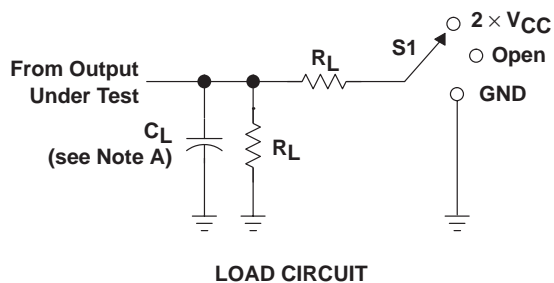


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## LOW-VOLTAGE 18-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

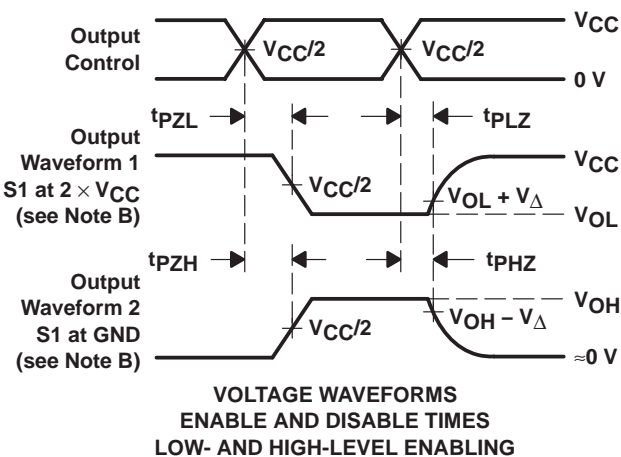
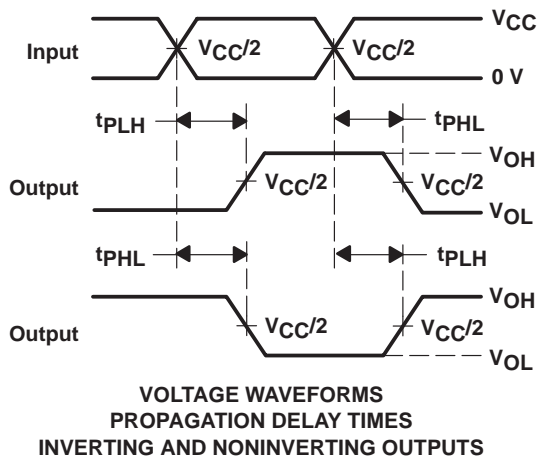
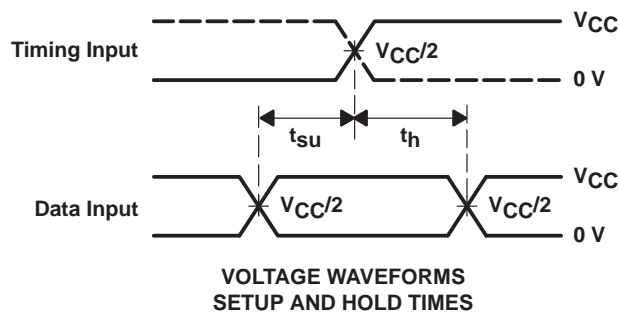
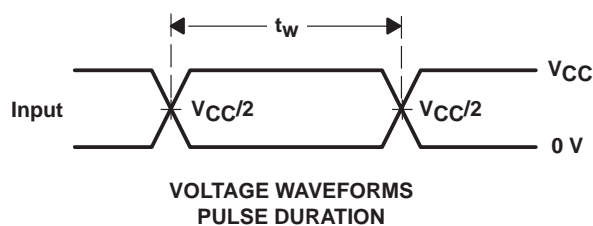
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### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 $\Omega$	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74CBTLV16235GR	PREVIEW	TSSOP	DGG	64	2000	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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