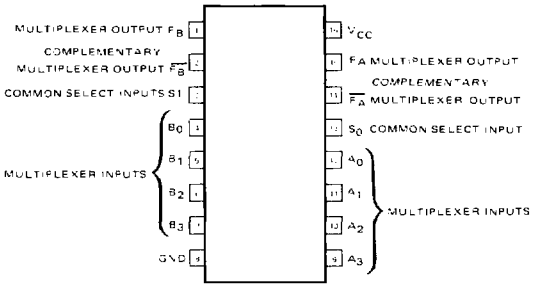
DUAL 4-INPUT MULTIPLEXER — 9309

SPEED/PACKAGE AVAILABILITY

S9309 F,W N9309 B,F

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	A_0	A_1	A_2	A_3	F_A	$\overline{F}_A$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	B_0	B_1	B_2	B_3	F_B	$\overline{F}_B$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = either high or low logic level

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				9309 C_L = 15pF			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
t_{PD+}	Turn off delay	S_0	Z_a		24 or 24	32 36	ns
t_{PD-}	Turn on delay				24 or 24	32 36	ns

Load circuit and typical waveforms are shown at the front of section.

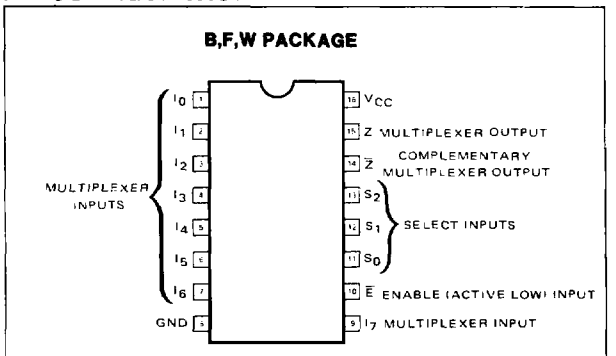
8-INPUT MULTIPLEXER — 9312

SPEED/PACKAGE AVAILABILITY

S9312 F,W N9312 B,F

PIN CONFIGURATION

B,F,W PACKAGE



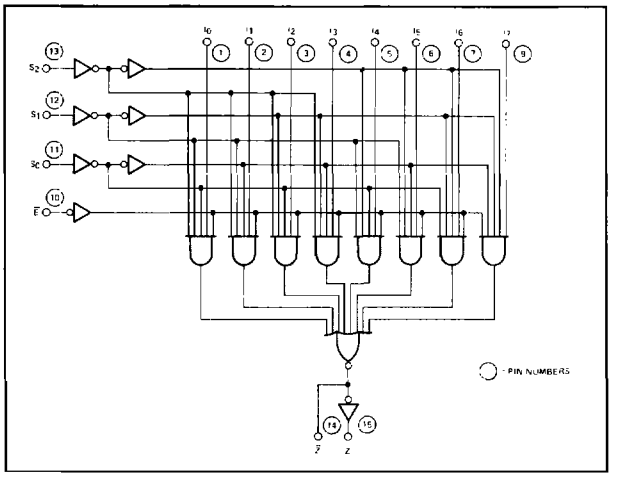
8-INPUT MULTIPLEXER — 9312

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = high voltage level
L = low voltage level
X = level does not affect output.

LOGIC DIAGRAM

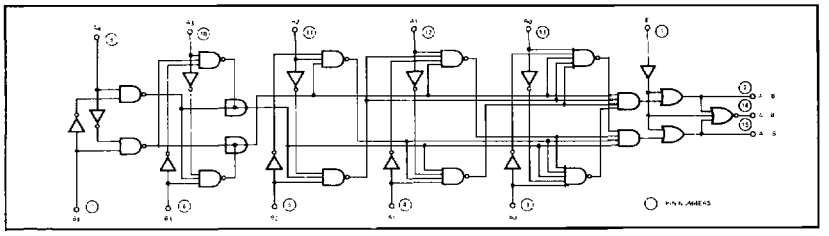


5-BIT COMPARATOR — 9324

SPEED/PACKAGE AVAILABILITY

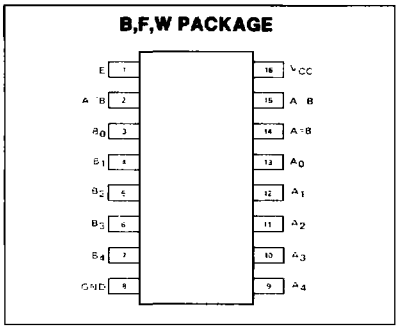
S9324 F,W N9324 B,F

LOGIC DIAGRAM



PIN CONFIGURATION

B,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				9324 C_L = 15pF R_L = 400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time							
t_{PLH}	Low-to-high	A_2	A>B		23	28	ns
t_{PHL}	High-to-low				19	23	
t_{PLH}	Low-to-high	A_2	A=B		40	45	
t_{PHL}	High-to-low				35	42	
t_{PLH}	Low-to-high	A_2	A<B		29	37	
t_{PHL}	High-to-low				24	29	
t_{PLH}	Low-to-high	$\overline{E}$	A=B		12	17	
t_{PHL}	High-to-low				10	16	

Load circuit and typical waveforms are shown at the front of section.

LOGIC

8-BIT COMPARATOR — 9324

TRUTH TABLE

$\overline{E}$	Ay	By	A<B	A>B	A=B
H	X	X	L	L	L
L	Word A=Word B		L	L	H
L	Word A>Word B		L	H	L
L	Word B>Word A		H	L	L

H = high voltage level
L = low voltage level
X = either high or low voltage level

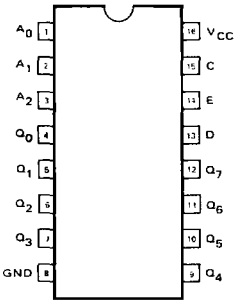
8-BIT ADDRESSABLE LATCH — 9334

SPEED/PACKAGE AVAILABILITY

S9334 F,W N9334 B

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

PRESENT OUTPUT STATES														
$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					ADDRESSABLE
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						LATCH
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

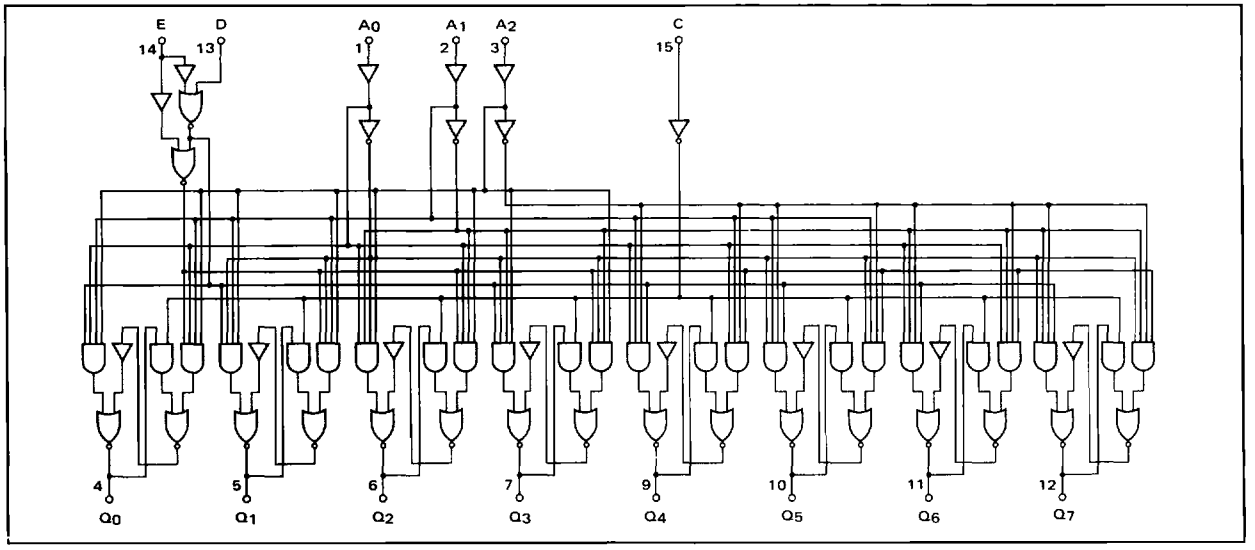
X = don't care condition
L = low voltage level
H = high voltage level
Q_{N-1} = previous output state

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				9334 C_L=15pF R_L=680Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time							
t_{PLH}	Low-to-high	Delay enable	Output		19	23	ns
t_{PHL}	High-to-low				16	24	
t_{PLH}	Low-to-high	Delay Data	Output		28	35	
t_{PHL}	High-to-low				16	24	
t_{PLH}	Low-to-high	Delay Address	Output			35	
t_{PHL}	High-to-low					35	
t_{PHL}	High-to-low	Delay Clear	Output		21	25	

Load circuit and typical waveforms are shown at the front of section.

LOGIC DIAGRAM

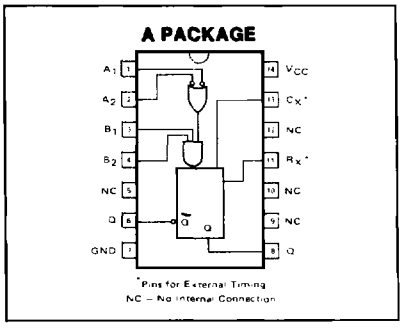


LOGIC

SPEED/PACKAGE AVAILABILITY

N9601 A,F

PIN CONFIGURATION



Load circuit and waveform shown at front of section.