Document No.	853–0623
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100155
Quad 2–Way Multiplexer–Latch

FEATURES

- **Typical propagation delay: 1.1ns**
- **Typical supply current ($-I_{EE}$): 93mA**

DESCRIPTION

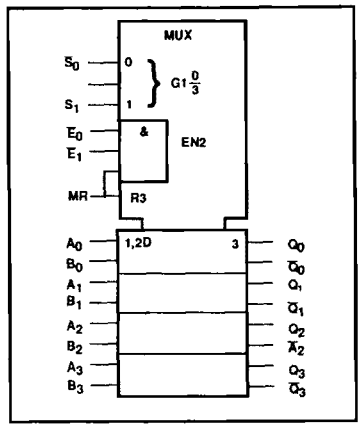
The 100155 is a multiplexer that switches one of two 4–bit inputs, A or B, through a latch, to the outputs (Q_n, $\overline{Q}_n$). This part can also perform an OR function on A and B. The select lines $\overline{S}_0$ and S_1 decide whether word A, word B, or A + B will be sent to the latch. When enables $\overline{E}_0$ and $\overline{E}_1$ are Low, the latch presents the selected input word to the outputs (Q_n, $\overline{Q}_n$). When either $\overline{E}_0$ or $\overline{E}_1$ go High, the data currently at the outputs are latched. If the Master Reset line (MR) is High, Q will be Low, and $\overline{Q}$ will be High regardless of the level of the other outputs.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_3$, $B_0 - B_3$	Data inputs
$\overline{E}_0$, $\overline{E}_1$	Enable inputs
$\overline{S}_0$, S_1	Data select inputs
MR	Master reset inputs
$Q_0 - Q_3$	True data outputs
$\overline{Q}_0 - \overline{Q}_3$	Complemetary data outputs

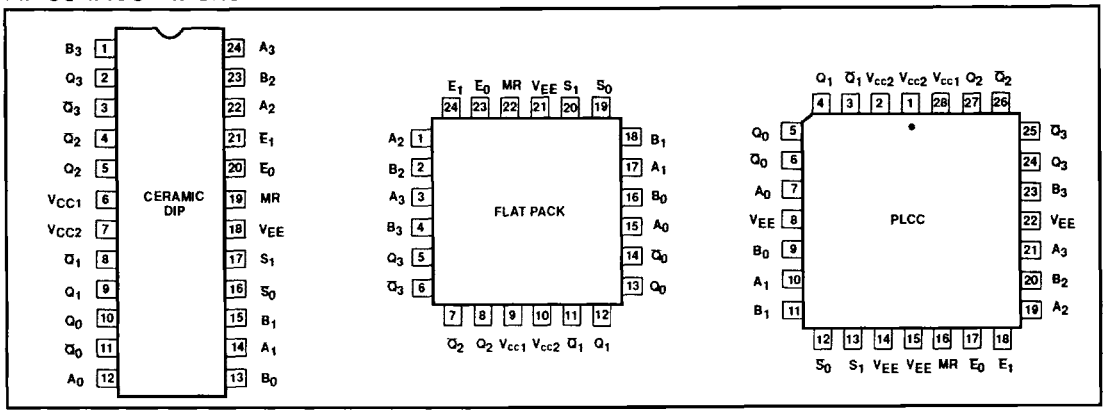
IEC/IEEE SYMBOL



ORDERING INFORMATION

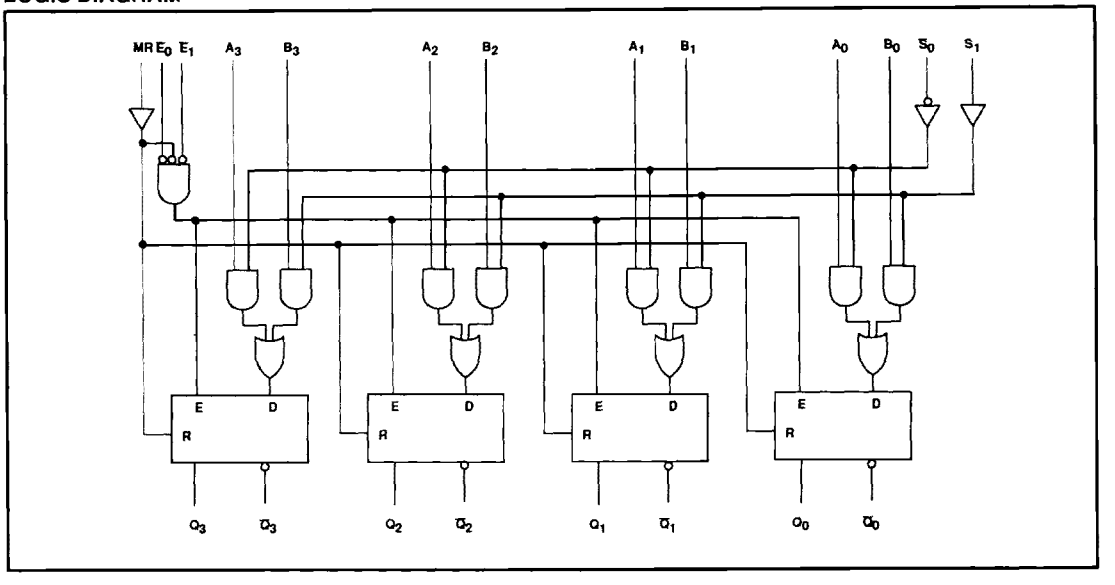
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100155F
24–Pin Ceramic Flat Pack	100155Y
28–Pin PLCC	100155A

PIN CONFIGURATIONS



Multiplexer–Latch | 100155

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS	
Reset	Enable		Select		Data			
MR	$\overline{E}_0$	$\overline{E}_1$	$\overline{S}_0$	S_1	A_n	B_n	Q_n	$\overline{Q}_n$
H	X	X	X	X	X	X	L	H
L	L	L	H	H	X	H	H	L
L	L	L	H	H	X	L	L	H
L	L	L	L	L	H	X	H	L
L	L	L	L	L	L	X	L	H
L	L	L	H	L	X	X	L	H
L	L	L	L	H	X	H	H	L
L	L	L	L	H	H	X	H	L
L	L	L	L	H	L	L	L	H
L	H	X	X	X	X	X	Latched*	Latched*
L	X	H	X	X	X	X	Latched*	Latched*

NOTES:
* = Signal level present on latch outputs just before rising transition of enable line is held on latch outputs.
H = High voltage level
L = Low voltage level
X = Don't care
NC = No change

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electyrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	$\overline{S}_0$, S_1		One input under test at V_{IHMAX}, other inputs at V_{ILMIN}.				220	µA
		$\overline{E}_0$, E_1	$\overline{S}_0$ at V_{ILMIN}., S_1 at V_{IHMAX}.					350	µA
		A_n, B_n						340	µA
		MR						430	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}, other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			66	93	133	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_n, $\overline{Q}_n$	Waveform 1	0.50 0.50	1.90 1.90	0.60 0.60	1.85 1.85	0.50 0.50	1.90 1.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 to Q_n, $\overline{Q}_n$		1.50 1.50	3.50 3.50	1.50 1.50	3.40 3.40	1.50 1.50	3.50 3.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n, $\overline{Q}_n$	Waveform 1,2	0.90 0.90	2.50 2.50	1.00 1.00	2.40 2.40	1.00 1.00	2.50 2.50	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	0.90 0.90	3.00 3.00	0.90 0.90	2.90 2.90	0.90 0.90	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1	0.60 0.60	2.20 2.20	0.60 0.60	2.10 2.10	0.45 0.45	2.20 2.20	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}_n$	Waveform 3	0.90		0.90		0.90		ns
t_h	Hold time, $\overline{E}_n$ to A_n, B_n		0.40		0.40		0.40		ns
t_s	Setup time, $\overline{S}_0$, S_1 to $\overline{E}_n$		2.40		2.40		2.70		ns
t_h	Hold time, $\overline{E}_n$ to $\overline{S}_0$, S_1		–0.6		–0.6		–0.6		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	1.50		1.50		1.50		ns
$t_w(H)$	Pulse width, MR	Waveform 2	2.50		2.50		2.50		ns
$t_w(L)$	Pulse width, $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_n, $\overline{Q}_n$	Waveform 1	0.50 0.50	1.90 1.90	0.60 0.60	1.85 1.85	0.50 0.50	1.90 1.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 to Q_n, $\overline{Q}_n$		1.50 1.50	3.50 3.50	1.50 1.50	3.40 3.40	1.50 1.50	3.50 3.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.90 0.90	2.50 2.50	1.00 1.00	2.40 2.40	1.00 1.00	2.50 2.50	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	0.90 0.90	3.00 3.00	0.90 0.90	2.90 2.90	0.90 0.90	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1	0.60 0.60	2.20 2.20	0.60 0.60	2.10 2.10	0.45 0.45	2.20 2.20	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}_n$	Waveform 3	0.90		0.90		0.90		ns
t_h	Hold time, $\overline{E}_n$ to A_n, B_n		0.40		0.40		0.40		ns
t_s	Setup time, $\overline{S}_0$, S_1 to $\overline{E}_n$		2.40		2.40		2.70		ns
t_h	Hold time, $\overline{E}_n$ to $\overline{S}_0$, S_1		–0.6		–0.6		–0.6		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	1.50		1.50		1.50		ns
$t_w(H)$	Pulse width, MR	Waveform 2	2.50		2.50		2.50		ns
$t_w(L)$	Pulse width, $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_n, $\overline{Q}_n$	Waveform 1	0.50 0.50	1.70 1.70	0.60 0.60	1.65 1.65	0.50 0.50	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 to Q_n, $\overline{Q}_n$		1.50 1.50	3.30 3.30	1.50 1.50	3.20 3.20	1.50 1.50	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.90 0.90	2.30 2.30	1.00 1.00	2.20 2.20	1.00 1.00	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	0.90 0.90	2.80 2.80	0.90 0.90	2.70 2.70	0.90 0.90	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1	0.60 0.60	2.20 2.20	0.60 0.60	2.10 2.10	0.45 0.45	2.20 2.20	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}_n$	Waveform 3	0.80		0.80		0.80		ns
t_h	Hold time, $\overline{E}_n$ to A_n, B_n		0.30		0.30		0.30		ns
t_s	Setup time, $\overline{S}_0$, S_1 to $\overline{E}_n$		2.60		2.60		2.60		ns
t_h	Hold time, $\overline{E}_n$ to $\overline{S}_0$, S_1		–0.8		–0.8		–0.8		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	1.40		1.40		1.40		ns
$t_w(H)$	Pulse width, MR	Waveform 2	2.50		2.50		2.50		ns
$t_w(L)$	Pulse width, $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

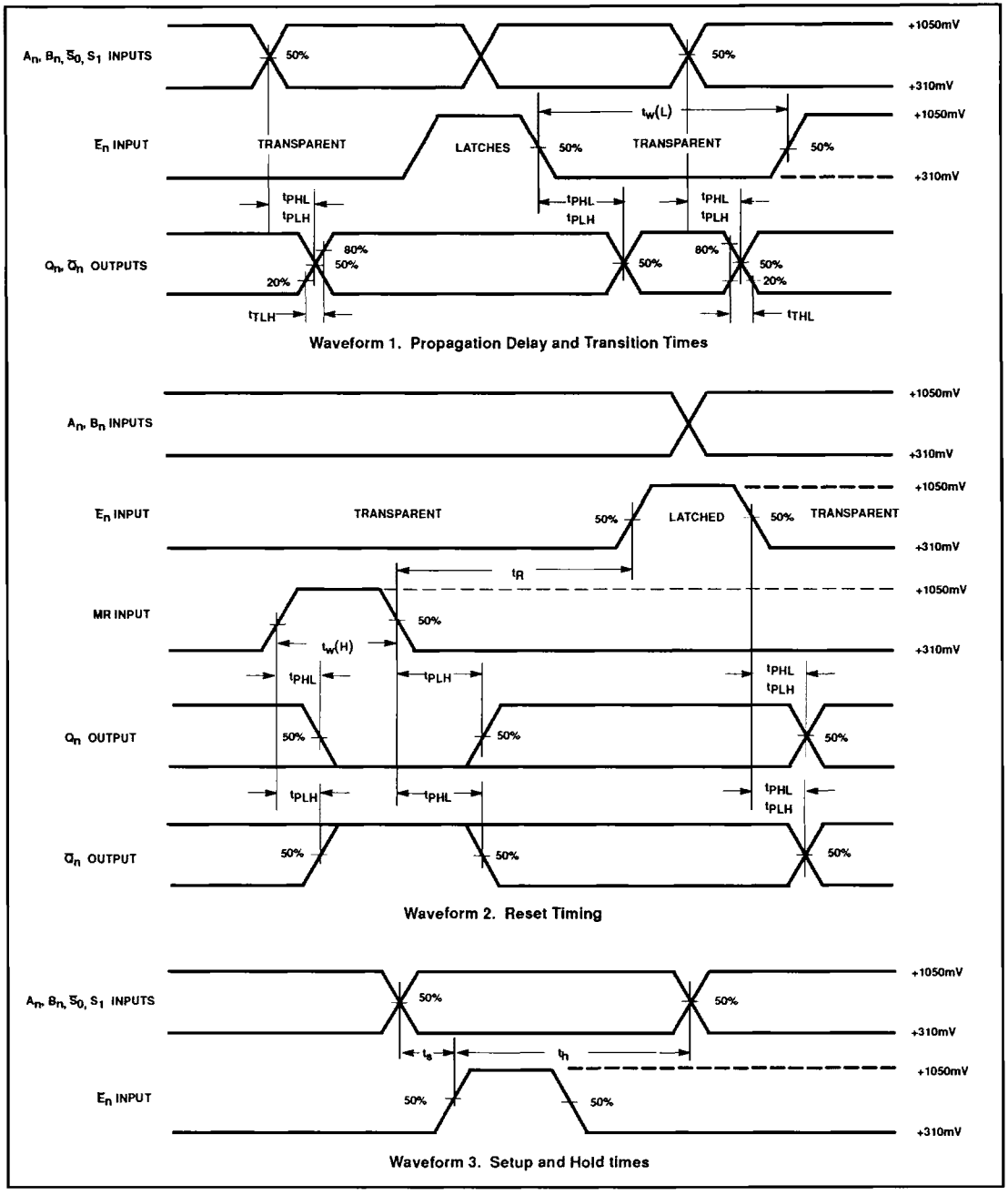
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_n, $\overline{Q}_n$	Waveform 1	0.50 0.50	1.70 1.70	0.60 0.60	1.65 1.65	0.50 0.50	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 to Q_n, $\overline{Q}_n$		1.50 1.50	3.30 3.30	1.50 1.50	3.20 3.20	1.50 1.50	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.90 0.90	2.30 2.30	1.00 1.00	2.20 2.20	1.00 1.00	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	0.90 0.90	2.80 2.80	0.90 0.90	2.70 2.70	0.90 0.90	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1	0.60 0.60	2.20 2.20	0.60 0.60	2.10 2.10	0.45 0.45	2.20 2.20	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}_n$	Waveform 3	0.80		0.80		0.80		ns
t_h	Hold time, $\overline{E}_n$ to A_n, B_n		0.30		0.30		0.30		ns
t_s	Setup time, $\overline{S}_0$, S_1 to $\overline{E}_n$		2.60		2.60		2.60		ns
t_h	Hold time, $\overline{E}_n$ to $\overline{S}_0$, S_1		–0.8		–0.8		–0.8		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	1.40		1.40		1.40		ns
$t_w(H)$	Pulse width, MR	Waveform 2	2.50		2.50		2.50		ns
$t_w(L)$	Pulse width, $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Waveform 2. Reset Timing

Waveform 3. Setup and Hold times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.