LOW POWER SCHOTTKY INTEGRATED CIRCUITS

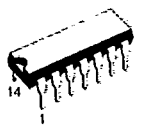
T54LS03
T74LS03

67C 16006 D T-43-15

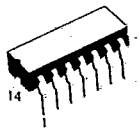
QUAD 2-INPUT NAND GATE

DESCRIPTION

The T54LS03/T74LS03 is a high speed QUAD 2-INPUT NAND GATE fabricated in LOW POWER SCHOTTKY technology.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

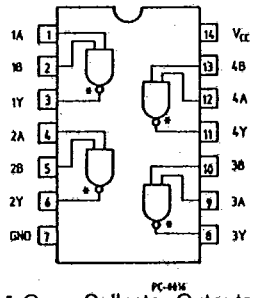
C1
Plastic Chip Carrier

ORDERING NUMBERS:

T54LS03 D2	T74LS03 C1
T74LS03 D1	T74LS03 M1
T74LS03 B1	

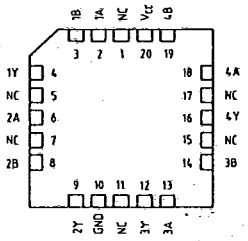
PIN CONNECTION (top view)

DUAL IN LINE



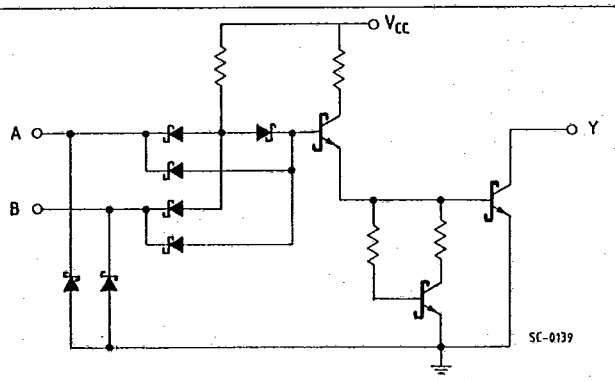
* Open Collector Outputs

CHIP CARRIER



NC = No Internal Connection

SCHEMATIC



T54LS03
T74LS03

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	X	H
X	L	H
H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS03D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS03XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Typ.	Max.	Test Conditions (Note 1)		Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
I_{OH}	Output HIGH Current	54,74			100	V_{CC} = MIN, V_{OH} = 5.5V, V_{IN} = V_{IL}		μA
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = 2.0V	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V		μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{CCH}	Supply Current HIGH				1.6	V_{CC} = MAX, V_{IN} = 0V		mA
I_{CCL}	Supply Current LOW				4.4	V_{CC} = MAX, Inputs Open		mA

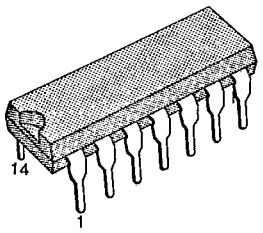
AC CHARACTERISTICS: T_A = 25°C (See page 576 for AC test circuit and waveforms)

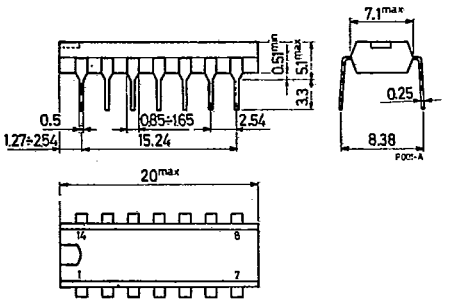
Symbol	Parameter	Limits Min.	Typ.	Max.	Test Conditions	Units
t_{PLH}	Turn Off Delay, Input to Output		17	32	V_{CC} = 5.0V C_L = 15pF, R_L = 2.0kΩ	ns
t_{PHL}	Turn On Delay, Input to Output		15	28		ns

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Typical values are at V_{CC} = 5.0V, T_A = 25°C.

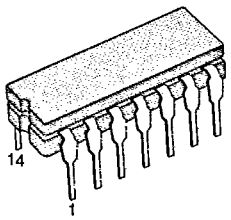
Packages

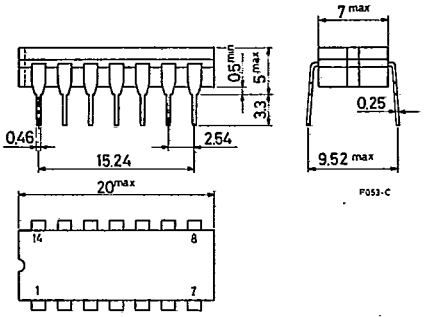
14-LEAD PLASTIC DIP





14-LEAD CERAMIC DIP





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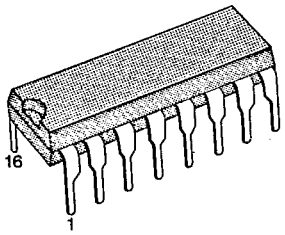
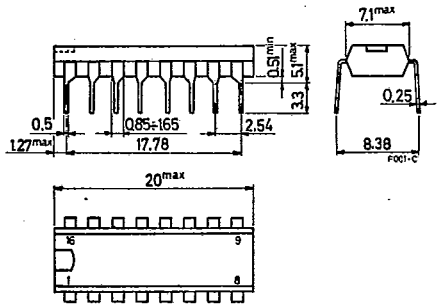
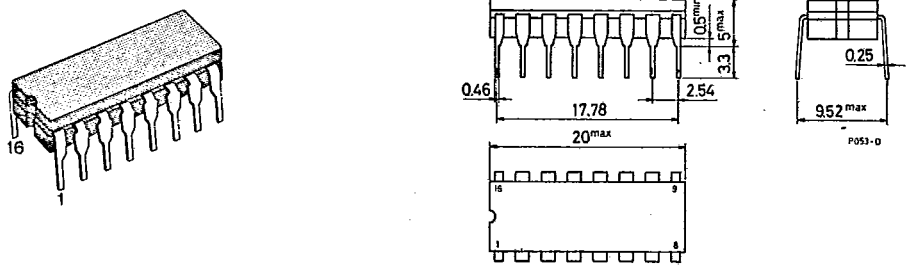




Packages

16-LEAD CERAMIC DIP



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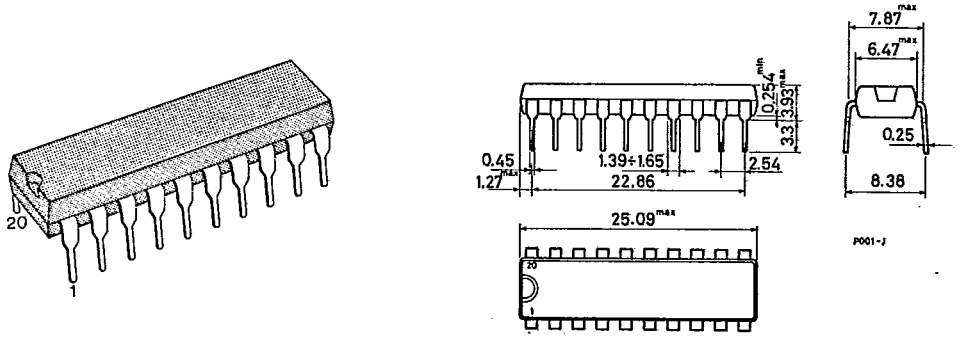

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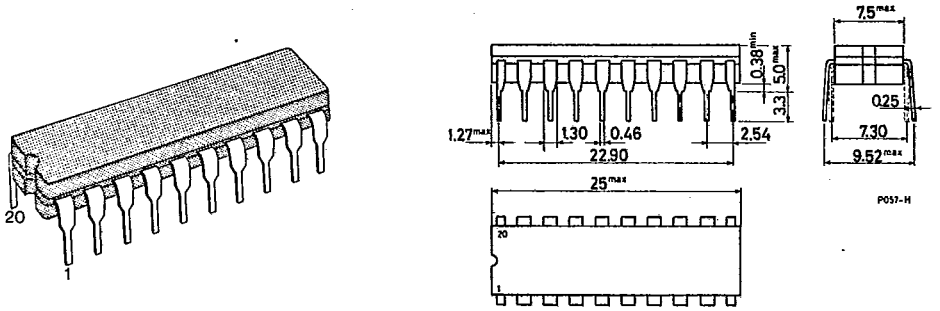
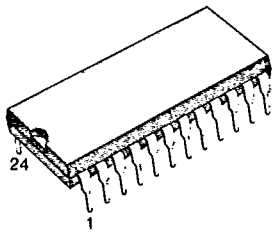
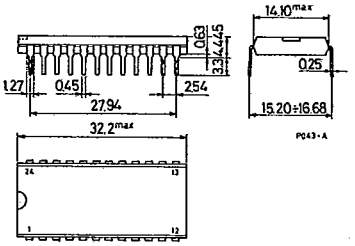


Packages

24-LEAD PLASTIC DIP





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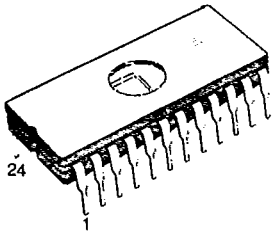
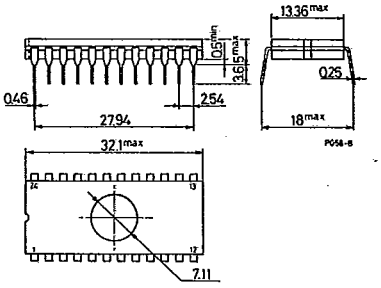
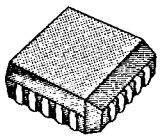
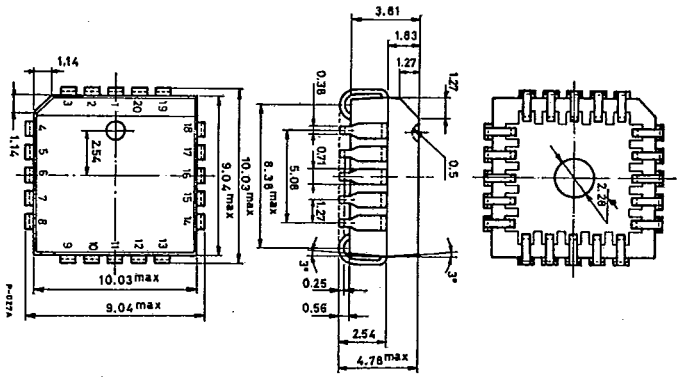




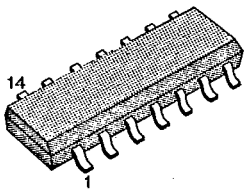
CHIP CARRIER 20 LEAD PLASTIC

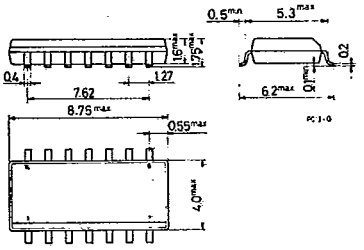




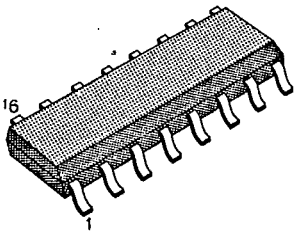
Packages

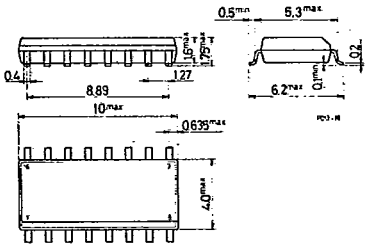
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.