



# CY74FCT16543T CY74FCT162543T

## 16-Bit Latched Transceivers

### Features

- Low power, pin-compatible replacement for ABT functions
- FCT-E speed at 3.4 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to +85°C
- V<sub>CC</sub> = 5V ± 10%

#### CY74FCT16543T Features:

- 64 mA sink current, 32 mA source current
- Typical V<sub>OLP</sub> (ground bounce) < 1.0V at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

#### CY74FCT162543T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V<sub>OLP</sub> (ground bounce) < 0.6V at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

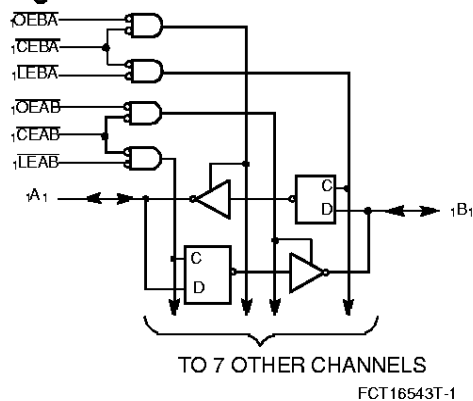
### Functional Description

The CY74FCT16543T and CY74FCT162543T are 16-bit, high-speed, low power latched transceivers that are organized as two independent 8-bit D-type latched transceivers containing two sets of eight D-type latches with separate Latch Enable (LEAB, LEAB) and Output Enable (OEAB, OEAB) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B input Enable (CEAB) must be LOW in order to enter data from A or to take data from B as indicated in the truth table. With CEAB LOW, a LOW signal on the A-to-B Latch Enable (LEAB) makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With CEAB and OEAB both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses OEAB, LEAB, and OEAB inputs flow-through pinout and small shrink packaging and in simplifying board design. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

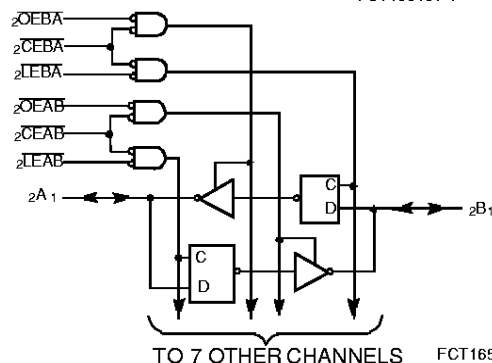
The CY74FCT16543T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162543T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162543T is ideal for driving transmission lines.

### Logic Block Diagrams



FCT16543T-1



FCT16543T-2

### Pin Configuration

#### Top View SSOP/TSSOP

1OEAB	1	56	1OEBA
1LEAB	2	55	1LEBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A <sub>1</sub>	5	52	1B <sub>1</sub>
1A <sub>2</sub>	6	51	1B <sub>2</sub>
V <sub>CC</sub>	7	50	V <sub>CC</sub>
1A <sub>3</sub>	8	49	1B <sub>3</sub>
1A <sub>4</sub>	9	48	1B <sub>4</sub>
1A <sub>5</sub>	10	47	1B <sub>5</sub>
GND	11	46	GND
1A <sub>6</sub>	12	45	1B <sub>6</sub>
1A <sub>7</sub>	13	44	1B <sub>7</sub>
1A <sub>8</sub>	14	43	1B <sub>8</sub>
2A <sub>1</sub>	15	42	2B <sub>1</sub>
2A <sub>2</sub>	16	41	2B <sub>2</sub>
2A <sub>3</sub>	17	40	2B <sub>3</sub>
GND	18	39	GND
2A <sub>4</sub>	19	38	2B <sub>4</sub>
2A <sub>5</sub>	20	37	2B <sub>5</sub>
2A <sub>6</sub>	21	36	2B <sub>6</sub>
V <sub>CC</sub>	22	35	V <sub>CC</sub>
2A <sub>7</sub>	23	34	2B <sub>7</sub>
2A <sub>8</sub>	24	33	2B <sub>8</sub>
GND	25	32	GND
2CEAB	26	31	2CEBA
2LEAB	27	30	2LEBA
2OEAB	28	29	2OEBA

FCT16543T-3



**Pin Description**

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

**Function Table<sup>[1]</sup>**

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A to B	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs <sup>[2]</sup>

**Maximum Ratings<sup>[3, 4]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l -55°C to +125°C  
 Ambient Temperature with Power Applied ..... Com'l -55°C to +125°C  
 DC Input Voltage ..... -0.5V to +7.0V  
 DC Output Voltage ..... -0.5V to +7.0V  
 DC Output Current (Maximum Sink Current/Pin) ..... -60 to +120 mA

Power Dissipation ..... 1.0W  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[6]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>			±1	µA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>I</sub> =GND			±1	µA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	µA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	µA
I <sub>OS</sub>	Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[8]</sup>			±1	µA

**Notes:**

1. A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .
2. Data prior to  $\overline{LEAB}$  LOW-to-HIGH Transition  
 H = HIGH Voltage Level. L = LOW Voltage Level.  
 X = Don't Care. Z = High Impedance.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
5. Typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = +25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
8. Tested at +25°C.



### Output Drive Characteristics for CY74FCT16543T

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

### Output Drive Characteristics for CY74FCT162543T

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[7]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[7]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA		0.3	0.55	V

### Capacitance<sup>[6]</sup> (T<sub>A</sub> = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

### Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit	
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max. V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	5	500	μA	
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max. V <sub>IN</sub> =3.4V <sup>[9]</sup>	0.5	1.5	mA	
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[10]</sup>	V <sub>CC</sub> =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND	60	100	μA/MHz	
I <sub>C</sub>	Total Power Supply Current <sup>[11]</sup>	V <sub>CC</sub> =Max., f <sub>1</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OE=GND	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	0.6	1.5	mA
			V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	0.9	2.3	mA
		V <sub>CC</sub> =Max., f <sub>1</sub> =2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, OE=GND	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	2.4	4.5 <sup>[12]</sup>	mA
			V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	6.4	16.5 <sup>[12]</sup>	mA

#### Notes:

9. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11.
  - I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>
  - I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub>D<sub>H</sub>N<sub>T</sub> + I<sub>CCD</sub>(f<sub>0</sub>/2 + f<sub>1</sub>N<sub>1</sub>)
  - I<sub>CC</sub> = Quiescent Current with CMOS input levels
  - ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)
  - D<sub>H</sub> = Duty Cycle for TTL inputs HIGH
  - N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>
  - I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)
  - f<sub>0</sub> = Clock frequency for registered devices, otherwise zero
  - f<sub>1</sub> = Input signal frequency
  - N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>
 All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.



**Switching Characteristics** Over the Operating Range<sup>[13]</sup>

Parameter	Description	CY74FCT16543T CY74FCT162543T		CY74FCT16543AT CY74FCT162543AT		Unit	Fig. No. <sup>[14]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode A to B or B to A	1.5	8.5	1.5	6.5	ns	1, 3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to A, LEAB to B	1.5	12.5	1.5	8.0	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	1.5	12.0	1.5	9.0	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	1.5	9.0	1.5	7.5	ns	1, 7, 8
t <sub>SU</sub>	Set-up Time HIGH or LOW A or B to LEAB or LEBA	2.0	—	2.0	—	ns	4
t <sub>H</sub>	Hold Time HIGH or LOW A or B to LEAB or LEBA	2.0	—	2.0	—	ns	4
t <sub>W</sub>	LEBA or LEAB Pulse Width LOW	4.0	—	4.0	—	ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[15]</sup>	—	0.5	—	0.5	ns	—

Parameter	Description	CY74FCT16543CT CY74FCT162543CT		CY74FCT16543ET CY74FCT162543ET		Unit	Fig. No. <sup>[14]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode A to B or B to A	1.5	5.1	1.5	3.4	ns	1, 3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to A, LEAB to B	1.5	5.6	1.5	3.7	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	1.5	7.8	1.5	4.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	1.5	6.5	1.5	4.0	ns	1, 7, 8
t <sub>SU</sub>	Set-up Time HIGH or LOW A or B to LEAB or LEBA	2.0	—	1.0	—	ns	4
t <sub>H</sub>	Hold Time HIGH or LOW A or B to LEAB or LEBA	2.0	—	1.0	—	ns	4
t <sub>W</sub>	LEBA or LEAB Pulse Width LOW	4.0	—	3.0	—	ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[15]</sup>	—	0.5	—	0.5	ns	—

**Notes:**

- 13. Minimum limits are guaranteed but not tested on Propagation Delays.
- 14. See "Parameter Measurement Information" in the General Information section.
- 15. Skew between any two outputs of the same package switching in the same directional. This parameter is guaranteed by design.



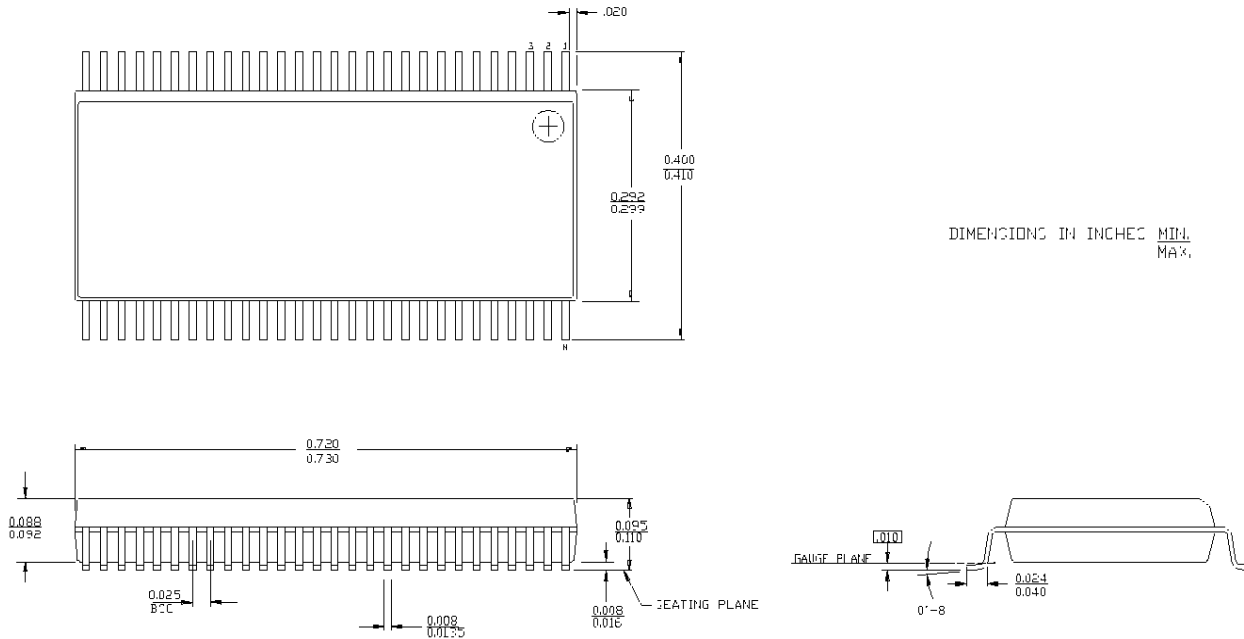
**Ordering Information CY74FCT16543**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.4	CY74FCT16543ETPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16543ETPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT16543CTPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16543CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT16543ATPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16543ATPVC	O56	56-Lead (300-Mil) SSOP	
8.5	CY74FCT16543TPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16543TPVC	O56	56-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT162543**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.4	CY74FCT162543ETPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162543ETPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162543CTPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162543CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT162543ATPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162543ATPVC	O56	56-Lead (300-Mil) SSOP	
8.5	CY74FCT162543TPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162543TPVC	O56	56-Lead (300-Mil) SSOP	

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**Package Diagrams**
**56-Lead Shrunken Small Outline Package O56**

**56-Lead Thin Shrunken Small Outline Package Z56**
