CY74FCT163652

16-Bit Registered Transceiver

Features

- **5V tolerant Inputs and Outputs**
- **24 mA balanced drive outputs**
- **Low power, pin-compatible replacement for LCX, LPT, LVC, LVCH & LVT families**
- **FCT-C speed at 5.4 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial temperature range of −40°C to +85°C**
- **V_{CC} = 2.7V to 3.6V**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 3.3V, T_A= 25°C**

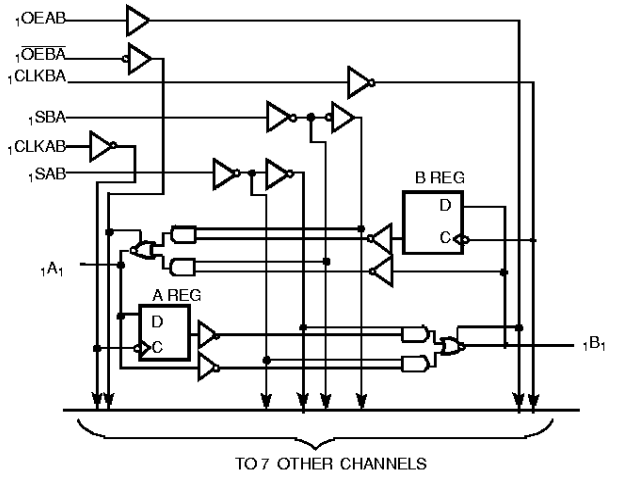
Functional Description

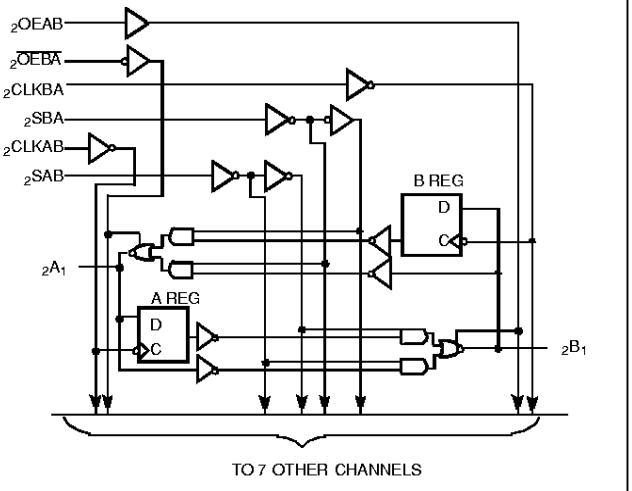
The CY74FCT163652 is a 16-bit, high-speed, low-power, registered transceiver that is organized as two independent 8-bit bus transceivers with three-state D-type registers and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. OEAB and $\overline{OEBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CLKAB or CLKBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CY74FCT163652 has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The inputs and outputs were designed to be capable of being driven by 5.0V buses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power-off disable feature enabling them to be used in applications requiring live insertion.

Logic Block Diagrams

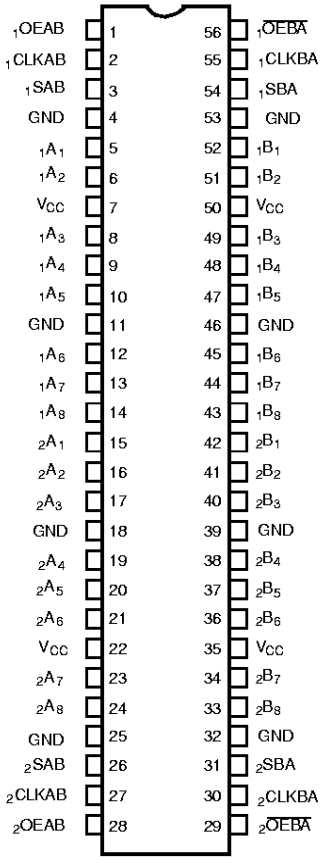




Pin Configuration

SSOP/TSSOP

Top View



Pin Description

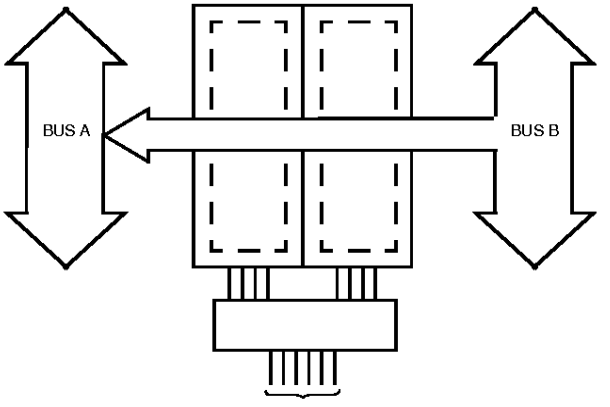
Name	Description
A	Data Register A Inputs, Data Register B Outputs
B	Data Register B Inputs, Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

Function Table[1]

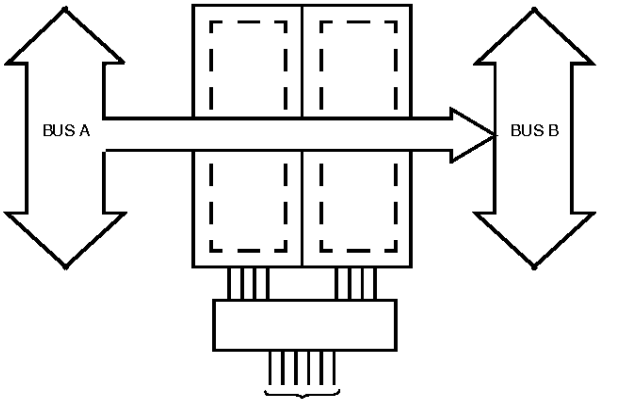
Inputs						Data I/O[2]		
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A	B	Operation or Function
L L	H H	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	↓ ↓	H or L ↓	X X[3]	X X	Input Input	Unspecified[2] Output	Store A, Hold B Store A in Both Registers
L L	X L	H or L ↓	↓ ↓	X X	X X[3]	Unspecified[2]	Input Input	Hold A, Store B Store B in both Registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes:

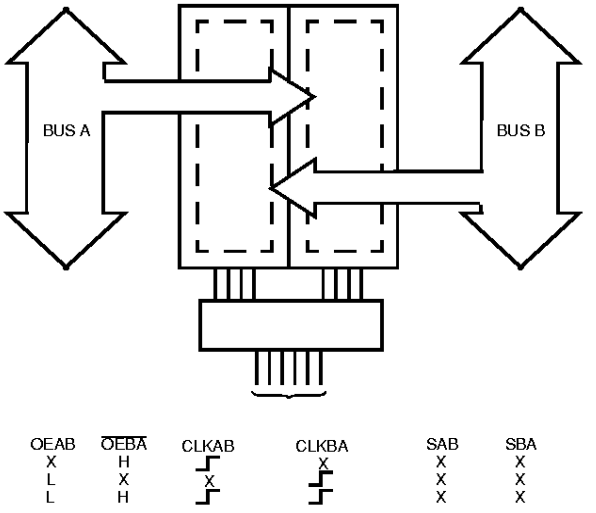
1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ↓ = LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
3. Select control=L; clocks can occur simultaneously.
   Select control=H; clocks must be staggered to load both registers.



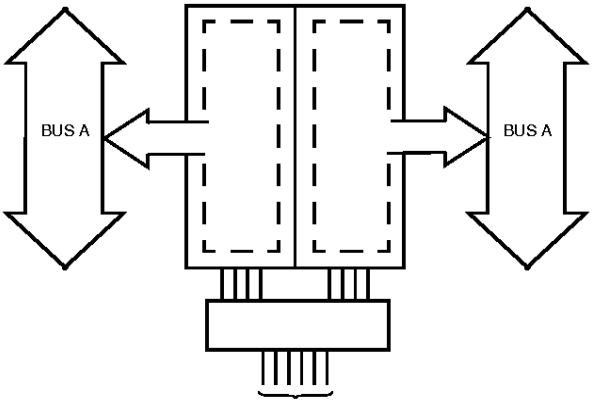
Real-Time Transfer
Bus B to Bus A



Real-Time Transfer
Bus A to Bus B



Storage from
A and/or B



Transfer Stored Data
to A and/or B

Maximum Ratings[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage Range ..... 0.5V to +4.6V

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... –60 to +120 mA

Power Dissipation..... 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	–40°C to +85°C	2.7V to 3.6V

Note:

4. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Condition	Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage	All Inputs	2.0		5.5	V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=5.5V			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=5.5V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=GND			±1	µA
I_{ODL}	Output LOW Current[7]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	50	90	200	mA
I_{ODH}	Output HIGH Current[7]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–36	–60	–110	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}= –0.1 mA	V_{CC}–0.2			V
		V_{CC}=3.0V, I_{OH}= –8 mA	2.4[8]	3.0		
		V_{CC}=3.0V, I_{OH}= –24 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}= 0.1mA			0.2	V
		V_{CC}=Min., I_{OL}= 24 mA		0.3	0.5	
I_{OS}	Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=GND	–60	–135	–240	mA
I_{OFF}	Power-Off Disable[7]	V_{CC}=0V, V_{OUT}≤4.5V			±100	µA

Capacitance[6] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

5. Typical values are at V_{CC}=3.3V, +25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametrics tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
8. V_{OH}=V_{CC}–0.6V at rated current.

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$ $V_{IN} \ge V_{CC}-0.2V$	0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	$V_{IN}=V_{CC}-0.6V$[9]	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., Outputs Open $\overline{OEAB}$=$\overline{OEAB}$=GND One Input Toggling 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	50	75	µA/MHz
I_C	Total Power Supply Current[11]	V_{CC}=Max., Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle $\overline{OEAB}$=$\overline{OEBA}$=GND One-Bit Toggling, f_1=5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.5	0.8	mA
			$V_{IN}=V_{CC}-0.6V$ or V_{IN}=GND	0.5	0.8	mA
		V_{CC}=Max., Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle $\overline{OEAB}$=$\overline{OEBA}$=GND Sixteen Bits Toggling f_1=2.5 MHz, 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	2.5	3.8[12]	mA
			$V_{IN}=V_{CC}-0.6V$ or V_{IN}=GND	2.6	4.1[12]	mA

Notes:

9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0 N_C/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    N_C = Number of clock inputs changing at f_1
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range[13,14]

Parameter	Description	CY74FCT163652A		CY74FCT163652C		Unit	Fig. No.[15]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	6.3	1.5	5.4	ns	1, 3
t_{PZH} t_{PHL}	Output Enable Time OEAB or $\overline{OEBA}$ to Bus	1.5	9.8	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time OEAB or $\overline{OEBA}$ to Bus	1.5	6.3	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus	1.5	7.7	1.5	6.2	ns	1, 5
t_{SU}	Set-Up time HIGH or LOW Bus to Clock	2.0	—	2.0	—	ns	4
t_H	Hold Time HIGH or LOW Bus to Clock	1.5	—	1.5	—	ns	4
t_W	Clock Pulse Width HIGH or LOW	5.0	—	5.0	—	ns	5
$t_{SK(O)}$	Output Skew[16]	—	0.5	—	0.5	ns	

Ordering Information CY74FCT163652

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT163652CPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163652CPVC	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT163652APAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163652APVC	O56	56-Lead (300-Mil) SSOP	

Notes:
13. Minimum limits are guaranteed, but not tested, on propagation delays.
14. For V_{CC} =2.7, propagation delay, output enable and output disable times should be degraded by 20%.
15. See "Parameter Measurement Information" in the General Information section.
16. Skew between any two outputs of the same package switching in the same direction. This parameter guaranteed by design.

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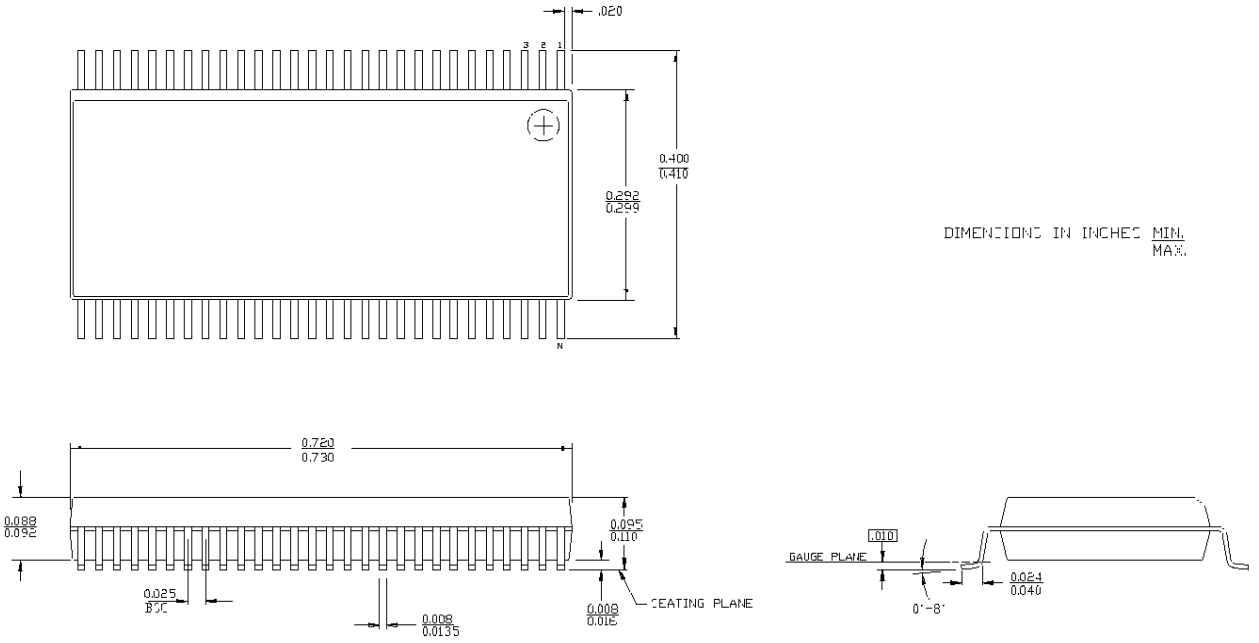
Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56