FAST CMOS 16-BIT LATCHED TRANSCEIVER

IDT54/74FCT162543AT/CT

FEATURES:

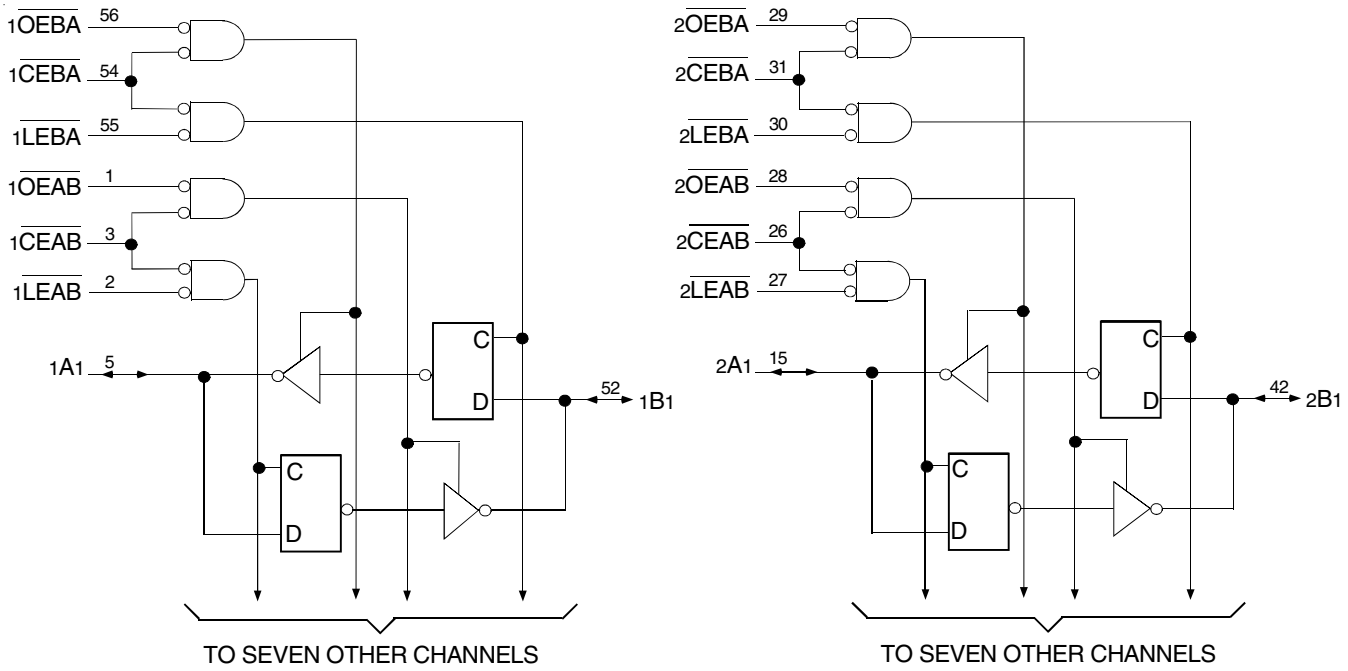
- **0.5 MICRON CMOS Technology**
- **High-speed, low-power CMOS replacement for ABT functions**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Low input and output leakage ≤1µA (max.)**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **V_{CC} = 5V ±10%**
- **Balanced Output Drivers:**
  - *±24mA (industrial)*
  - *±16mA (military)*
- **Reduced system switching noise**
- **Typical VOLP (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**
- **Available in the following packages:**
  - *Industrial: SSOP, TSSOP, TVSOP*
  - *Military: CERPACK*

DESCRIPTION:

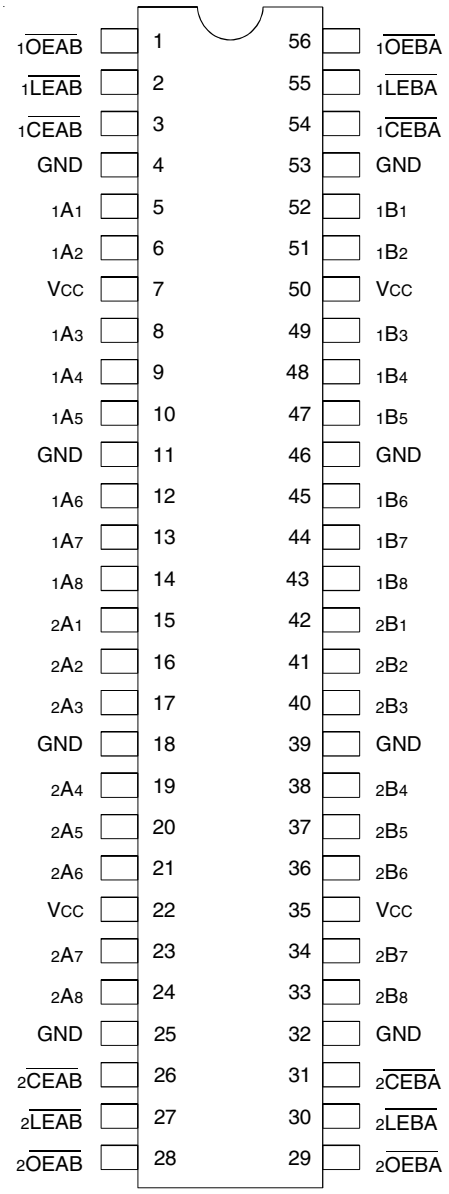
The FCT162543T 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable ($xCEAB$) must be low in order to enter data from the A port or to output data from the B port. $xLEAB$ controls the latch function. When $xLEAB$ is low, the latches are transparent. A subsequent low-to-high transition of $xLEAB$ signal puts the A latches in the storage mode. $xOEAB$ performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using $xCEBA$, $xLEBA$, and $xOEBA$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162543T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162543T is a plug-in replacement for the FCT16543T and 54/74ABT16543 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP/ CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
x$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
x$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
x$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
x$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
x$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
x$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to 7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Output and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(1, 2)

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
x$\overline{CEAB}$	x$\overline{LEAB}$	x$\overline{OEAB}$	xAx to xBx	xBx
H	X	X	Storing	Z
X	H	X	Storing	X
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs
L	L	H	Transparent	Z
L	H	H	Storing	Z

NOTES:
1. * Before x$\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedence
2. A-to-B data flow shown; B-to-A flow control is the same, except using x$\overline{CEBA}$, x$\overline{LEBA}$ and x$\overline{OEBA}$.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	5	500	µA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL I_{OH} = –24mA IND	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = 16mA MIL I_{OH} = 24mA IND	—	0.3	0.55	V

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND x$\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND x$\overline{CEBA}$ = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEBA}$ and x$\overline{OEAB}$ = GND x$\overline{CEBA}$ = V_{CC} Sixteen Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

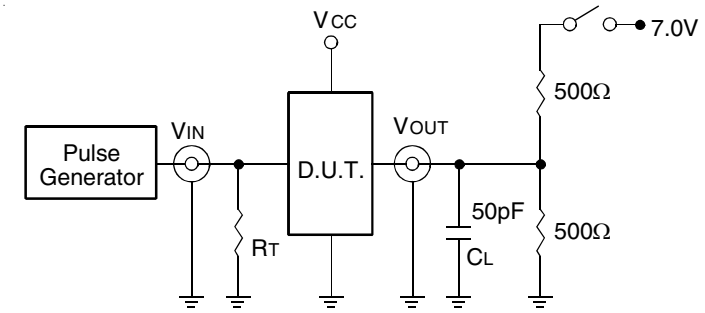
NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

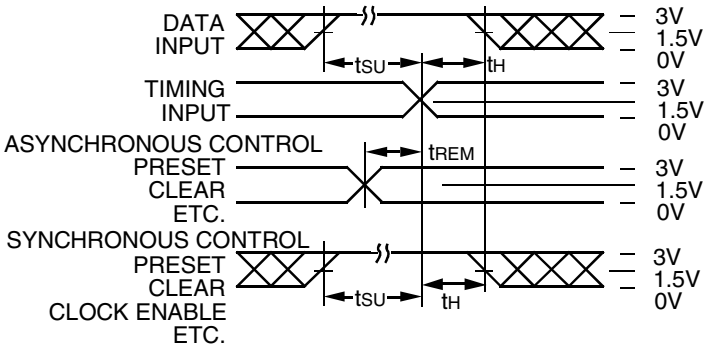
Symbol	Parameter	Condition[1]	FCT162543AT				FCT162543CT				Unit
			Ind.		Mil.		Ind.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.5	1.5	3.5	1.5	6.1	ns
t_{PLH} t_{PHL}	Propagation Delay x$\overline{LEBA}$ to xAx, x$\overline{LEAB}$ to xBx		1.5	8	1.5	9	1.5	4.1	1.5	8	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx		1.5	9	1.5	10	1.5	4.8	1.5	9	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx		1.5	7.5	1.5	8.5	1.5	4	1.5	7.5	ns
t_{SU}	Set-up Time HIGH or LOW xAx or xBx to x$\overline{LEAB}$ or x$\overline{LEBA}$		2	—	2	—	1	—	2	—	ns
t_H	Hold Time HIGH or LOW xAx or xBx to x$\overline{LEAB}$ or x$\overline{LEBA}$		2	—	2	—	1	—	2	—	ns
t_W	x$\overline{LEBA}$ or x$\overline{LEAB}$ Pulse Width LOW		4	—	5	—	3[4]	—	5	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

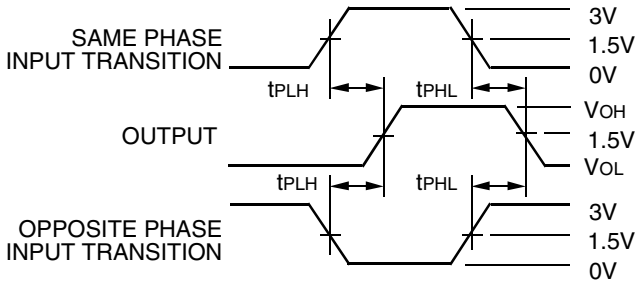
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



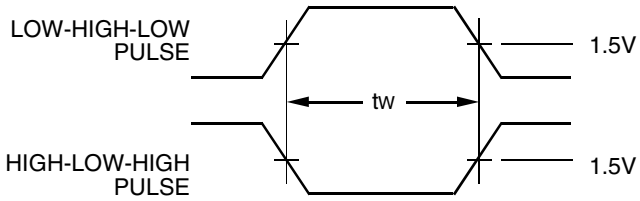
Propagation Delay

SWITCH POSITION

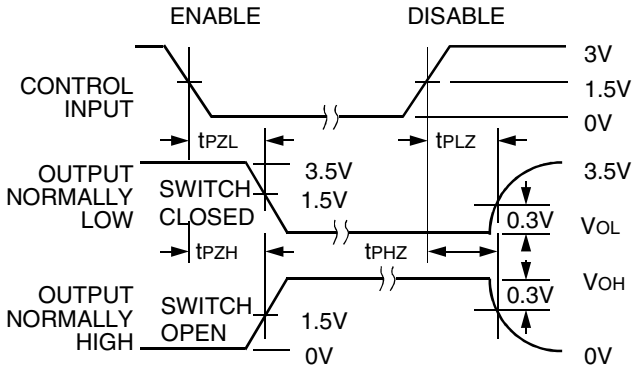
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

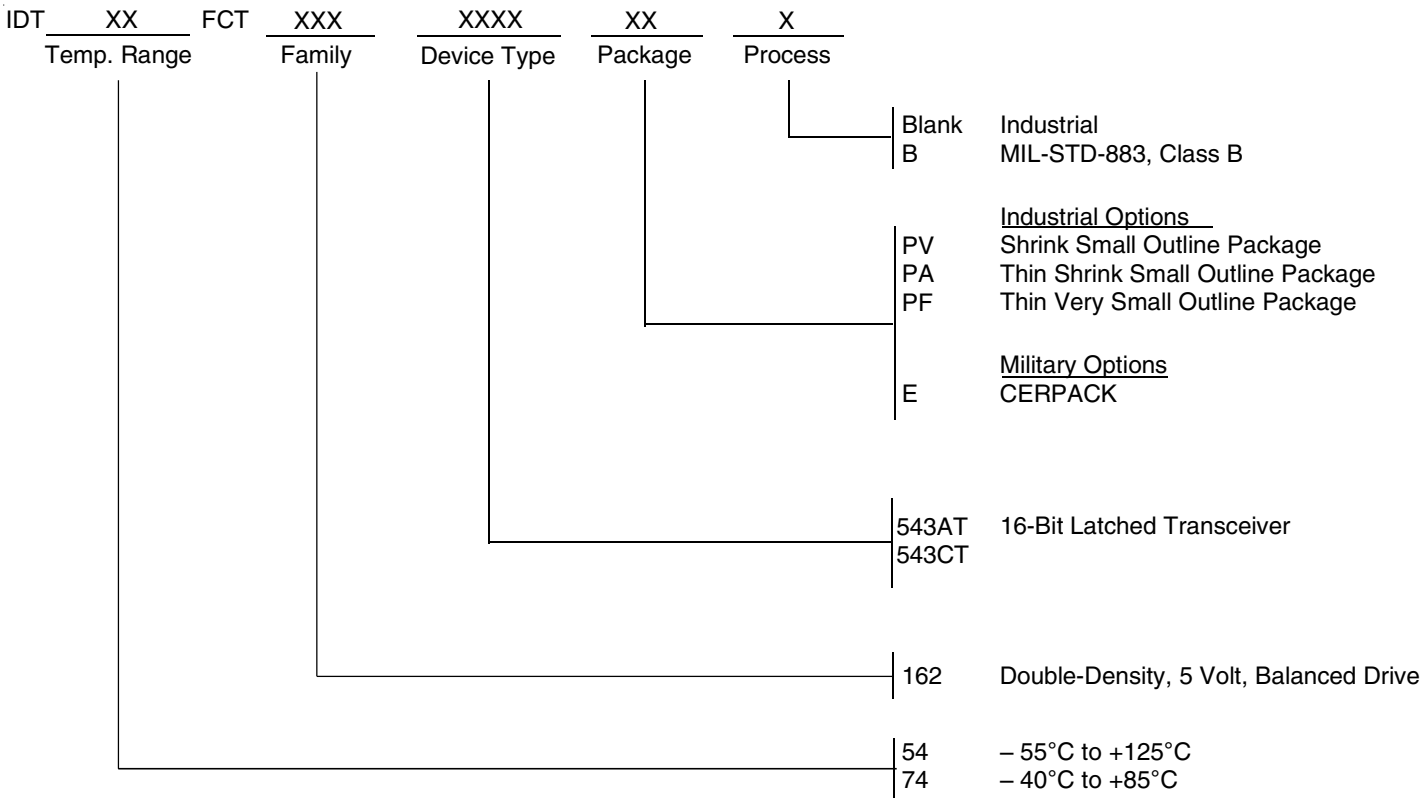


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

3/28/2002 Removed standard speed grade

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459