To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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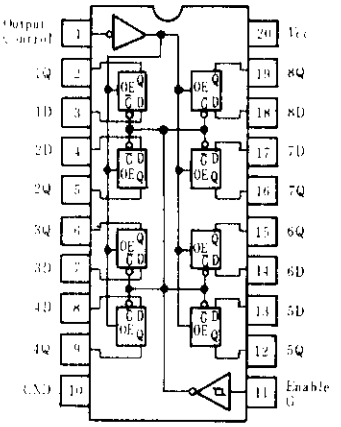
HD74LS373 ●Octal D-type Transparent Latches (with three-state outputs)

The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

■PIN ARRANGEMENT



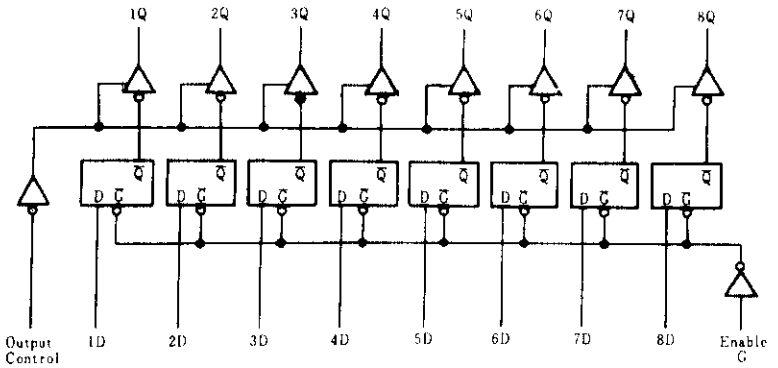
(Top View)

■FUNCTION TABLE

Inputs			Output
Output control	Enable G	D	Q
L	H	H	H
L	H	L	L
L	L	×	Q_0
H	×	×	Z

Notes: H = high level, L = low level, X = irrelevant
Q_0 = level of Q before the indicated steady-state input conditions were established.
Z = off (high-impedance) state of a three-state output

■BLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output voltage		V_{OH}	—	—	5.5	V
Output current		I_{OH}	—	—	−2.6	mA
		I_{OL}	—	—	24	mA
Enable pulse width	"H" level	t_w	15	—	—	ns
	"L" level		15	—	—	
Data setup time		t_{su}	5↓	—	—	ns
Data hold time		t_h	25↓	—	—	ns

Note) ↓ : The arrow indicates the falling edge of clock pulse.

■ELECTRICAL CHARACTERISTICS (Ta=−20～+75°C)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	—	—	V
	V_{IL}	Data inputs		—	—	0.7	V
		G, Output control inputs		—	—	0.8	
Output voltage	V_{OH}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=$V_{IL\ max}$, I_{OH}=−2.6mA		2.4	—	—	V
	V_{OL}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=$V_{IL\ max}$	I_{OL}=12mA	—	—	0.4	V
			I_{OL}=24mA	—	—	0.5	
Off-state output current	I_{OZH}	V_{CC}=5.25V, V_{IH}=2V	V_O=2.7V	—	—	20	μA
	I_{OZL}		V_O=0.4V	—	—	−20	
Input current	I_{IH}	V_{CC}=5.25V, V_I=2.7V		—	—	20	μA
	I_{IL}	V_{CC}=5.25V, V_I=0.4V		—	—	−0.4	mA
	I_I	V_{CC}=5.25V, V_I=7V		—	—	0.1	mA
Short-circuit output current	I_{OS}	V_{CC}=5.25V		−30	—	−130	mA
Supply current	I_{CC}	V_{CC}=5.25V, V_I=4.5V (Output control)		—	24	40	mA
Input clamp voltage	V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA		—	—	−1.5	V

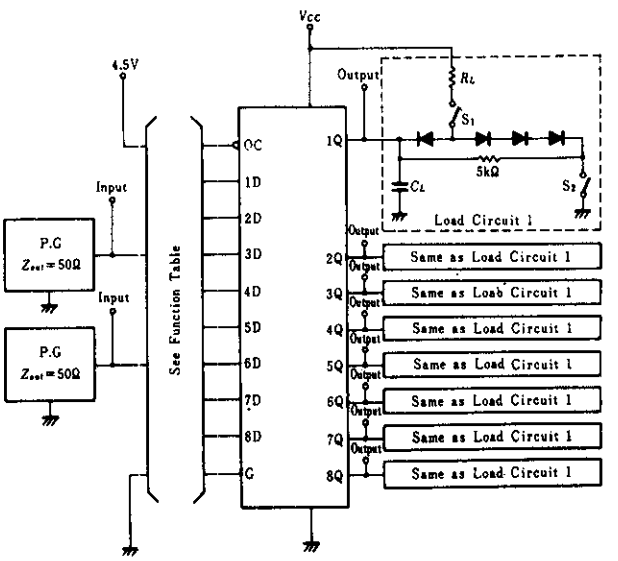
* V_{CC}=5V, Ta=25°C

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	D	Q	C_L=45pF, R_L=667Ω	—	12	18	ns
	t_{PHL}				—	12	18	
	t_{PLH}	G	Q		—	20	30	
	t_{PHL}				—	18	30	
Output enable time	t_{ZH}	OC	Q		—	15	28	
	t_{ZL}				—	25	36	
Output disable time	t_{HZ}	OC	Q	C_L=5pF, R_L=667Ω	—	12	20	
	t_{LZ}				—	15	25	

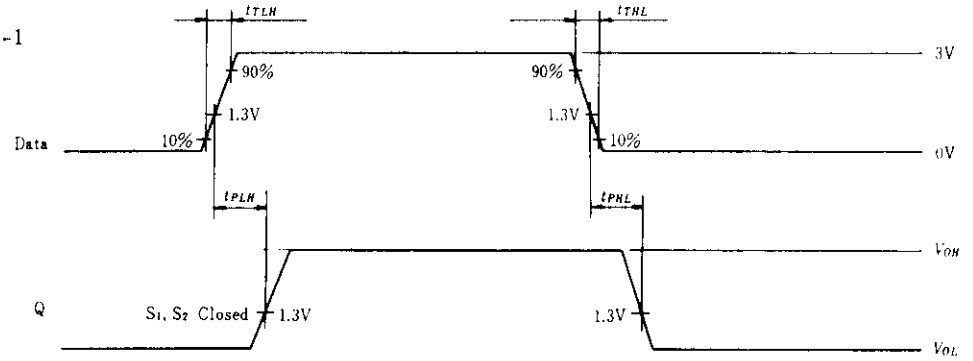
■TESTING METHOD

Test Circuit



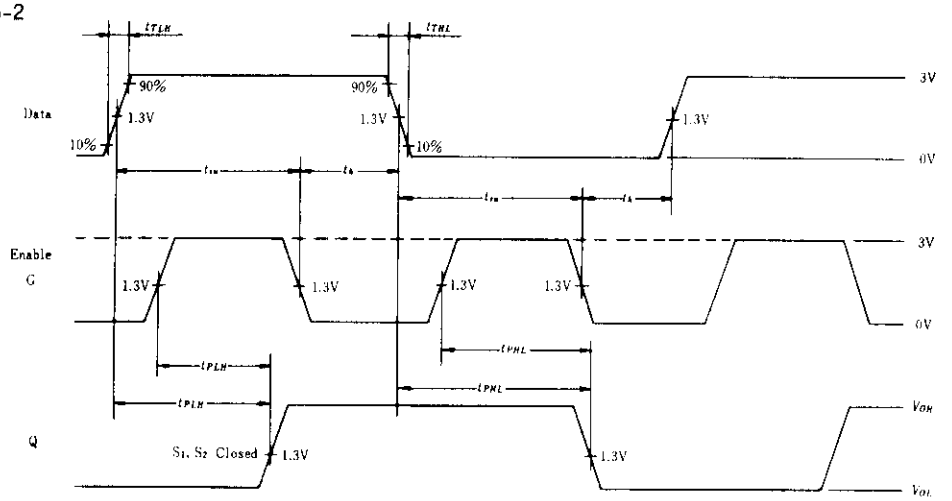
Notes: 1. C_L includes probe jig capacitance.
2. All diodes are 1S2074 (H).

Waveform-1



Notes: Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle 50%

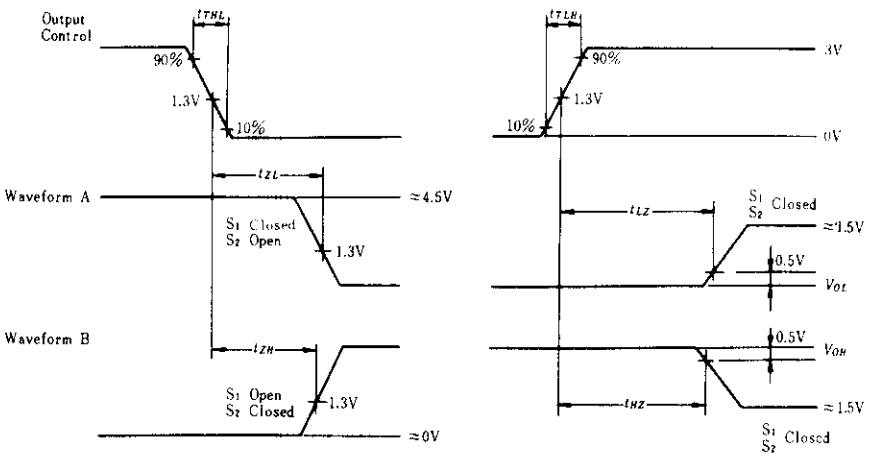
Waveform-2



Note: Enable input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz

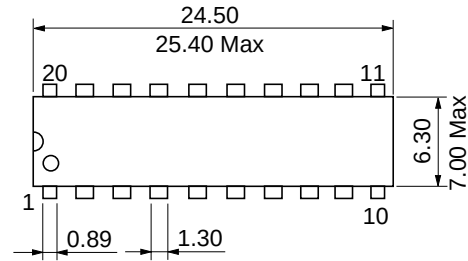
Data input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, G input is high.

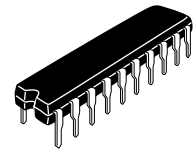
Waveform-3

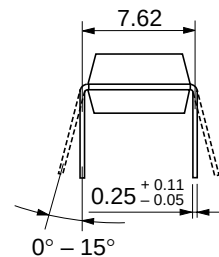


Notes:
1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle 50%
2. Waveform A if for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

Unit: mm

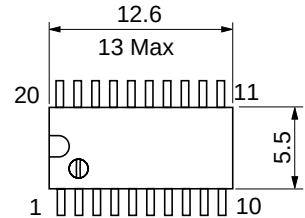


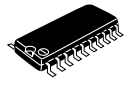


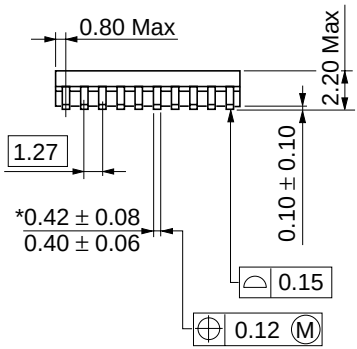


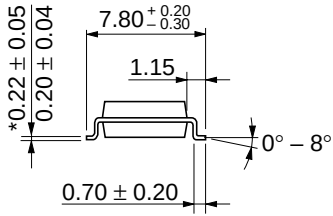
Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g

Unit: mm





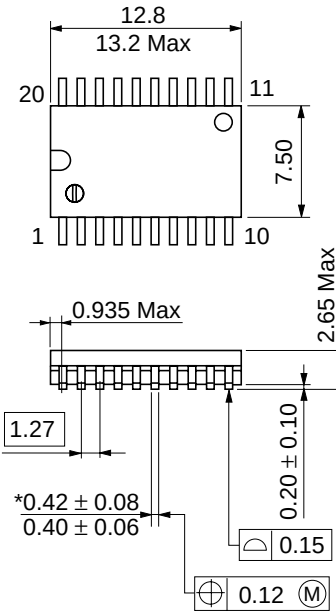


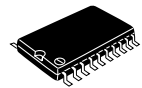


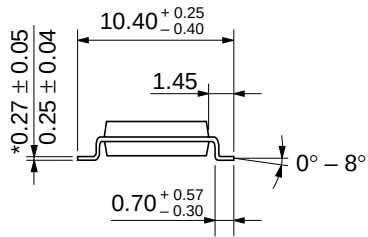
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

Unit: mm







*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX