



FAST CMOS 10-BIT BUFFER

IDT54/74FCT827AT/BT/CT

FEATURES:

- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- A, B, and C speed grades (-15mA I_{OH} , 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Available in the following packages:
 - Industrial: SOIC, SSOP, QSOP, TSSOP
 - Military: CERDIP, LCC, CERPACK

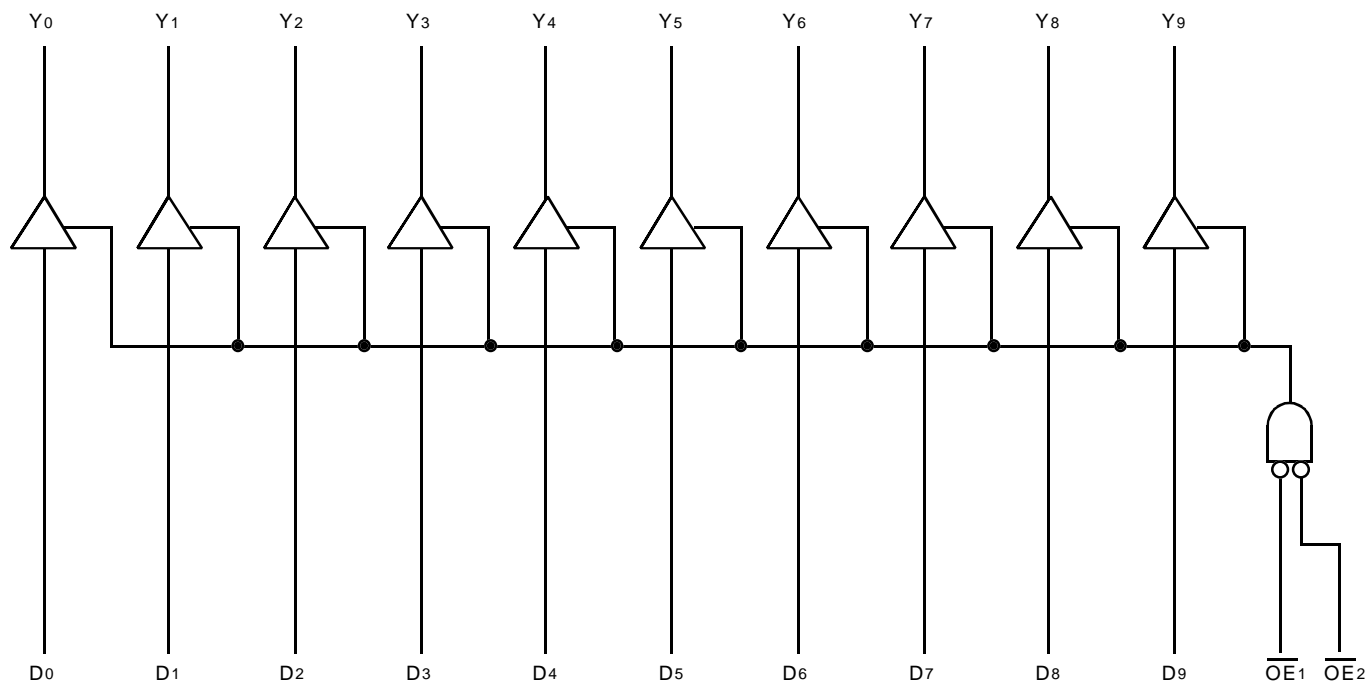
DESCRIPTION:

The FCT827T is built using an advanced dual metal CMOS technology.

The FCT827T 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the FCT827T high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes to ground and all outputs are designed for low-capacitance bus loading in high-impedance state.

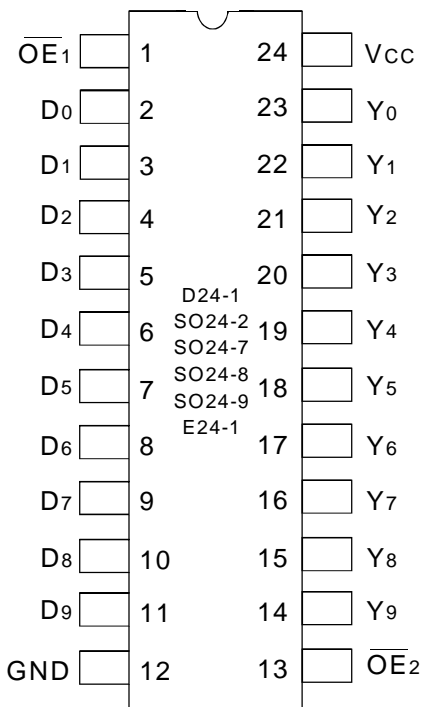
FUNCTIONAL BLOCK DIAGRAM



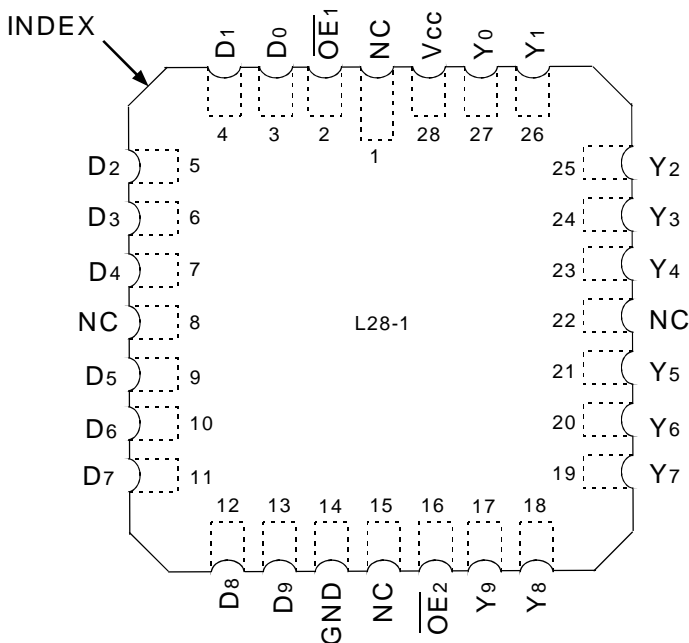
MILITARY AND INDUSTRIAL TEMPERATURE RANGES

AUGUST 2000

PIN CONFIGURATION



CERDIP/ SOIC/ SSOP/ QSOP/ TSSOP/ CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V _{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

8T-link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

8T-link

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Name	I/O	Description
OE _i	I	When both are LOW, the outputs are enabled. When either one or both are HIGH, the outputs are High Z.
D _i	I	10-bit data input.
Y _i	O	10-bit data output.

FUNCTION TABLE(1)

Inputs			Outputs		Function
OE ₁	OE ₂	D _i	Y _i		
L	L	L	L		Transparent
L	L	H	H		
H	X	X	Z		Three-State
X	H	X	Z		

NOTE:

- H = HIGH
L = LOW
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{II}	Input LOW Current ⁽⁴⁾		$V_I = 0.5\text{V}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -6\text{mA MIL}$ $I_{OH} = -8\text{mA IND}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL}$ $I_{OH} = -15\text{mA IND}$	2	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 32\text{mA MIL}$ $I_{OL} = 48\text{mA IND}$	—	0.3	0.5	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_1 = \overline{OE}_2 = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.8	4.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = \text{GND}$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3	6 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5	14 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS - INDUSTRIAL

Symbol	Parameter	Conditions ⁽¹⁾	FCT827AT		FCT827BT		FCT827CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay DI to Yi	CL = 50pF RL = 500Ω	1.5	8	1.5	5	1.5	4.4	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	15	1.5	13	1.5	10	
t _{PZH} t _{PZL}	Output Enable Time \overline{OE}_i to Yi	CL = 50pF RL = 500Ω	1.5	12	1.5	8	1.5	7	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	23	1.5	15	1.5	14	
t _{PHZ} t _{PLZ}	Output Disable Time \overline{OE}_i to Yi	CL = 5pF ⁽³⁾ RL = 500Ω	1.5	9	1.5	6	1.5	5.7	ns
		CL = 50pF RL = 500Ω	1.5	10	1.5	7	1.5	6	

SWITCHING CHARACTERISTICS - MILITARY

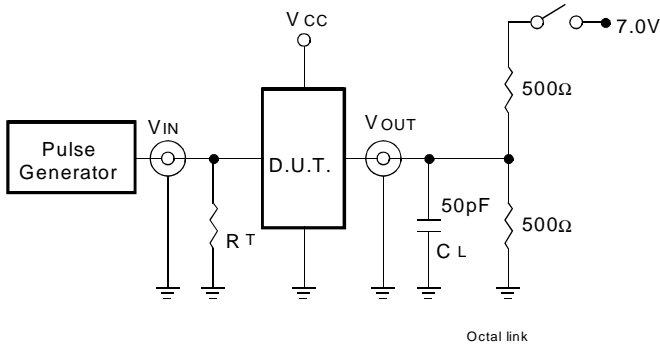
Symbol	Parameter	Conditions ⁽¹⁾	FCT827AT		FCT827BT		FCT827CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay DI to Yi	CL = 50pF RL = 500Ω	1.5	9	1.5	6.5	1.5	5	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	17	1.5	14	1.5	11	
t _{PZH} t _{PZL}	Output Enable Time \overline{OE}_i to Yi	CL = 50pF RL = 500Ω	1.5	13	1.5	9	1.5	8	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	25	1.5	16	1.5	15	
t _{PHZ} t _{PLZ}	Output Disable Time \overline{OE}_i to Yi	CL = 5pF ⁽³⁾ RL = 500Ω	1.5	9	1.5	7	1.5	6.7	ns
		CL = 50pF RL = 500Ω	1.5	10	1.5	8	1.5	7	

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

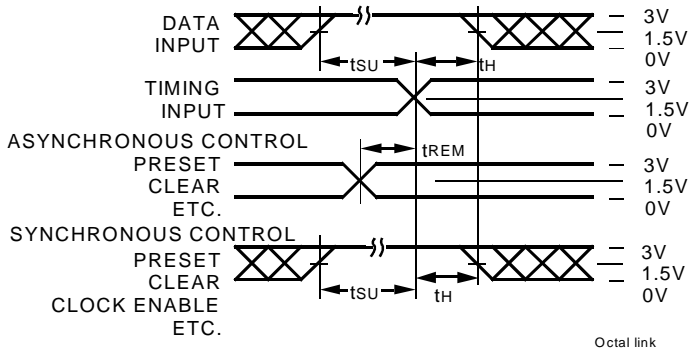
8-link

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

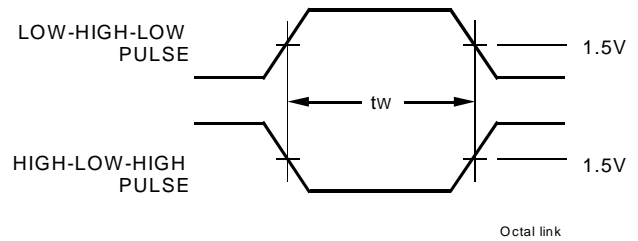
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES

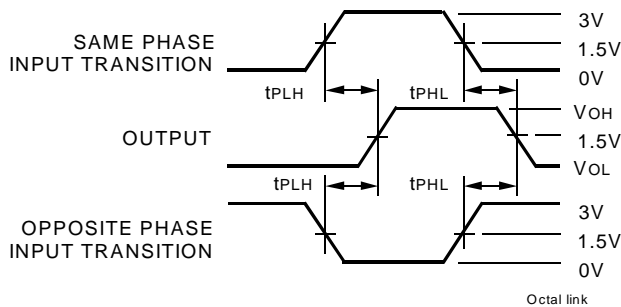


Octal link

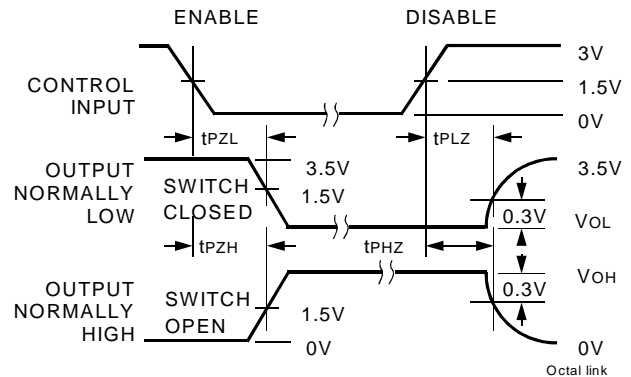
PULSE WIDTH



PROPAGATION DELAY



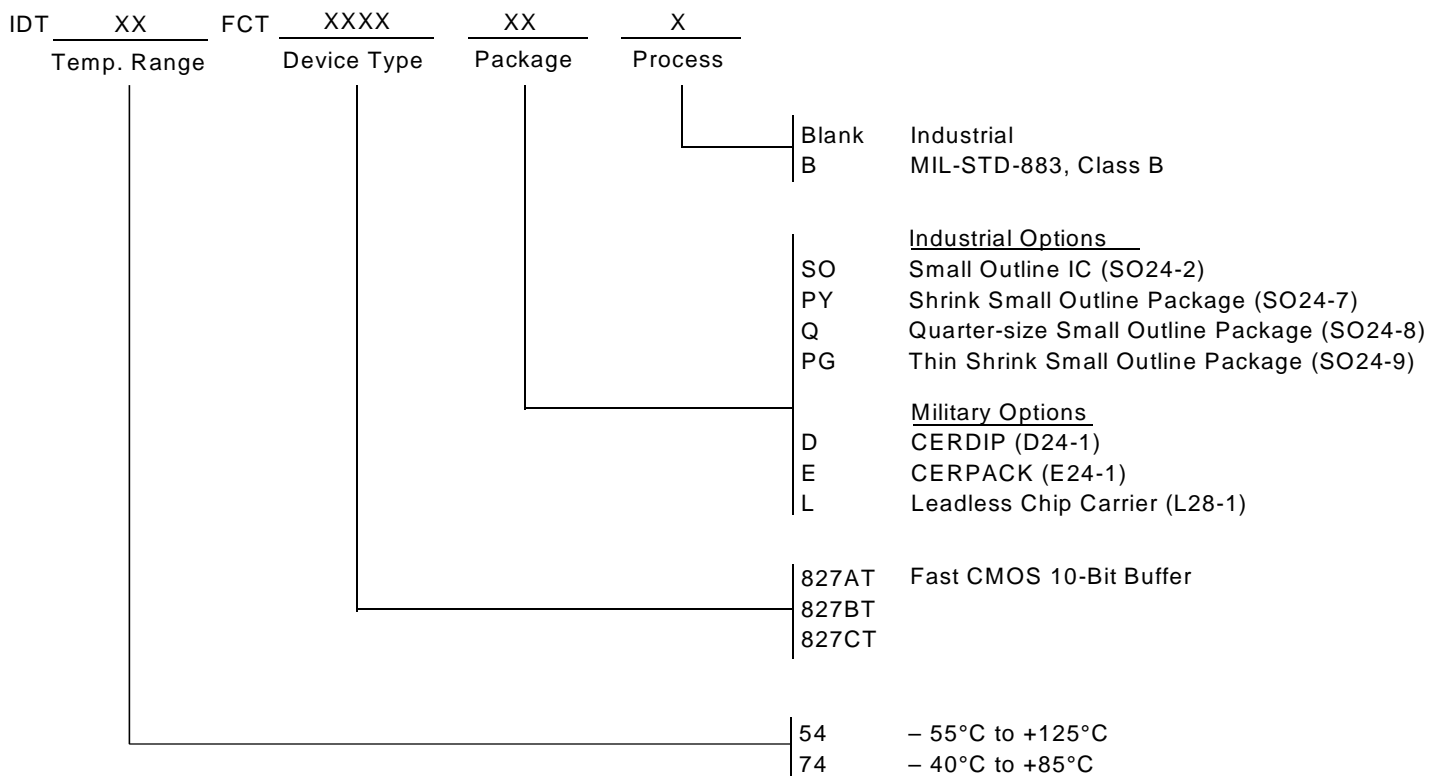
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
 www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.
 The IDT logo is a registered trademark of Integrated Device Technology, Inc.