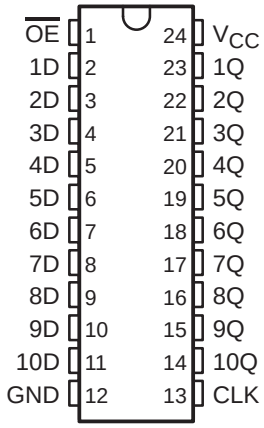
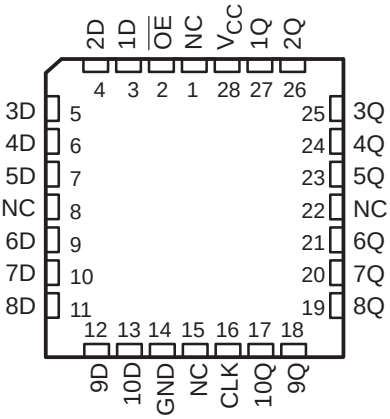
- **Functionally Equivalent to AMD's AM29821**
- **Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Outputs Have Undershoot-Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce dc Loading Effects**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54AS821A . . . JT PACKAGE
SN74AS821A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS821A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are true to the data (D) input.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

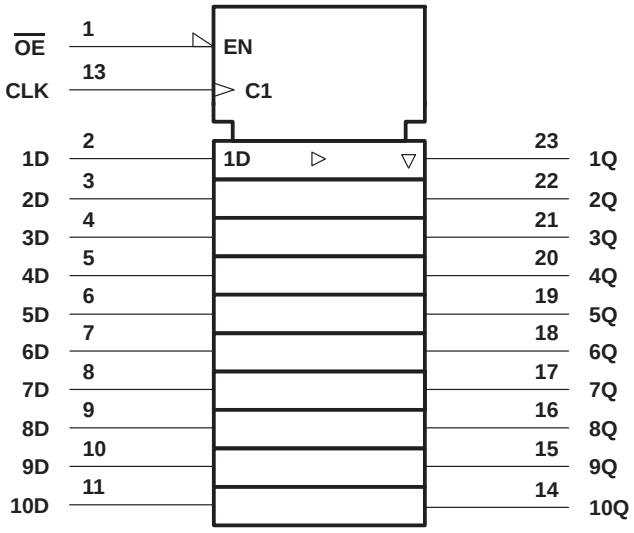
$\overline{OE}$ does not affect the internal operation of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS821A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS821A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

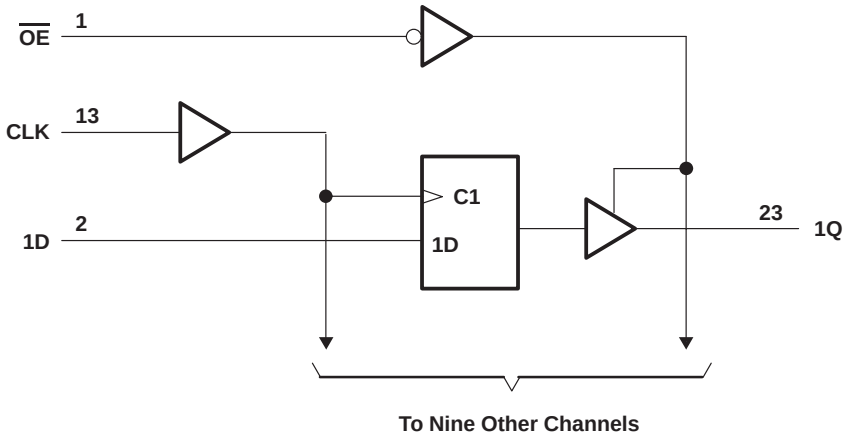
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54AS821A . . . . . –55°C to 125°C
SN74AS821A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS821A			SN74AS821A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			32			48	mA
t_w*	Pulse duration, CLK high or low	9			8			ns
t_{su}*	Setup time, data before CLK↑	7			6			ns
t_h*	Hold time, data after CLK↑	0			0			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS821A			SN74AS821A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} –2			V_{CC} –2			V
	V_{CC} = 4.5 V	I_{OH} = –15 mA	2.4	3.2		2.4	3.2		
		I_{OH} = –24 mA	2			2			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 32 mA		0.25	0.5				V
		I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–50			–50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5			–0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		55	88		55	88	mA
		Outputs low		68	109		68	109	
		Outputs disabled		70	113		70	113	

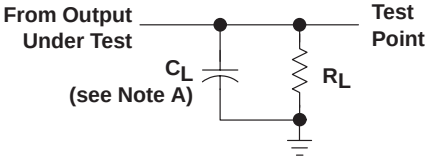
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

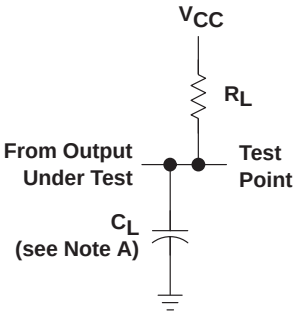
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54AS821A		SN74AS821A		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	14	3.5	13	
t_{PZH}	$\overline{OE}$	Any Q	4	12	3	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OE}$	Any Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

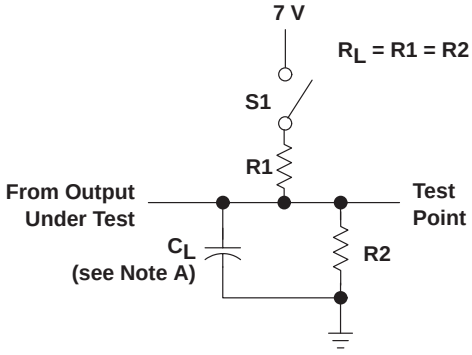
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



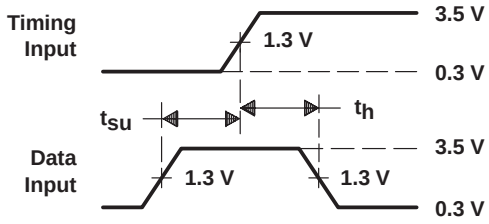
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



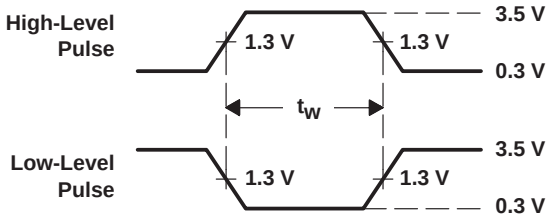
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



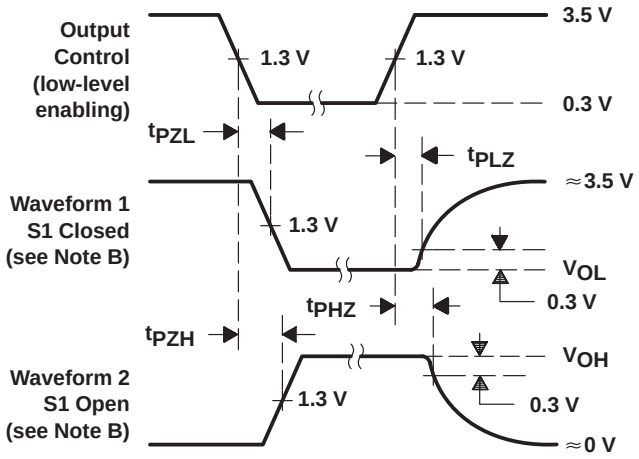
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



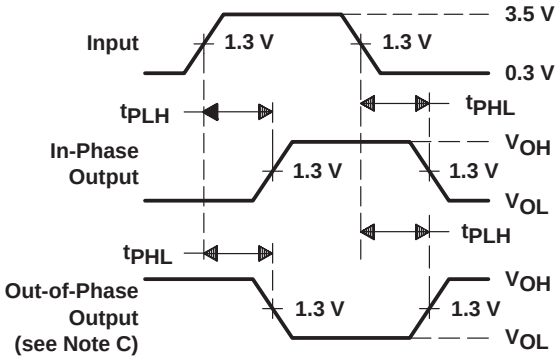
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY | APPLICATION NOTES | RELATED DOCUMENTS

PRODUCT SUPPORT: TRAINING

SN54AS821A, 10-Bit Bus Interface Flip-Flops With 3-State Outputs

DEVICE STATUS: **ACTIVE**

FEATURES

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DESCRIPTION

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TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sdas230a.pdf (92 KB) (Updated: 08/01/1995)
Full datasheet in Zipped PostScript: sdas230a.psz (88 KB)

APPLICATION NOTES

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View Application Reports for Digital Logic

- Advanced Schottky (ALS and AS) Logic Families (SDAA010 - Updated: 08/01/1995)
- Advanced Schottky Load Management (SDYA016 - Updated: 02/01/1997)
- Designing With Logic (SDYA009C - Updated: 06/01/1997)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTS

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- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB - Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB - Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (SCAU001A, 850 KB - Updated: 03/01/1996)

PRICING/AVAILABILITY

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ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	BUDGETARY PRICE US$/UNIT QTY=1000+	PACK QTY	DSCC NUMBER	PRICING/AVAILABILITY
SN54AS821AJT	JT	24	-55 TO 125	ACTIVE	5.43	1		Check stock or order
SNJ54AS821AFK	FK	28	-55 TO 125	ACTIVE	13.23	168	5962-9078001M3A	Check stock or order
SNJ54AS821AJT	JT	24	-55 TO 125	ACTIVE	6.36	1	5962-9078001MLA	Check stock or order
SNJ54AS821AW	W	24	-55 TO 125	ACTIVE	12.24	170	5962-9078001MKA	Check stock or order

Table Data Updated on: 11/19/2000