



# 54ABT/74ABT374C

## Octal D-Type Flip-Flop with TRI-STATE® Outputs

### General Description

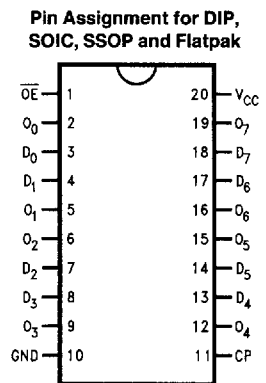
The 'ABT374C is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops.

### Features

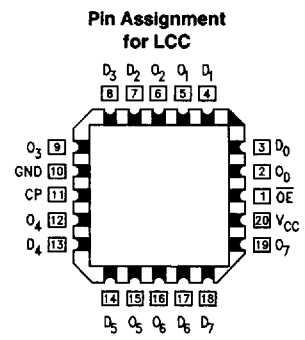
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

**Ordering Code:** See Section 10

### Connection Diagrams



TL/F/11510-1



TL/F/11510-2

### Pin Descriptions

Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Outputs

### Functional Description

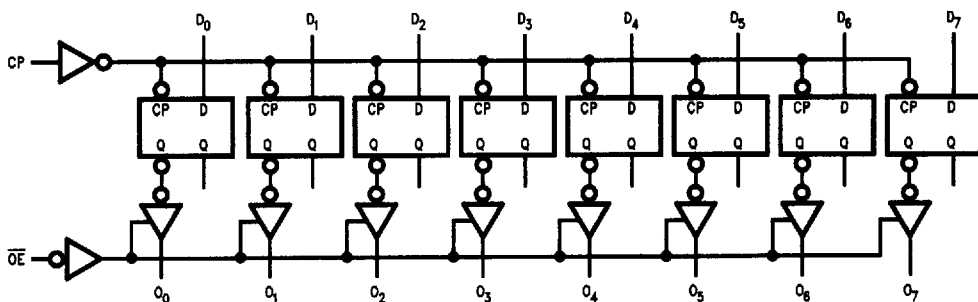
The 'ABT374C consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs are in a high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

### Logic Diagram



TL/F/11510-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	-0.5V to 5.5V -0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

DC Latchup Source Current:	OE Pin	-150 mA
(Across Comm Operating Range)	Other Pins	-500 mA
Over Voltage Latchup (I/O)		10V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

### Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	-40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100mV/ns

### DC Electrical Characteristics

Symbol	Parameter	ABT374C			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage						Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage						
V <sub>OH</sub>	Output HIGH Voltage	54ABT/74ABT	2.5		V	Min	I <sub>IN</sub> = -18 mA
		54ABT	2.0		V	Min	I <sub>OH</sub> = -3 mA
		74ABT	2.0		V	Min	I <sub>OH</sub> = -24 mA
					V	Min	I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage	54ABT	0.55		V	Min	I <sub>OL</sub> = 48 mA
		74ABT	0.55		V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current				5	μA	V <sub>IN</sub> = 2.7V (Note 2)
					5	μA	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test				7	μA	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current				-5	μA	V <sub>IN</sub> = 0.5V (Note 2)
					-5	μA	V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OZH</sub>	Output Leakage Current				50	μA	0 - 5.5V V <sub>OUT</sub> = 2.7V; OE = 2.0V
I <sub>OZL</sub>	Output Leakage Current				-50	μA	0 - 5.5V V <sub>OUT</sub> = 0.5V; OE = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current	-100	-275		mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEX</sub>	Output High Leakage Current				50	μA	Max V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test				100	μA	0.0 V <sub>OUT</sub> = 5.5V; All Others V <sub>CC</sub> or GND
I <sub>CCH</sub>	Power Supply Current				50	μA	Max All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current				30	mA	Max All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current				50	μA	Max OE = V <sub>CC</sub> ; All Others at V <sub>CC</sub> or GND
I <sub>CC1</sub>	Additional I <sub>CC</sub> /Input	Outputs Enabled	2.5		mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or GND
	Outputs TRI-STATE	2.5		mA			
	Outputs TRI-STATE	2.5		mA			
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 2)	No Load	0.30		mA/ MHz	Max	Outputs Open OE = GND, (Note 1) One Bit Toggling, 50% Duty Cycle

**Note 1:** For 8-bit toggling, I<sub>CCD</sub> < 0.8 mA/MHz

**Note 2:** Guaranteed, but not tested.

**DC Electrical Characteristics** (SOIC package) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		0.5	0.8	V	5.0	T <sub>A</sub> = 25°C (Note 1)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-1.3	-0.9		V	5.0	T <sub>A</sub> = 25°C (Note 1)
V <sub>OHV</sub>	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T <sub>A</sub> = 25°C (Note 3)
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	2.0	1.6		V	5.0	T <sub>A</sub> = 25°C (Note 2)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		1.3	0.8	V	5.0	T <sub>A</sub> = 25°C (Note 2)

**Note 1:** Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

**Note 2:** Max number of data inputs (n) switching. n - 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.

**Note 3:** Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

**AC Electrical Characteristics:** See Section 2 for Waveforms (SOIC and SSOP package)

Symbol	Parameter	74ABT			54ABT		74ABT		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Max Clock Frequency	150	200		150		150		MHz	
t <sub>PLH</sub>	Propagation Delay CP to O <sub>n</sub>	1.5	3.2	5.0	1.8	6.6	1.5	5.0	ns	2-3, 5
t <sub>PHL</sub>	CP to O <sub>n</sub>	1.5	3.3	5.0	2.6	7.6	1.5	5.0	ns	
t <sub>PZH</sub>	Output Enable Time	1.5	3.1	5.3	0.8	6.5	1.5	5.3	ns	2-4
t <sub>PZL</sub>		1.5	3.1	5.3	1.5	7.2	1.5	5.3	ns	
t <sub>PHZ</sub>	Output Disable Time	1.0	3.6	5.4	1.3	7.2	1.0	5.4	ns	2-4
t <sub>PLZ</sub>		1.0	3.4	5.4	1.0	7.0	1.0	5.4	ns	

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74ABT		54ABT		74ABT		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH	1.5		2.5		1.0		ns	2-6
t <sub>s</sub> (L)	or LOW D <sub>n</sub> to CP	1.5		2.5		1.5		ns	
t <sub>h</sub> (H)	Hold Time, HIGH	1.0		2.5		1.0		ns	2-6
t <sub>h</sub> (L)	or LOW D <sub>n</sub> to CP	1.0		2.5		1.0		ns	
t <sub>w</sub> (H)	Pulse Width, CP	3.0		3.3		3.0		ns	2-3
t <sub>w</sub> (L)	HIGH or LOW	3.0		3.3		3.0		ns	

**Extended AC Electrical Characteristics:** See Section 2 for Waveforms (SOIC package)

Symbol	Parameter	74ABTC		74ABTC		74ABTC		Units	Fig. No.
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 4)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 250\text{ pF}$ (Note 5)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 6)			
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $O_n$	1.5 1.5	5.7 5.7	2.0 2.0	7.8 7.8	2.0 2.0	10.0 10.0	ns	2-3, 5
$t_{PZH}$ $t_{PZL}$	Output Enable Time	1.5 1.5	6.2 6.2	2.0 2.0	8.0 8.0	2.0 2.0	10.5 10.5	ns	2-4
$t_{PHZ}$ $t_{PZL}$	Output Disable Time	1.0 1.0	5.5 5.5	(Note 7)		(Note 7)		ns	2-4

**Note 4:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc).

**Note 5:** This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

**Note 6:** This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 7:** The TRI-STATE delay Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet

**Skew:** See Section 2 (SOIC package) (Note 3)

Symbol	Parameter	74ABT		74ABT		Units	Fig. No.
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 3)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 4)			
		Max		Max			
$t_{OSHL}$ (Note 1)	Pin to Pin Skew HL Transitions	1.0		1.8		ns	2-13
$t_{OSLH}$ (Note 1)	Pin to Pin Skew LH Transitions	1.0		1.8		ns	2-13
$t_{PS}$ (Note 5)	Duty Cycle LH-HL Skew	1.8		4.3		ns	2-14
$t_{OST}$ (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0		4.3		ns	2-17
$t_{PV}$ (Note 2)	Device to Device Skew LH/HL Transitions	2.5		4.6		ns	2-20

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW ( $t_{OSHL}$ ), LOW to HIGH ( $t_{OSLH}$ ), or any combination switching LOW to HIGH and/or HIGH to LOW ( $t_{OST}$ ). This specification is guaranteed but not tested.

**Note 2:** Propagation delay variation for a given set of conditions (i.e., temperature and  $V_{CC}$ ) from device to device. This specification is guaranteed but not tested.

**Note 3:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc)

**Note 4:** This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load

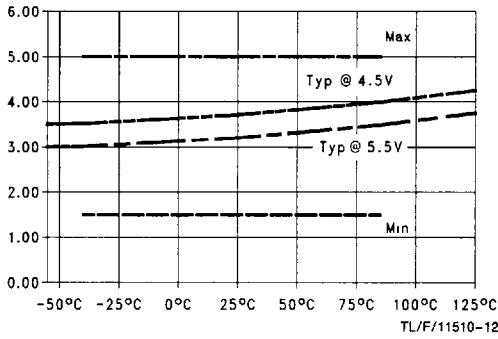
**Note 5:** This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

**Capacitance**

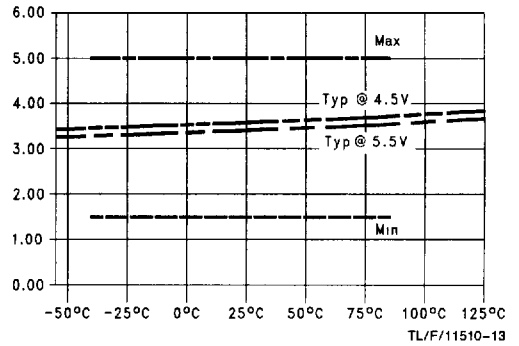
Symbol	Parameter	Typ	Units	Conditions ( $T_A = 25^\circ\text{C}$ )
$C_{IN}$	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$
$C_{OUT}$ (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$

**Note 1:**  $C_{OUT}$  is measured at frequency  $f = 1\text{ MHz}$ , per MIL-STD-883B, Method 3012.

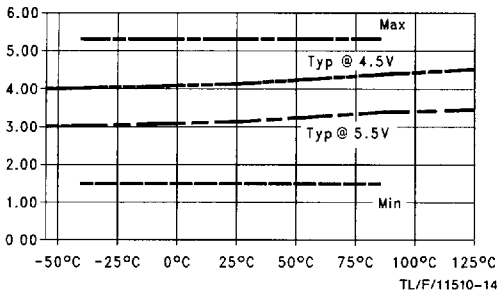
**$t_{PLH}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Clock to Output**



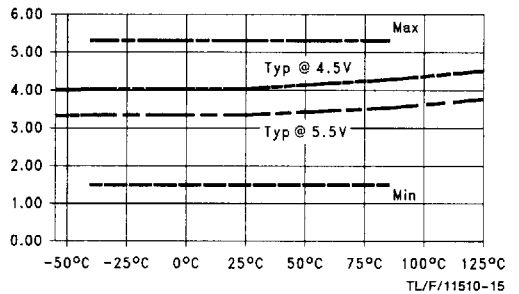
**$t_{PHL}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Clock to Output**



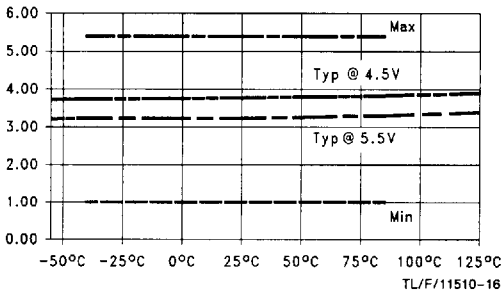
**$t_{PZH}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching OE to Output**



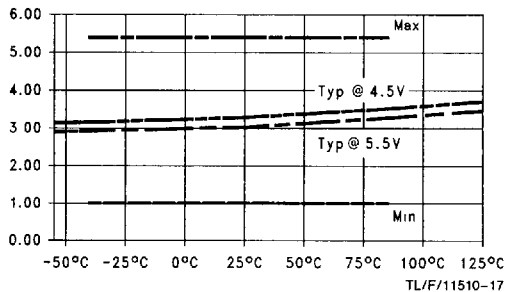
**$t_{PZL}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching OE to Output**



**$t_{PHZ}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching OE to Output**

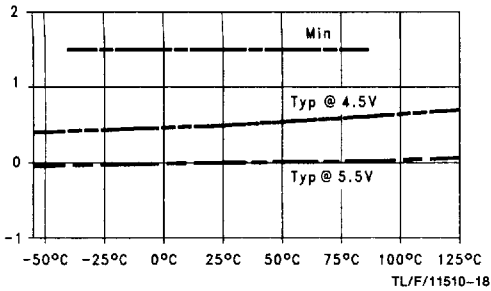


**$t_{PLZ}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching OE to Output**

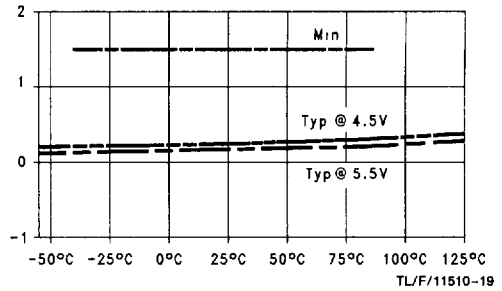


Dashed lines represent design characteristics, for specified guarantees, refer to AC Characteristics Tables

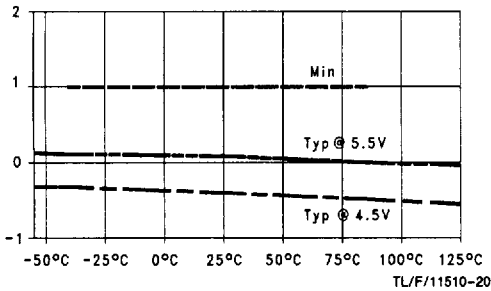
**$t_{SET}$  LOW vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Data to Clock**



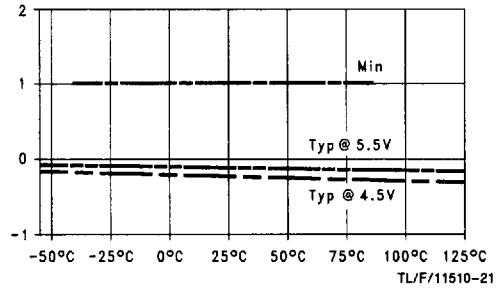
**$t_{SET}$  HIGH vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Data to Clock**



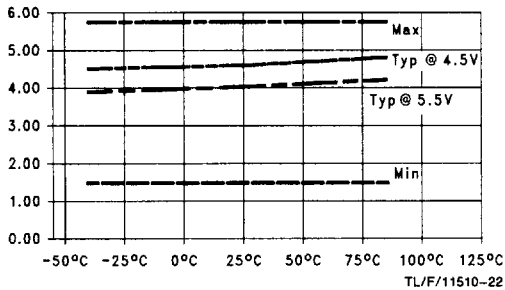
**$t_{HOLD}$  HIGH vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Data to Clock**



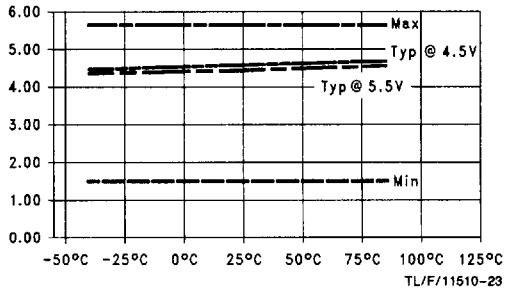
**$t_{HOLD}$  LOW vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
1 Output Switching Data to Clock**



**$t_{PLH}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching Clock to Output**

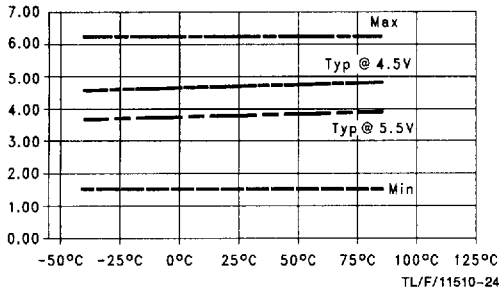


**$t_{PHL}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching Clock to Output**

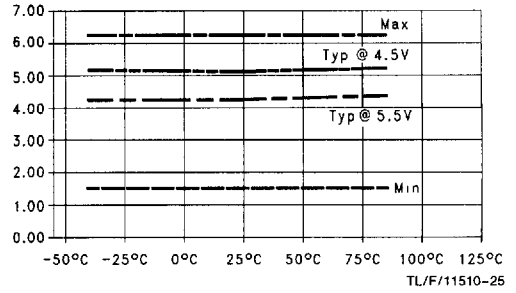


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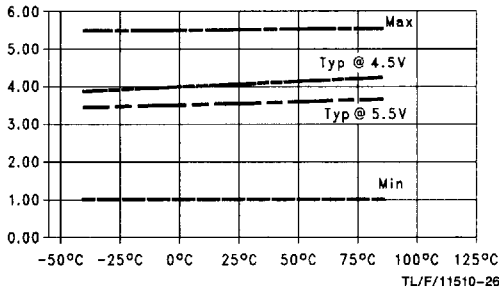
**$t_{pZH}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching  $\overline{OE}$  to Output**



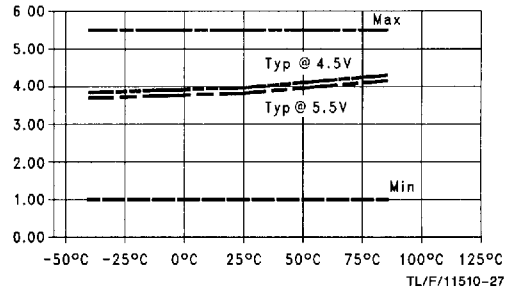
**$t_{pZL}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching  $\overline{OE}$  to Output**



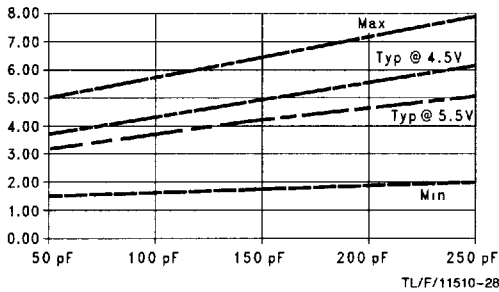
**$t_{pHZ}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching  $\overline{OE}$  to Output**



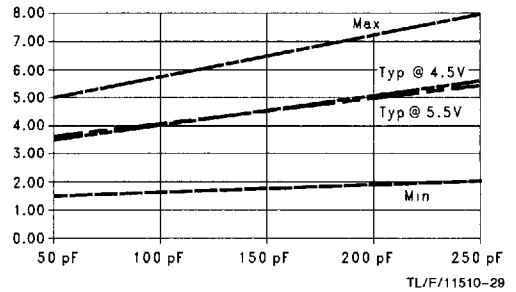
**$t_{pLZ}$  vs Temperature ( $T_A$ )  $C_L = 50$  pF,  
8 Outputs Switching  $\overline{OE}$  to Output**



**$t_{pLH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
1 Output Switching Clock to Output**



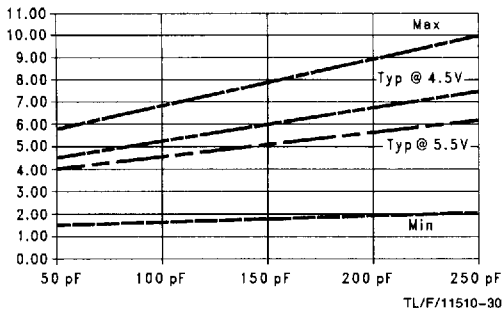
**$t_{pHL}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
1 Output Switching Clock to Output**



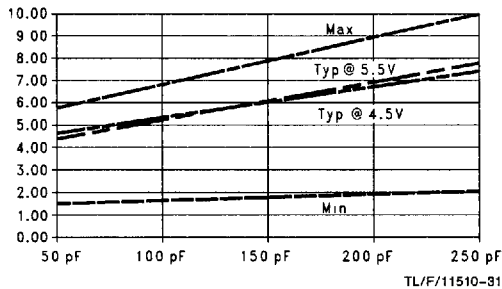
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.



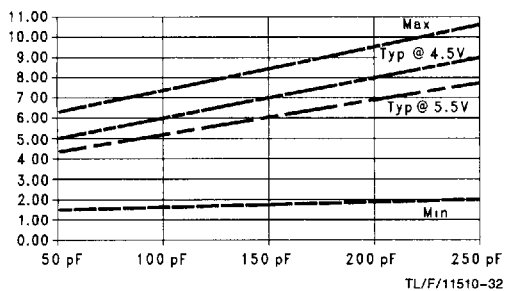
**$t_{PLH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching Clock to Output**



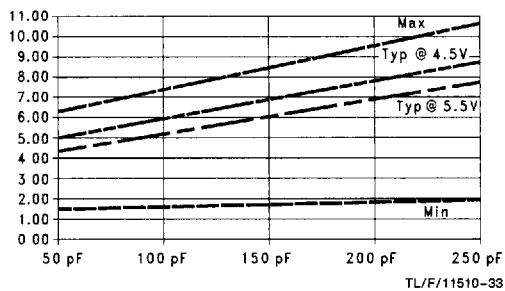
**$t_{PHL}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching Clock to Output**



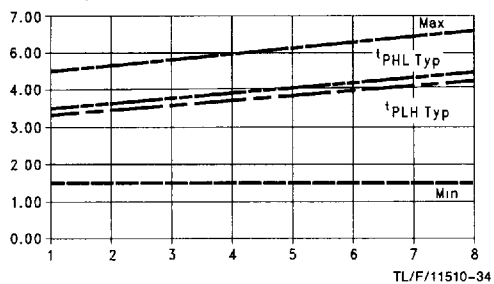
**$t_{pZH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching OE to Output**



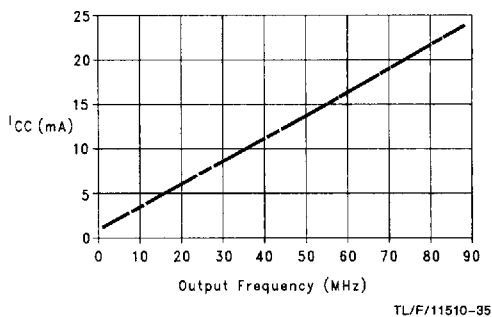
**$t_{pZL}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching OE to Output**



**$t_{PLH}$  and  $t_{PHL}$  vs Number Outputs Switching  
 $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ ,  
Outputs In Phase Clock to Output**



**Typical  $I_{CC}$  vs Output Switching Frequency  
 $C_L = 0\text{ pF}$ ,  $V_{CC} = V_{IH} = 5.5\text{V}$ , 1 Output  
Switching at 50% Duty Cycle Clock to Output**



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.